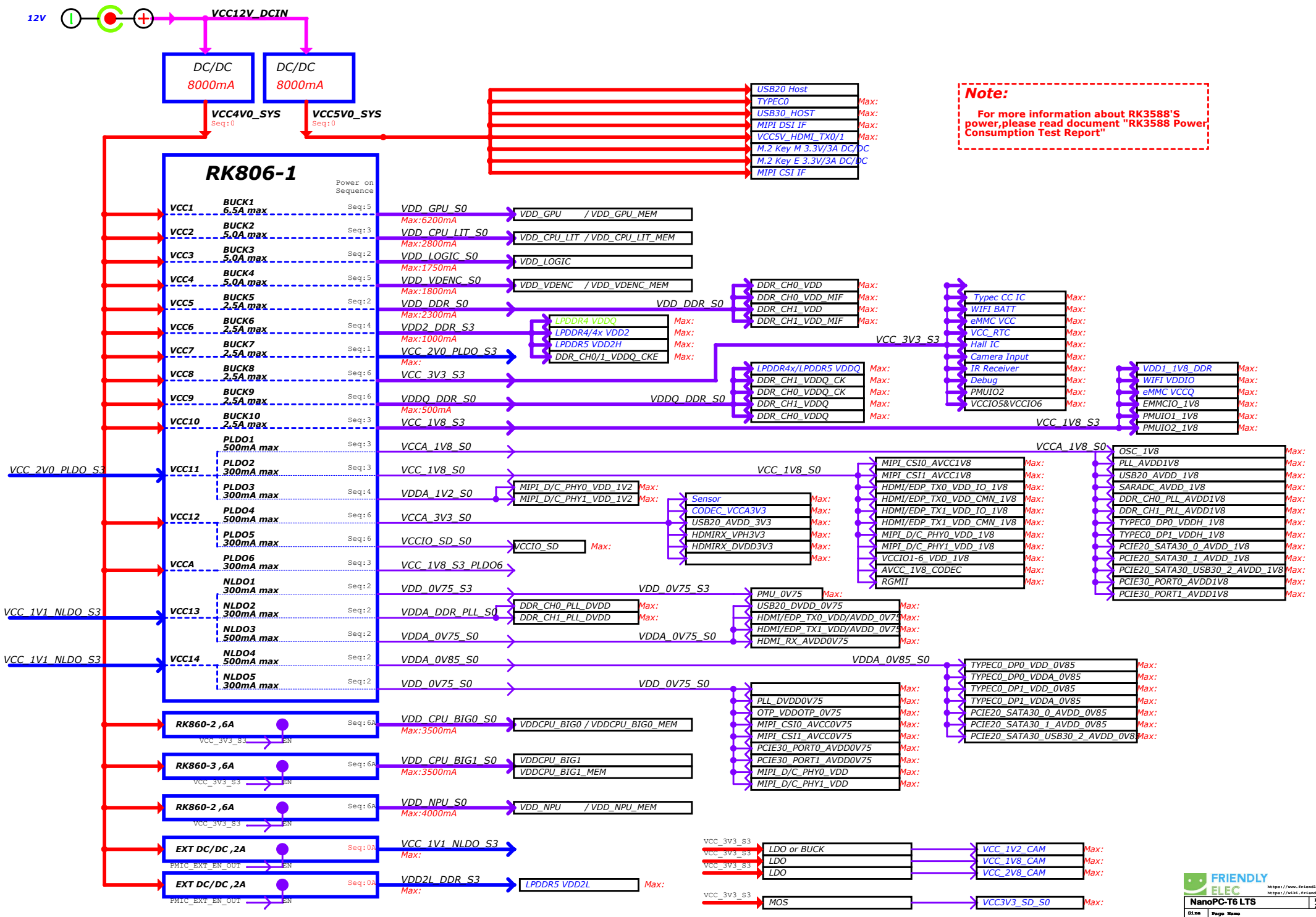
Power Tree


12V
VCC12V_DCIN
DC/DC 8000mA
DC/DC 8000mA
VCC4V0_SYS Seq:0
VCC5V0_SYS Seq:0
USB20 Host
TYPEC0 Max:
USB30_HOST Max:
MIPI DSI IF Max:
VCC5V_HDMI_TX0/1 Max:
M.2 Key M 3.3V/3A DC/DC
M.2 Key E 3.3V/3A DC/DC
MIPI CSI IF
Note:
For more information about RK3588'S power,please read document "RK3588 Power Consumption Test Report"
RK806-1
Power on Sequence
VCC1 BUCK1 6.5A max Seq:5
VCC2 BUCK2 5.0A max Seq:3
VCC3 BUCK3 5.0A max Seq:2
VCC4 BUCK4 5.0A max Seq:5
VCC5 BUCK5 2.5A max Seq:2
VCC6 BUCK6 2.5A max Seq:4
VCC7 BUCK7 2.5A max Seq:1
VCC8 BUCK8 2.5A max Seq:6
VCC9 BUCK9 2.5A max Seq:6
VCC10 BUCK10 2.5A max Seq:3
PLDO1 500mA max Seq:3
VCC11 PLDO2 300mA max Seq:3
PLDO3 300mA max Seq:4
VCC12 PLDO4 500mA max Seq:6
PLDO5 300mA max Seq:6
VCCA PLDO6 300mA max Seq:3
NLDO1 300mA max Seq:2
VCC13 NLDO2 300mA max Seq:2
NLDO3 500mA max Seq:2
VCC14 NLDO4 500mA max Seq:2
NLDO5 300mA max Seq:2
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
VCC_1V1_NLDO_S3
VDD_GPU_S0 Max:6200mA
VDD_CPU_LIT_S0 Max:2800mA
VDD_LOGIC_S0 Max:1750mA
VDD_VDENC_S0 Max:1800mA
VDD_DDR_S0 Max:2300mA
VDD2_DDR_S3 Max:1000mA
VCC_2V0_PLDO_S3 Max:
VCC_3V3_S3
VDDQ_DDR_S0 Max:500mA
VCC_1V8_S3
VCCA_1V8_S0
VCC_1V8_S0
VDDA_1V2_S0
VCCA_3V3_S0
VCCIO_SD_S0
VCC_1V8_S3_PLDO6
VDD_0V75_S3
VDDA_DDR_PLL_S0
VDDA_0V75_S0
VDDA_0V85_S0
VDD_0V75_S0
VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC
VDD_VDENC / VDD_VDENC_MEM
VDD_DDR_S0
LPDDR4 VDDQ Max:
LPDDR4/4x VDD2 Max:
LPDDR5 VDD2H Max:
DDR_CH0/1_VDDQ_CKE Max:
DDR_CH0_VDD Max:
DDR_CH0_VDD_MIF Max:
DDR_CH1_VDD Max:
DDR_CH1_VDD_MIF Max:
VCC_3V3_S3
Typec CC IC Max:
WIFI BATT Max:
eMMC VCC Max:
VCC_RTC Max:
Hall IC Max:
Camera Input Max:
IR Receiver Max:
Debug Max:
PMUIO2 Max:
VCCIO5&VCCIO6 Max:
VDDQ_DDR_S0
LPDDR4x/LPDDR5 VDDQ Max:
DDR_CH1_VDDQ_CK Max:
DDR_CH0_VDDQ_CK Max:
DDR_CH1_VDDQ Max:
DDR_CH0_VDDQ Max:
VCC_1V8_S3
VDD1_1V8_DDR Max:
WIFI VDDIO Max:
eMMC VCCQ Max:
EMMCIO_1V8 Max:
PMUIO1_1V8 Max:
PMUIO2_1V8 Max:
VCCA_1V8_S0
OSC_1V8 Max:
PLL_AVDD1V8 Max:
USB20_AVDD_1V8 Max:
SARADC_AVDD_1V8 Max:
DDR_CH0_PLL_AVDD1V8 Max:
DDR_CH1_PLL_AVDD1V8 Max:
TYPEC0_DP0_VDDH_1V8 Max:
TYPEC0_DP1_VDDH_1V8 Max:
PCIE20_SATA30_0_AVDD_1V8 Max:
PCIE20_SATA30_1_AVDD_1V8 Max:
PCIE20_SATA30_USB30_2_AVDD_1V8 Max:
PCIE30_PORT0_AVDD1V8 Max:
PCIE30_PORT1_AVDD1V8 Max:
MIPI_D/C_PHY0_VDD_1V2 Max:
MIPI_D/C_PHY1_VDD_1V2 Max:
Sensor Max:
CODEC_VCCA3V3 Max:
USB20_AVDD_3V3 Max:
HDMIRX_VPH3V3 Max:
HDMIRX_DVDD3V3 Max:
VCCIO_SD Max:
MIPI_CSI0_AVCC1V8 Max:
MIPI_CSI1_AVCC1V8 Max:
HDMI/EDP_TX0_VDD_IO_1V8 Max:
HDMI/EDP_TX0_VDD_CMN_1V8 Max:
HDMI/EDP_TX1_VDD_IO_1V8 Max:
HDMI/EDP_TX1_VDD_CMN_1V8 Max:
MIPI_D/C_PHY0_VDD_1V8 Max:
MIPI_D/C_PHY1_VDD_1V8 Max:
VCCIO1-6_VDD_1V8 Max:
AVCC_1V8_CODEC Max:
RGMII Max:
DDR_CH0_PLL_DVDD Max:
DDR_CH1_PLL_DVDD Max:
PMU_0V75 Max:
USB20_DVDD_0V75 Max:
HDMI/EDP_TX0_VDD/AVDD_0V75 Max:
HDMI/EDP_TX1_VDD/AVDD_0V75 Max:
HDMI_RX_AVDD0V75 Max:
TYPEC0_DP0_VDD_0V85 Max:
TYPEC0_DP0_VDDA_0V85 Max:
TYPEC0_DP1_VDD_0V85 Max:
TYPEC0_DP1_VDDA_0V85 Max:
PCIE20_SATA30_0_AVDD_0V85 Max:
PCIE20_SATA30_1_AVDD_0V85 Max:
PCIE20_SATA30_USB30_2_AVDD_0V8 Max:
PLL_DVDD0V75 Max:
OTP_VDDOTP_0V75 Max:
MIPI_CSI0_AVCC0V75 Max:
MIPI_CSI1_AVCC0V75 Max:
PCIE30_PORT0_AVDD0V75 Max:
PCIE30_PORT1_AVDD0V75 Max:
MIPI_D/C_PHY0_VDD Max:
MIPI_D/C_PHY1_VDD Max:
RK860-2 ,6A Seq:6A
RK860-3 ,6A Seq:6A
RK860-2 ,6A Seq:6A
EXT DC/DC ,2A Seq:0A
EXT DC/DC ,2A Seq:0A
VCC_3V3_S3
EN
PMIC_EXT_EN_OUT
VDD_CPU_BIG0_S0 Max:3500mA
VDD_CPU_BIG1_S0 Max:3500mA
VDD_NPU_S0 Max:4000mA
VCC_1V1_NLDO_S3 Max:
VDD2L_DDR_S3 Max:
VDDCPU_BIG0 / VDDCPU_BIG0_MEM
VDDCPU_BIG1
VDDCPU_BIG1_MEM
VDD_NPU / VDD_NPU_MEM
LPDDR5 VDD2L Max:
VCC_3V3_S3
LDO or BUCK
LDO
LDO
VCC_1V2_CAM Max:
VCC_1V8_CAM Max:
VCC_2V8_CAM Max:
MOS
VCC3V3_SD_S0 Max:
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NanoPC-T6 LTS
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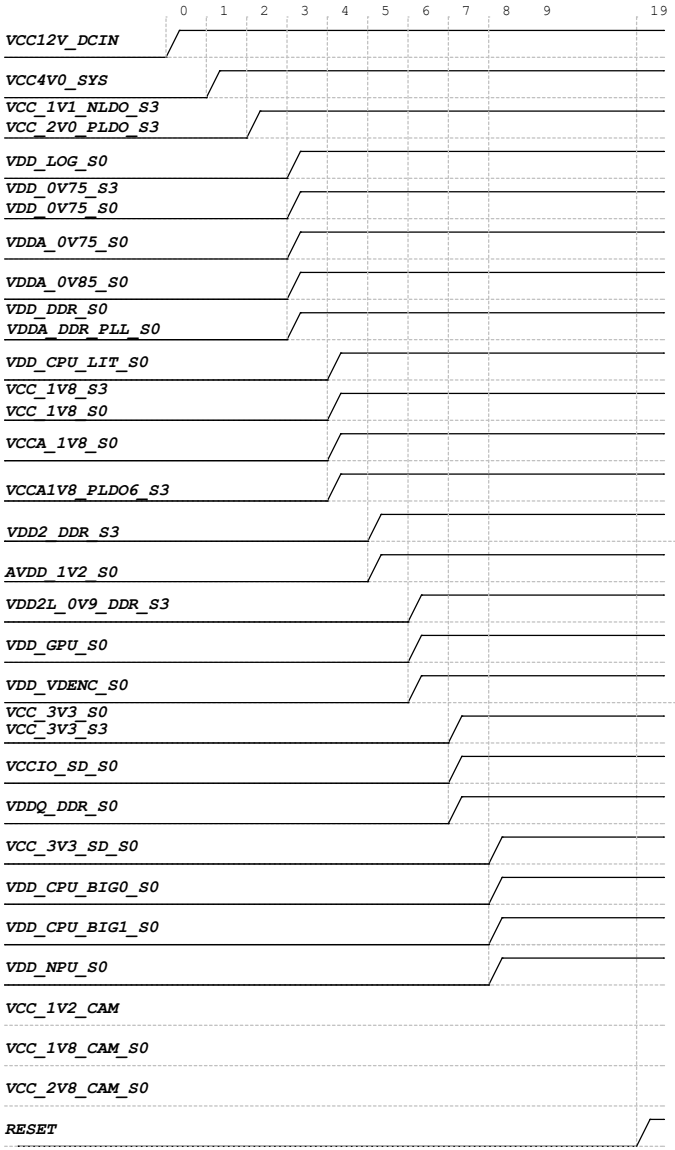
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

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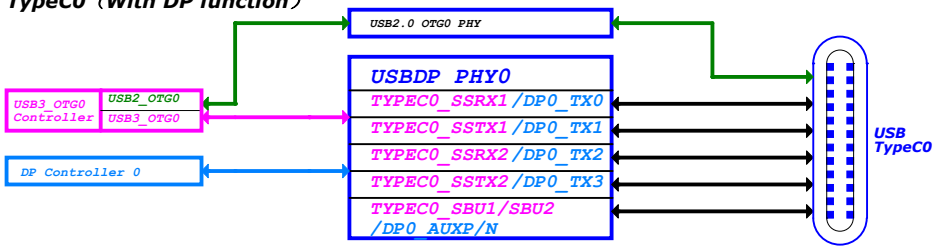
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1M/DP0_TX1M	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1M/DP1_TX1M	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

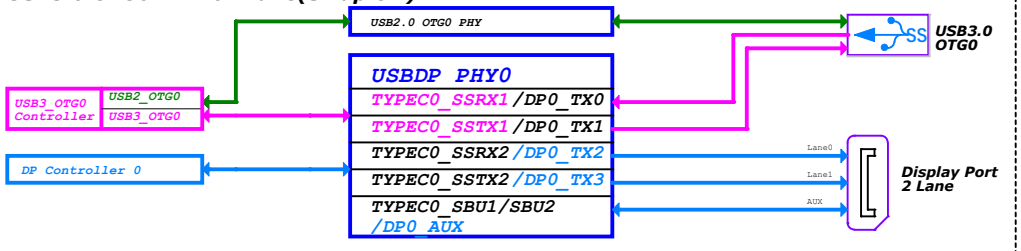
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

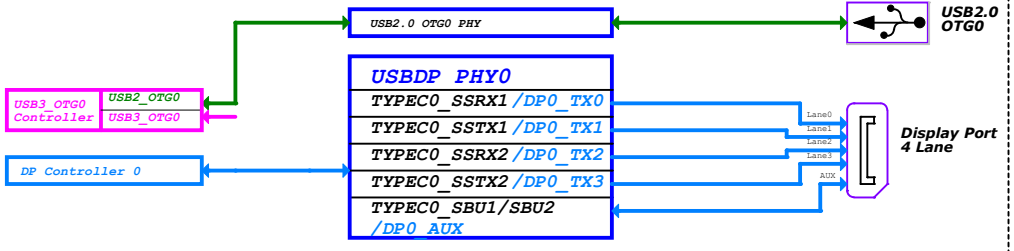
Config0:
TypeC0（With DP function）



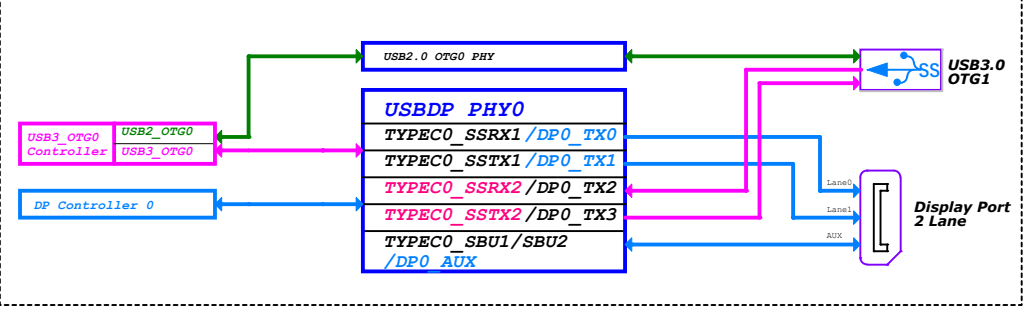
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



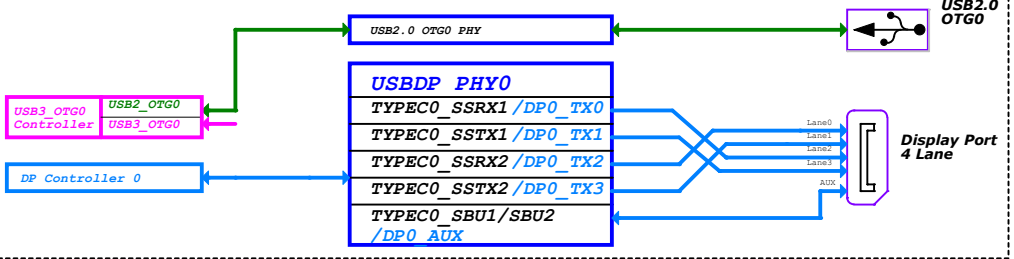
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



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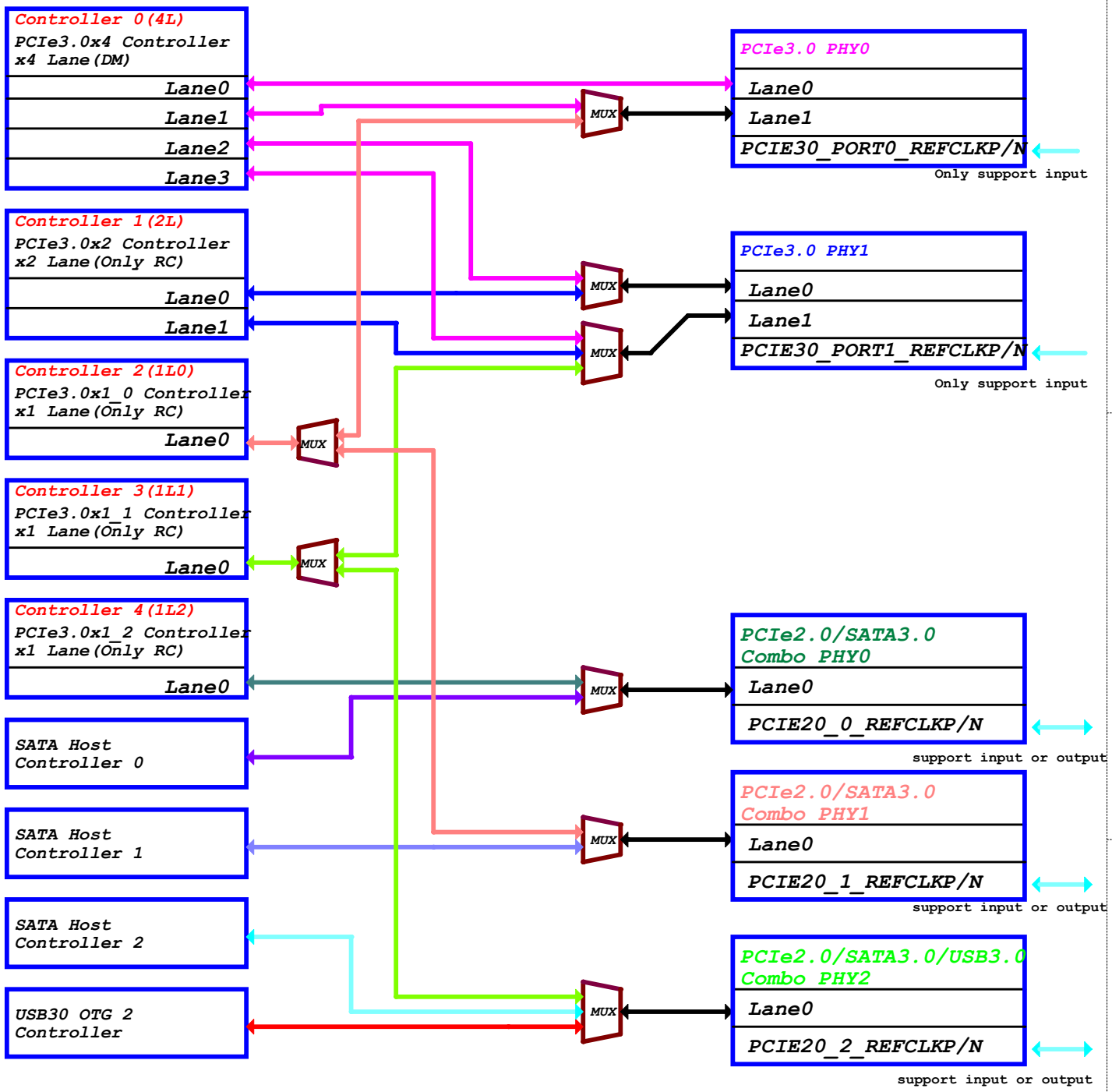
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

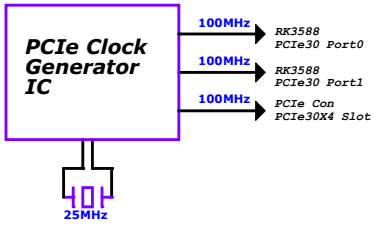
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

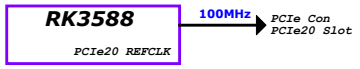
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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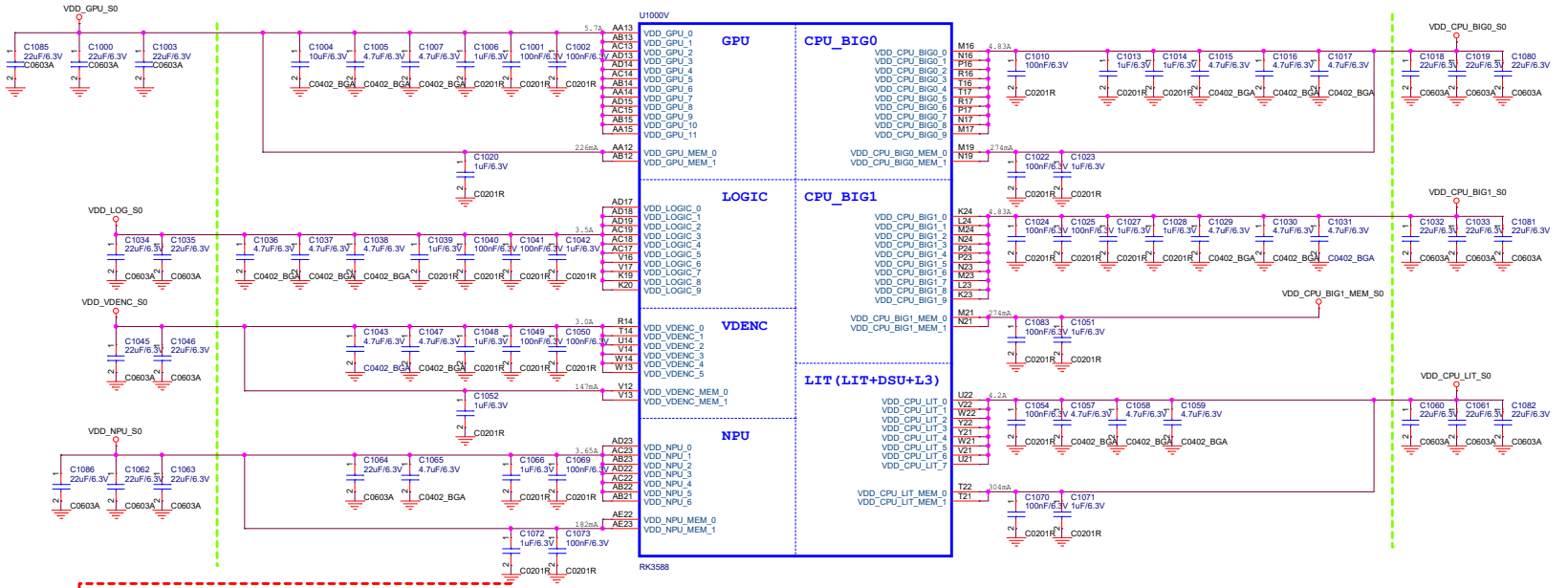
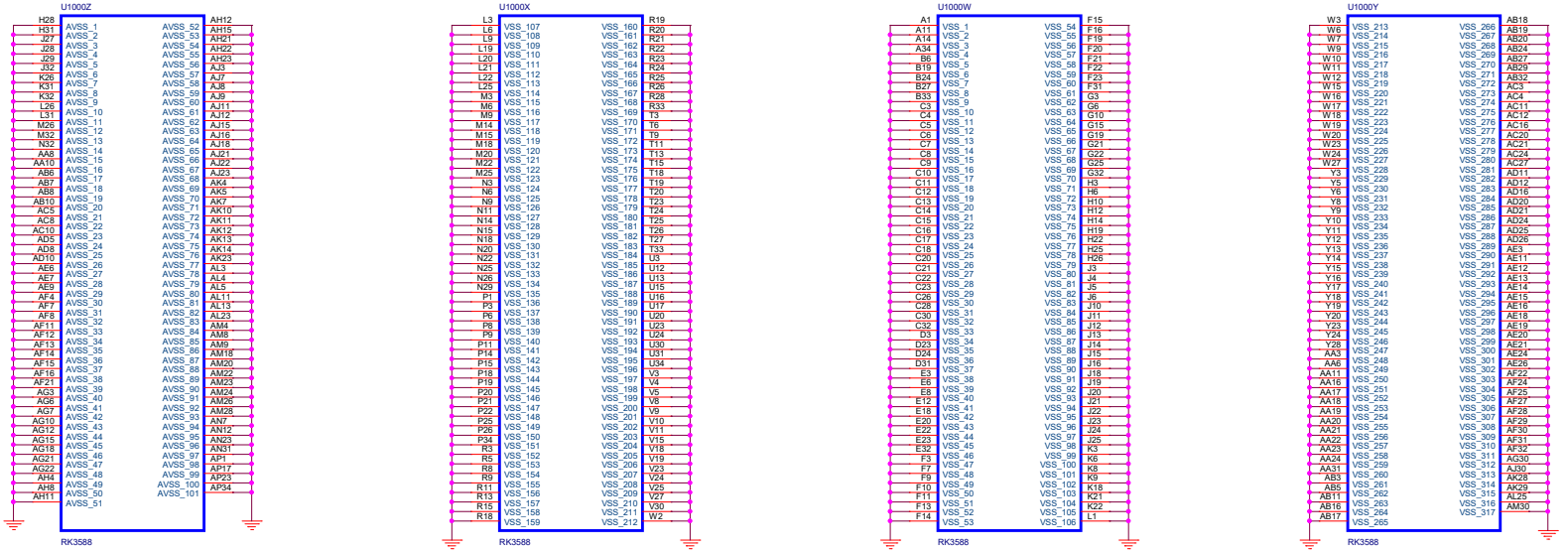
RK3588_V(POWER)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



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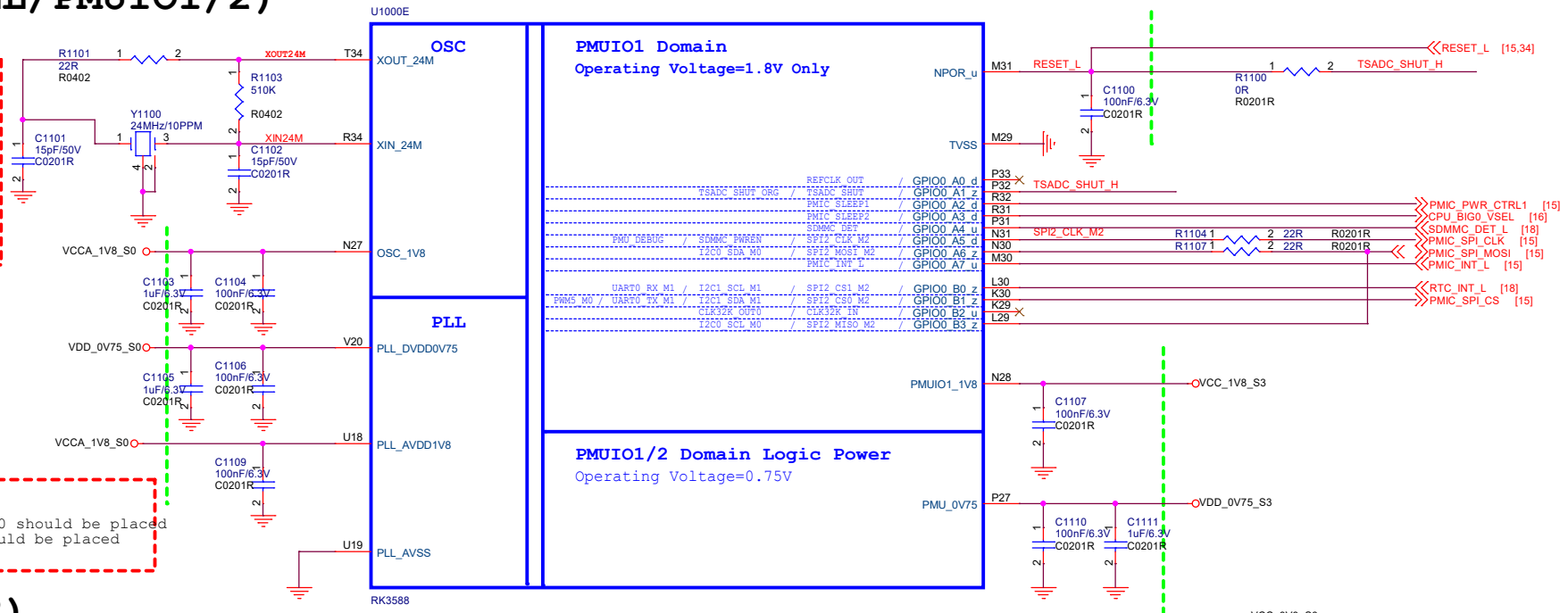
RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

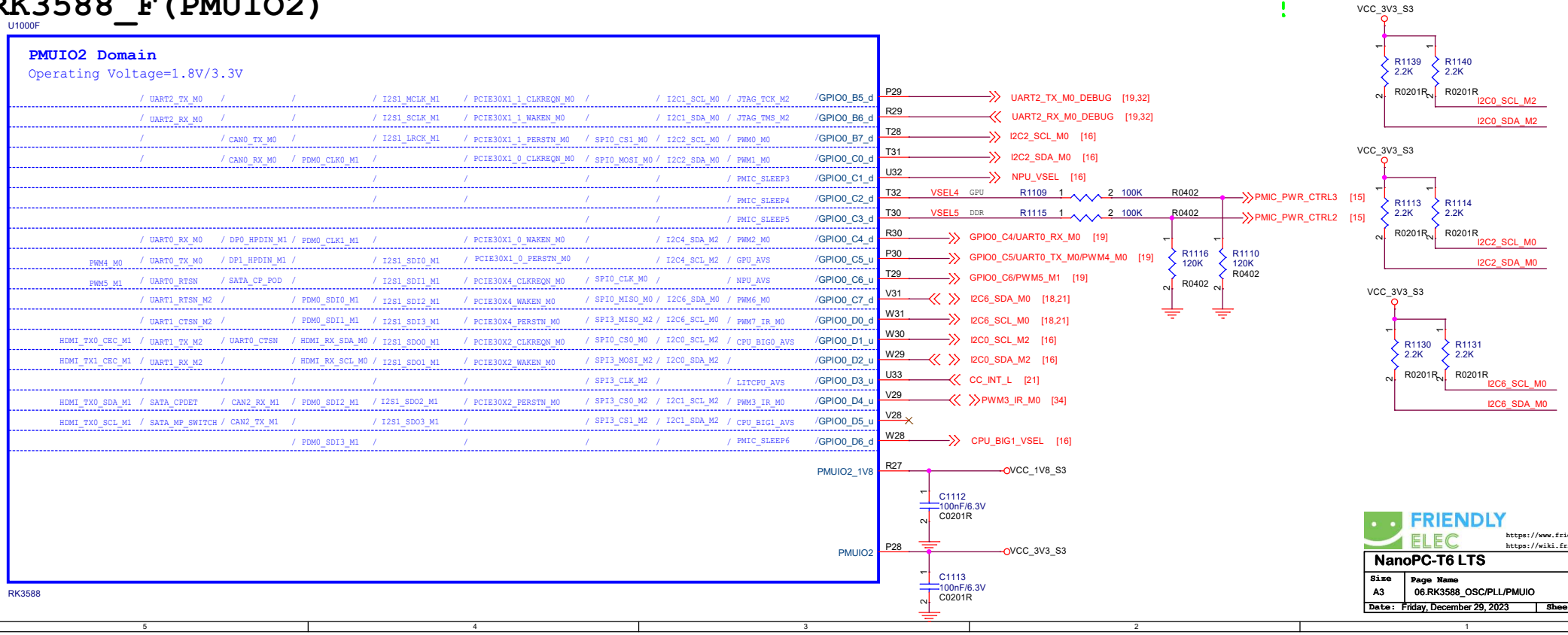
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588_F(PMUIO2)



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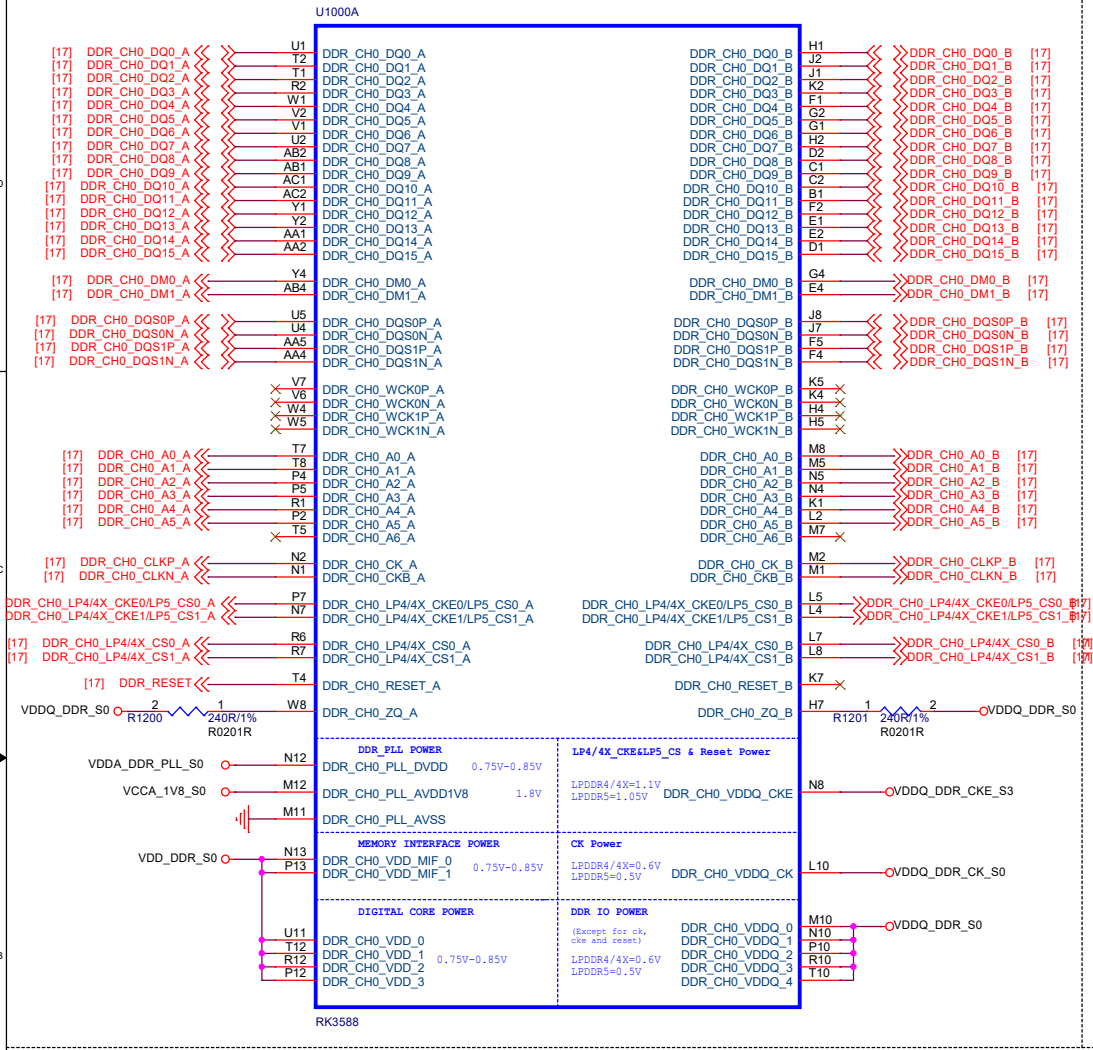
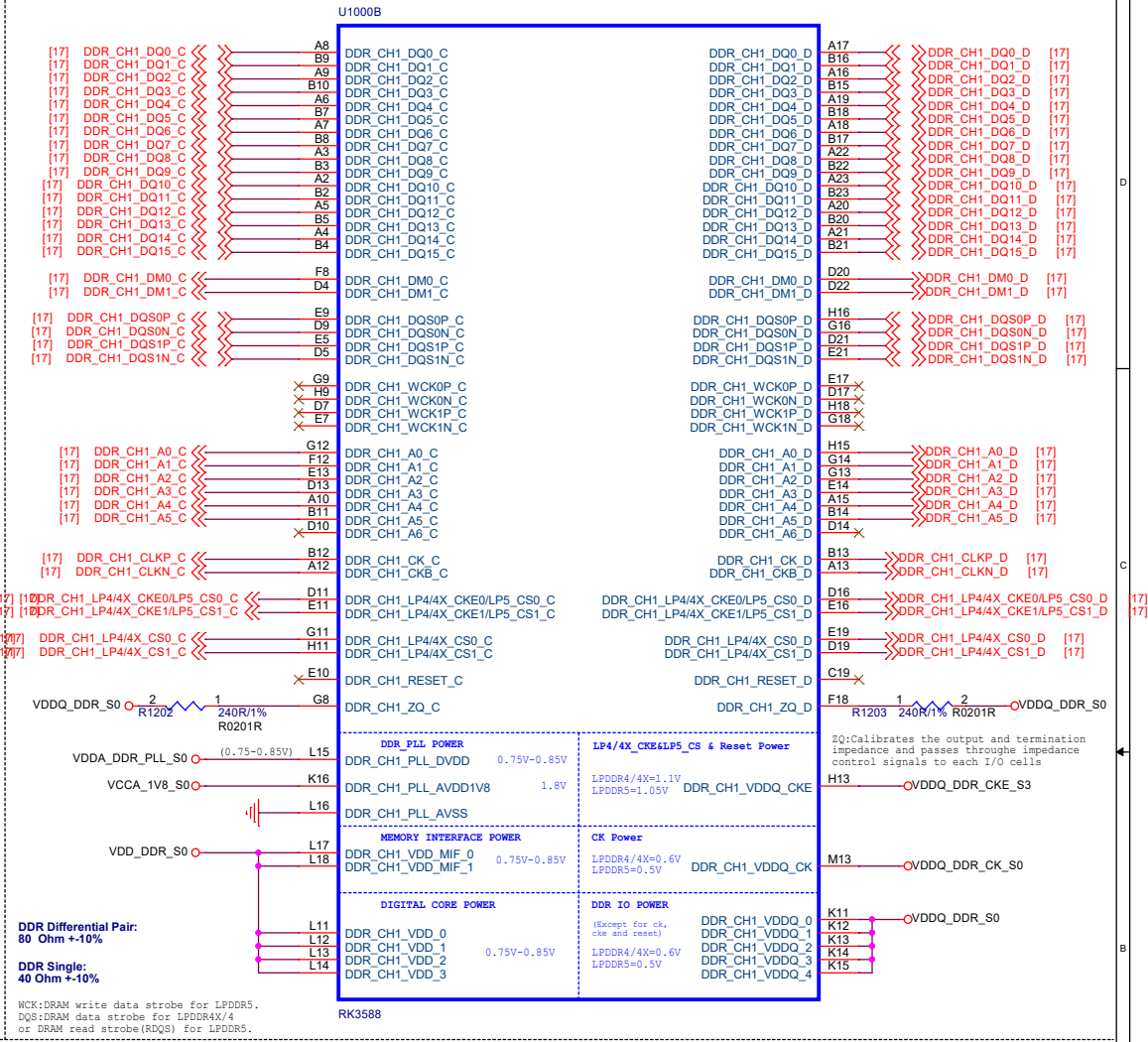
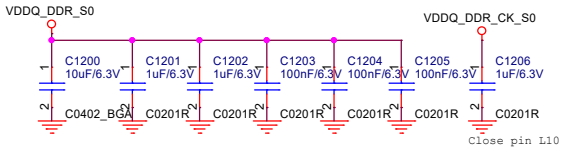




DDR FILTER



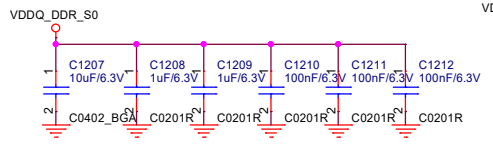
Hold power of CLK during retention times.

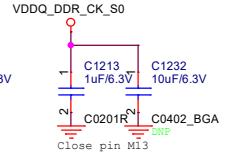
Sequence:
VDD-VDDQ_CKE-VDDQ

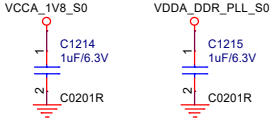
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET.
lpddr4X=1.1V/lpddr5=1.05V

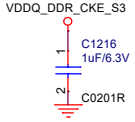
VDDQ_CK:power for CK.
LPDDR4/4X=0.6V/LPDDR5=0.5V

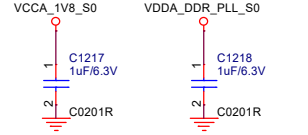
VDDQ:Power for DDR IO(except for ck, cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V

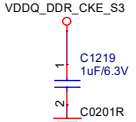


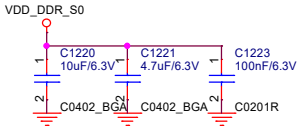


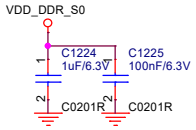


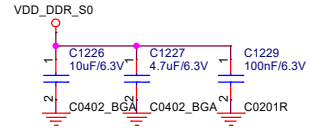


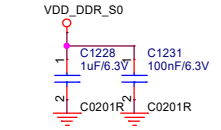












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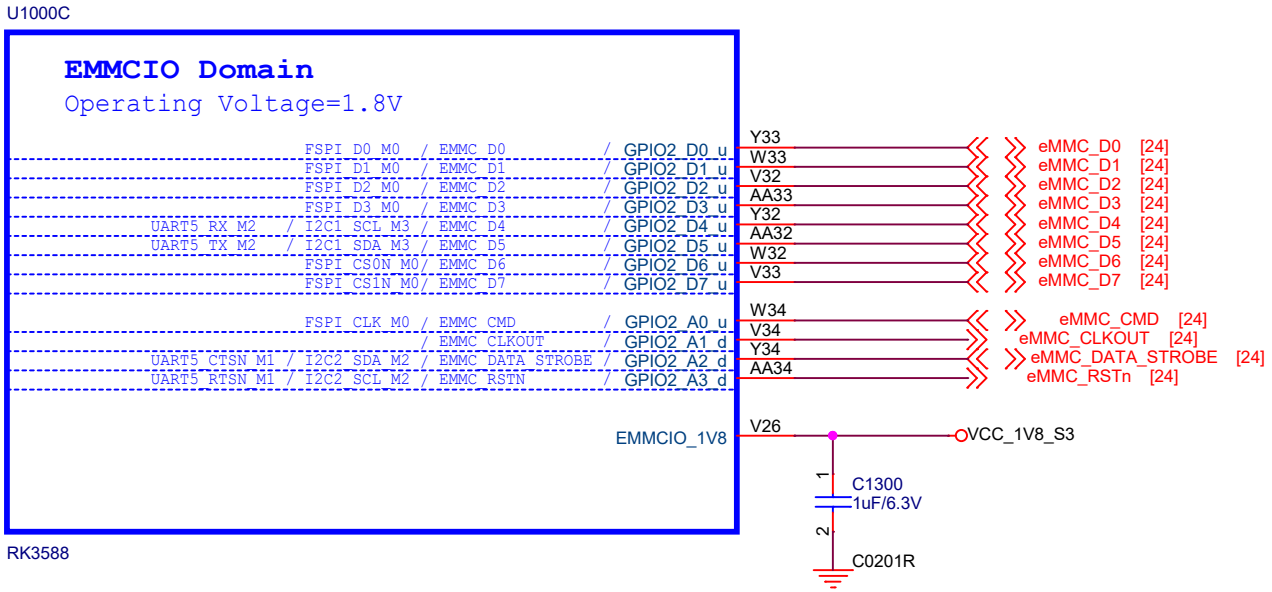
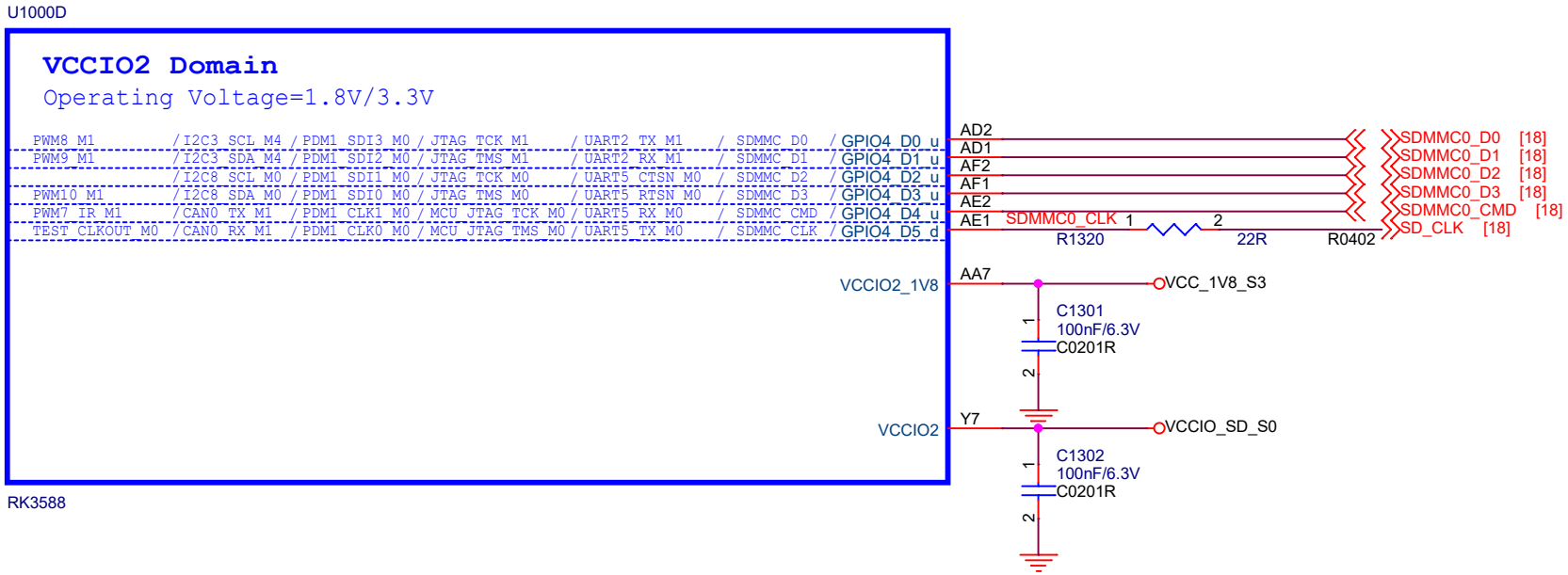
RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



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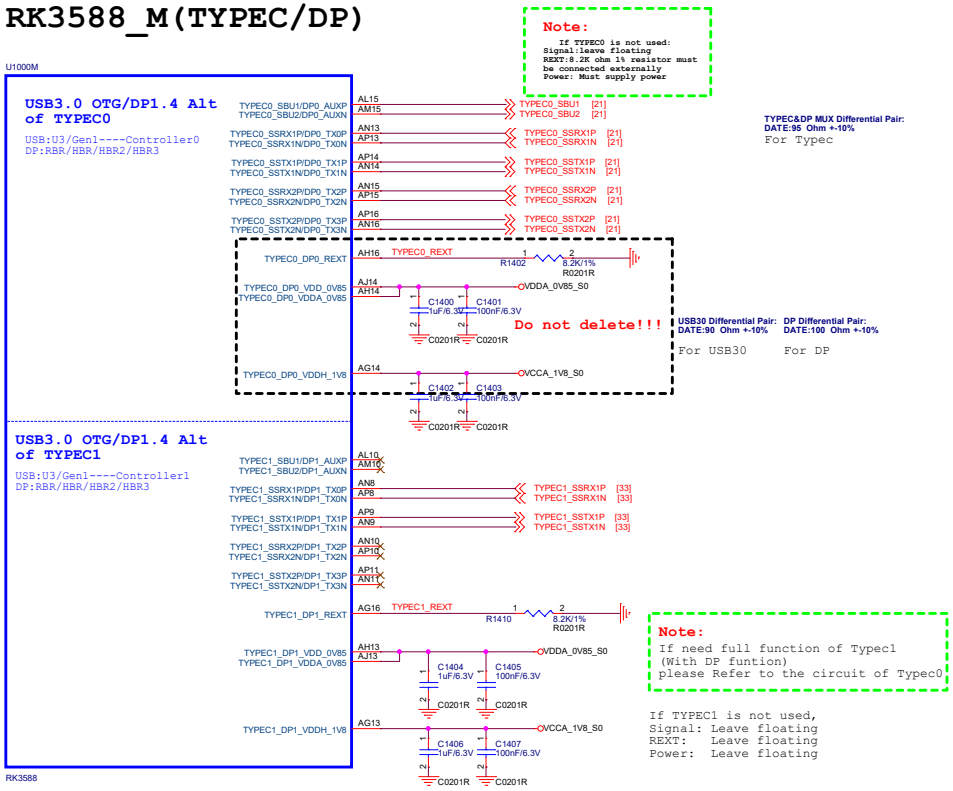
RK3588_M(TYPEC/DP)



Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

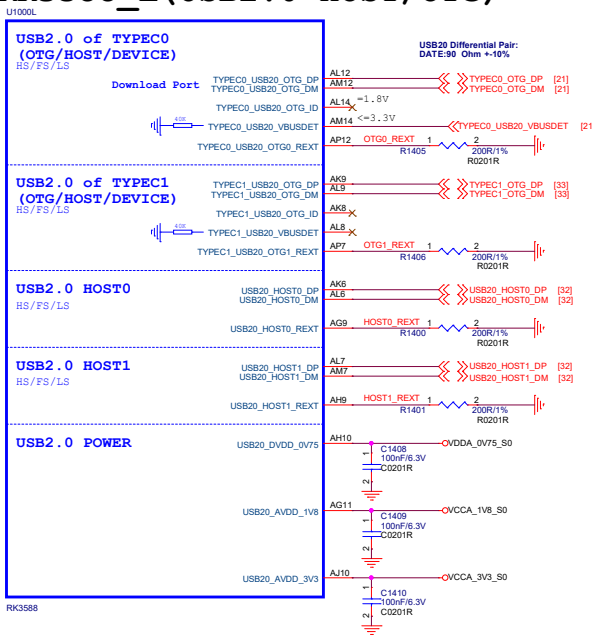
Note:
If need full function of Typec1
(With DP funtion)
please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

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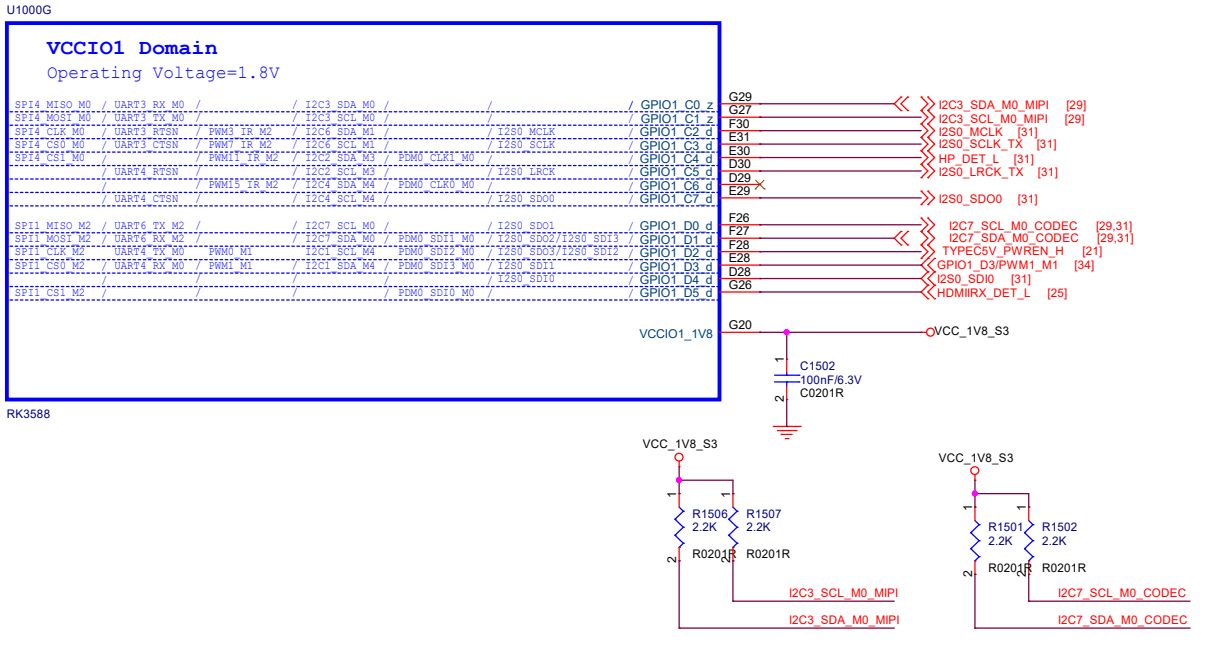
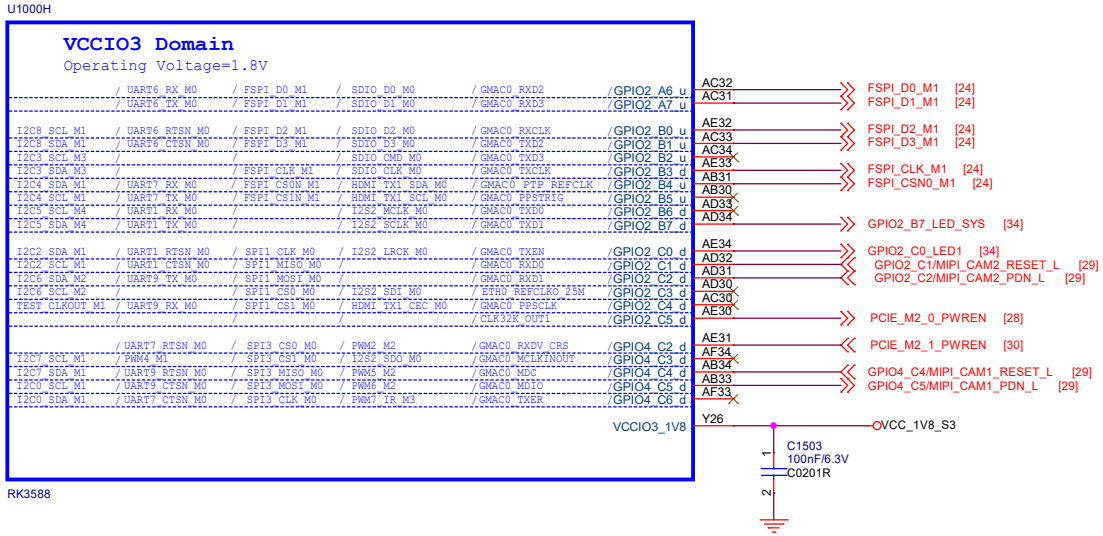
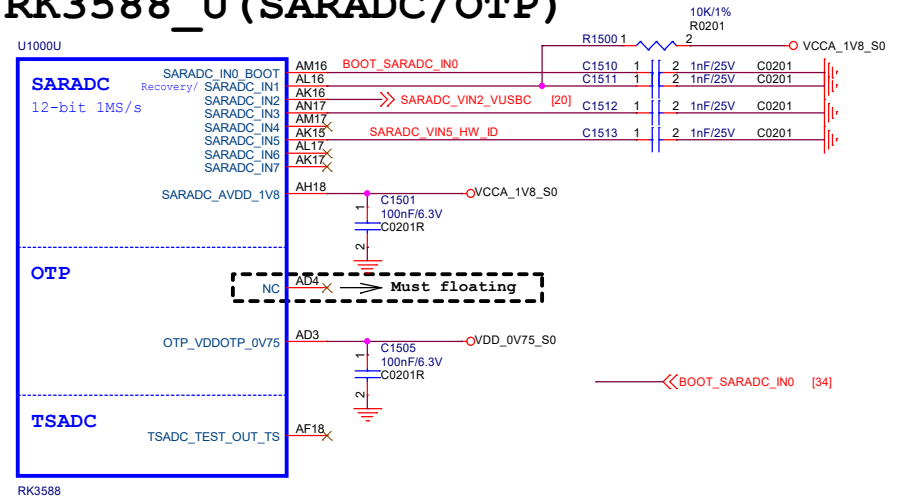
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

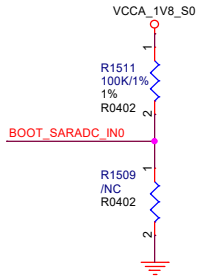
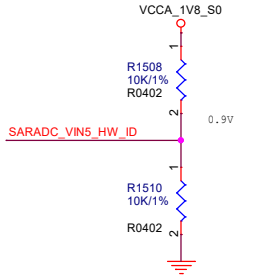


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG



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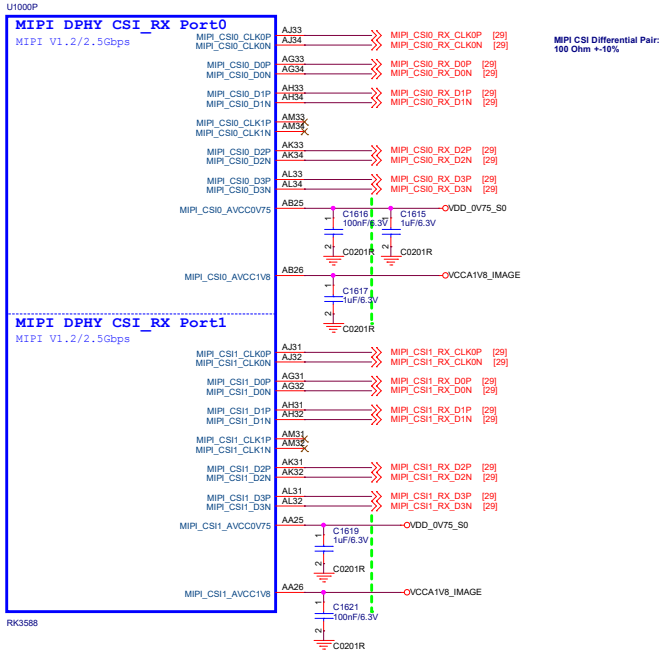
RK3588_Q/R(MIPI_D/C_PHY0/1)

RK3588_P(MIPI_DPHY_CSI_RX_PHY)



MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

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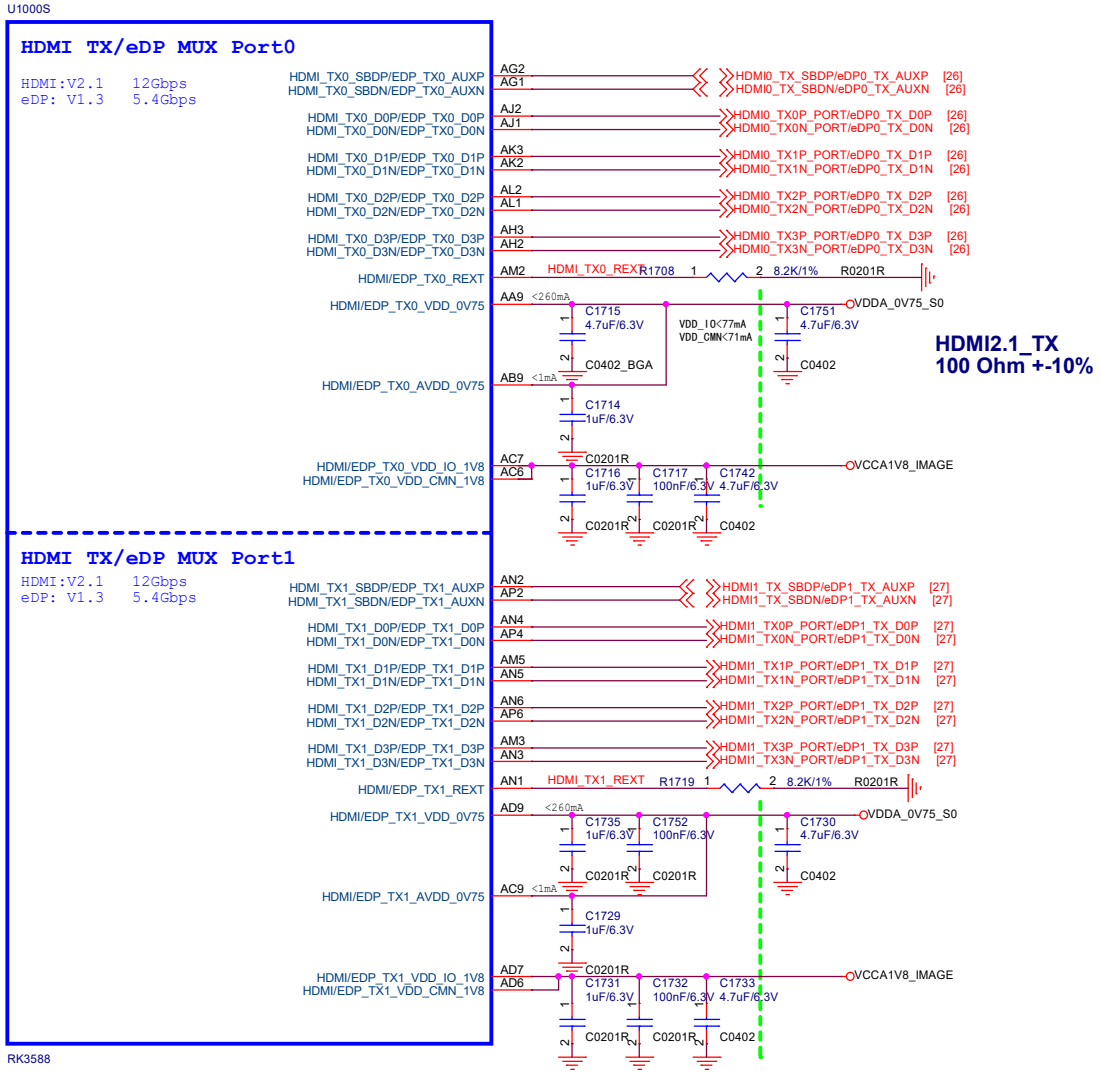
RK3588_S(HDMI2.1 TX)

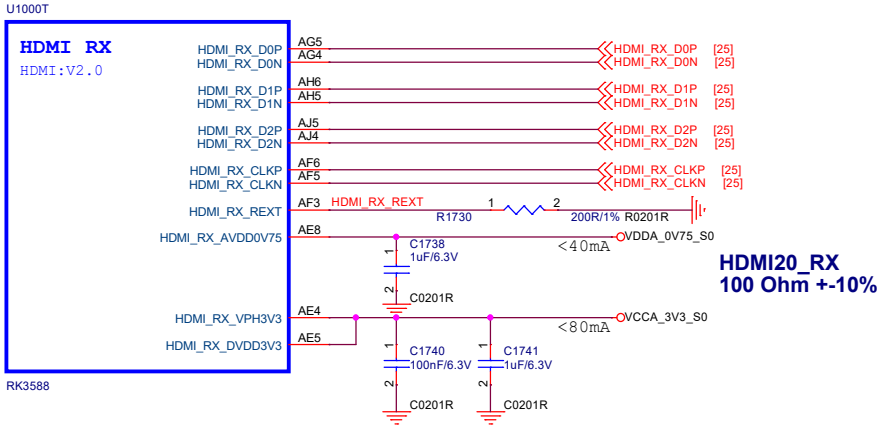
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

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RK3588_N(PCIE20)

Note:
If not used:
Signal:leave floating
Power: Floating

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN

L32 / L33 → PCIE20_0_REFCLKP [22] / PCIE20_0_REFCLKN [22]
M34 / M33 → PCIE20_0_TXP/SATA30_0_TXP [22] / PCIE20_0_TXN/SATA30_0_TXN [22]
N33 / N34 → PCIE20_0_RXP/SATA30_0_RXP [22] / PCIE20_0_RXN/SATA30_0_RXN [22]

PCIE20_SATA30_0_AVDD_0V85 — M28 — C1810 10uF/6.3V — C0402 — VDDA_0V85_S0
PCIE20_SATA30_0_AVDD_1V8 — M27 — C1808 1uF/6.3V — C0201R — VCCA_1V8_S0

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN

H32 / H33 → PCIE20_1_REFCLKP [23] / PCIE20_1_REFCLKN [23]
K33 / K34 → PCIE20_1_TXP/SATA30_1_TXP [23] / PCIE20_1_TXN/SATA30_1_TXN [23]
J33 / J34 → PCIE20_1_RXP/SATA30_1_RXP [23] / PCIE20_1_RXN/SATA30_1_RXN [23]

PCIE20_SATA30_1_AVDD_0V85 — L28 — C1818 100nF/6.3V — C0201R — VDDA_0V85_S0
PCIE20_SATA30_1_AVDD_1V8 — L27 — C1816 100nF/6.3V — C0201R — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN

G31 / G30 → PCIE20_2_REFCLKP [30] / PCIE20_2_REFCLKN [30]
H30 / H29 → PCIE20_2_TXP/SATA30_2_TXP [30] / PCIE20_2_TXN/SATA30_2_TXN [30]
J31 / J30 → PCIE20_2_RXP/SATA30_2_RXP [30] / PCIE20_2_RXN/SATA30_2_RXN [30]

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — C1806 1uF/6.3V — C0201R — VDDA_0V85_S0
PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — C1804 1uF/6.3V — C0201R — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN

Lane0: PCIE30_PORT0_TX0P/TX0N, PCIE30_PORT0_RX0P/RX0N
Lane1: PCIE30_PORT0_TX1P/TX1N, PCIE30_PORT0_RX1P/RX1N

E33 / E34 → PCIE30_PORT0_REFCLKP_IN [28] / PCIE30_PORT0_REFCLKN_IN [28]
D32 / D33 → PCIE30_PORT0_TX0P [28] / PCIE30_PORT0_TX0N [28]
G33 / G34 → PCIE30_PORT0_RX0P [28] / PCIE30_PORT0_RX0N [28]
C33 / C34 → PCIE30_PORT0_TX1P [28] / PCIE30_PORT0_TX1N [28]
F32 / F33 → PCIE30_PORT0_RX1P [28] / PCIE30_PORT0_RX1N [28]

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 1 2 200R/1% R0201R
PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C1802 1uF/6.3V — C0201R; C1803 4.7uF/6.3V — C0402

CLK Differential Pair:
100 Ohm ±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%

PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C1800 1uF/6.3V — C0201R; C1801 4.7uF/6.3V — C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN

Lane0: PCIE30_PORT1_TX0P/TX0N, PCIE30_PORT1_RX0P/RX0N
Lane1: PCIE30_PORT1_TX1P/TX1N, PCIE30_PORT1_RX1P/RX1N

A28 / B28 → PCIE30_PORT1_REFCLKP_IN [28] / PCIE30_PORT1_REFCLKN_IN [28]
B30 / A30 → PCIE30_PORT1_TX2P [28] / PCIE30_PORT1_TX2N [28]
B32 / A32 → PCIE30_PORT1_RX2P [28] / PCIE30_PORT1_RX2N [28]
C29 / B29 → PCIE30_PORT1_TX3P [28] / PCIE30_PORT1_TX3N [28]
C31 / B31 → PCIE30_PORT1_RX3P [28] / PCIE30_PORT1_RX3N [28]

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 1 2 200R/1% R0201R
PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C1814 1uF/6.3V — C0201R; C1815 4.7uF/6.3V — C0402

PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C1812 100nF/6.3V — C0201R; C1813 4.7uF/6.3V — C0402

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Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1	I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PMIC_SLEEP_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PMIC_SLEEP_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u
PMIC_SLEEP_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d
PMIC_SLEEP_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PMIC_SLEEP_M2	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u
PMIC_SLEEP_M3	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PMIC_SLEEP_M4		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PMIC_SLEEP_M5	IR_M0	UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PMIC_SLEEP_M6	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PMIC_SLEEP_M7	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PMIC_SLEEP_M8	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d
PMIC_SLEEP_M9	IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	GPIO3_A0/SPI4_MISO_M1/PWM10_M0 [19]	GPIO3_A0_u
AA30	GPIO3_A1/SPI4_MOSI_M1 [19]	GPIO3_A1_u
AD27	GPIO3_A2/SPI4_CLK_M1/UART8_TX_M1 [19]	GPIO3_A2_u
AE27	GPIO3_A3/SPI4_CS0_M1/UART8_RX_M1 [19]	GPIO3_A3_u
AD28	GPIO3_A4/SPI4_CS1_M1 [19]	GPIO3_A4_d
AH30		GPIO3_A5_d
AH27	GPIO3_A6/LCD_RST [29]	GPIO3_A6_d
AG29		GPIO3_A7_u
AG28	GPIO3_B0/PWM9_M0 [19]	GPIO3_B0_u
AH29	GPIO3_B1/PWM2_M1//LCD_BL [29]	GPIO3_B1_d
AE28	GPIO3_B2 [19]	GPIO3_B2_d
AC28	GPIO3_B3 [19]	GPIO3_B3_u
AC29	GPIO3_B4 [19]	GPIO3_B4_u
AD29	GPIO3_B5/UART3_TX_M1/PWM12_M0 [19]	GPIO3_B5_u
AE29	GPIO3_B6/UART3_RX_M1/PWM13_M0 [19]	GPIO3_B6_d
AA28	GPIO3_B7 [19]	GPIO3_B7_d
Y29	GPIO3_C0/TP_INT_L [29]	GPIO3_C0_d
Y27	TP_RST_L [29]	GPIO3_C1_d
Y31	GPIO3_C2/PWM14_M0 [19]	GPIO3_C2_d
Y30	GPIO3_C3/PWM15_IR_M0 [19]	GPIO3_C3_d
AH26	HDMITX1_CEC_M2 [27]	GPIO3_C4_u
AH25	HDMITX1_SDA_M1 [27]	GPIO3_C5_u
AG26	HDMITX1_SCL_M1 [27]	GPIO3_C6_u
AJ24	I2C5_SCL_M0_TP [29]	GPIO3_C7_u
AH24	I2C5_SDA_M0_TP [29]	GPIO3_D0_u
AG23	HDMI_RX_CEC [25]	GPIO3_D1_d
AG25	HDMI_RX_SCL_M1 [25]	GPIO3_D2_d
AG24	HDMI_RX_SDA_M1 [25]	GPIO3_D3_d
AA27	HDMIIRX_HPDOUT_H [25]	GPIO3_D4_d
AB28	GPIO3_D5/PWM11_M3/LCD_2_BL [29]	GPIO3_D5_d

VCCIO5_1V8 — W25 — C1903 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO5 — W26 — C1902 100nF/6.3V C0201R — OVCC_3V3_S3

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VCC_3V3_S3 — R10064 2.2K R0201R — R10065 2.2K R0201R — I2C4_SDA_M3_TP — I2C4_SCL_M3_TP

VCC_3V3_S3 — R3820 2.2K R0201R — R3821 2.2K R0201R — I2C5_SDA_M0_TP — I2C5_SCL_M0_TP

VCC_3V3_S3 — R10119 2.2K R0201R — R10120 2.2K R0201R — I2C8_SCL_M2 — I2C8_SDA_M2

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1		I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1		I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1			I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2			PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2	I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2	I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2	I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3	I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA5_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1		I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

AK30	GPIO4_A0/TP_2_INT_L [29]	GPIO4_A0_d
AL30	TP_2_RST_L [29]	GPIO4_A1_d
AM29	PCIE_WIFI_PERSTn [30]	GPIO4_A2_d
AL29	LCD_2_BL_EN_H [29]	GPIO4_A3_d
AL28	PCIE_2SGLAN_PERSTB [22]	GPIO4_A4_d
AK27	SDMMC_PWREN [18]	GPIO4_A5_d
AL27	TYPEC0_SBU1_DC [21]	GPIO4_A6_d
AM27	TYPEC0_SBU2_DC [21]	GPIO4_A7_d
AK26	USB30_HOST_PWREN_H [33]	GPIO4_B0_d
AL24	HDMI0_TX_ON_H [26]	GPIO4_B1_u
AK25	HDMI1_TX_ON_H [27]	GPIO4_B2_u
AM25	PCIE_2SGLAN_PERSTB_B [23]	GPIO4_B3_u
AL26	PCIE30X4_CLKREQn_M1_L [28]	GPIO4_B4_u
AJ26	PCIe_WIFI_DISABLEn [30]	GPIO4_B5_d
AJ27	PCIE30X4_PERSTn_M1_L [28]	GPIO4_B6_d
AJ28	HDMITX0_SCL_M0 [26]	GPIO4_B7_u
AJ25	HDMITX0_SDA_M0 [26]	GPIO4_C0_u
AK24	HDMITX0_CEC_M0 [26]	GPIO4_C1_d

VCCIO6_1V8 — AC25 — C1909 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO6 — AC26 — C1908 100nF/6.3V C0201R — OVCC_3V3_S3

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RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2	I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2	I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
	PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2	I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
		SPI2_MISO_M0		HDMI_TX1_SCL_M2			GPIO1_A4_d
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0			GPIO1_A5_d
		SPI2_CLK_M0		HDMI_TX1_HPD_M0			GPIO1_A6_d
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2		PDM1_SDI0_M1		GPIO1_A7_u
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3		PDM1_SDI1_M1		GPIO1_B0_u
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3		PDM1_SDI2_M1		GPIO1_B1_d
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3		PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2		PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2		PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2			UART7_TX_M2	GPIO1_B5_u
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0	I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
	HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M0	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
	HDMI_RX_SDA_M2	PWM15_IR_M3		PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

A24	GPIO1_A0/UART6_RX_M1 [19]	GPIO1_A0_d
A25	GPIO1_A1/UART6_TX_M1 [19]	GPIO1_A1_d
A26	I2C4_SDA_M3_TP [29]	GPIO1_A2_d
A27	I2C4_SCL_M3_TP [29]	GPIO1_A3_d
B25	USB20_HOST_PWREN_H [32]	GPIO1_A4_d
B26	HDMITX0_HPDIN_M0 [26]	GPIO1_A5_d
C24	HDMITX1_HPDIN_M0 [27]	GPIO1_A6_d
C25	GPIO1_A7 [19]	GPIO1_A7_u
C27	GPIO1_B0 [19]	GPIO1_B0_u
D25	GPIO1_B1/SPI0_MISO_M2 [19]	GPIO1_B1_d
D26	GPIO1_B2/SPI0_MOSI_M2/UART4_RX_M2 [19]	GPIO1_B2_d
D27	GPIO1_B3/SPI0_CLK_M2/UART4_TX_M2 [19]	GPIO1_B3_d
E24	GPIO1_B4/SPI0_CS0_M2/UART7_RX_M2 [19]	GPIO1_B4_u
E25	GPIO1_B5/SPI0_CS1_M0/UART7_TX_M2 [19]	GPIO1_B5_u
E26	MIPI_CAM1_CLKOUT [29]	GPIO1_B6_u
E27	MIPI_CAM2_CLKOUT [29]	GPIO1_B7_u
F24	I2C8_SCL_M2 [19]	GPIO1_D6_u
F25	I2C8_SDA_M2 [19]	GPIO1_D7_u

VCCIO4_1V8 — H20 — C1907 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO4 — H21 — C9951 100nF/6.3V C0201R — OVCC_3V3_S3

RK3588

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Size A2	Page Name 14.RK3588_1.8V/ 3.3V GPIO		
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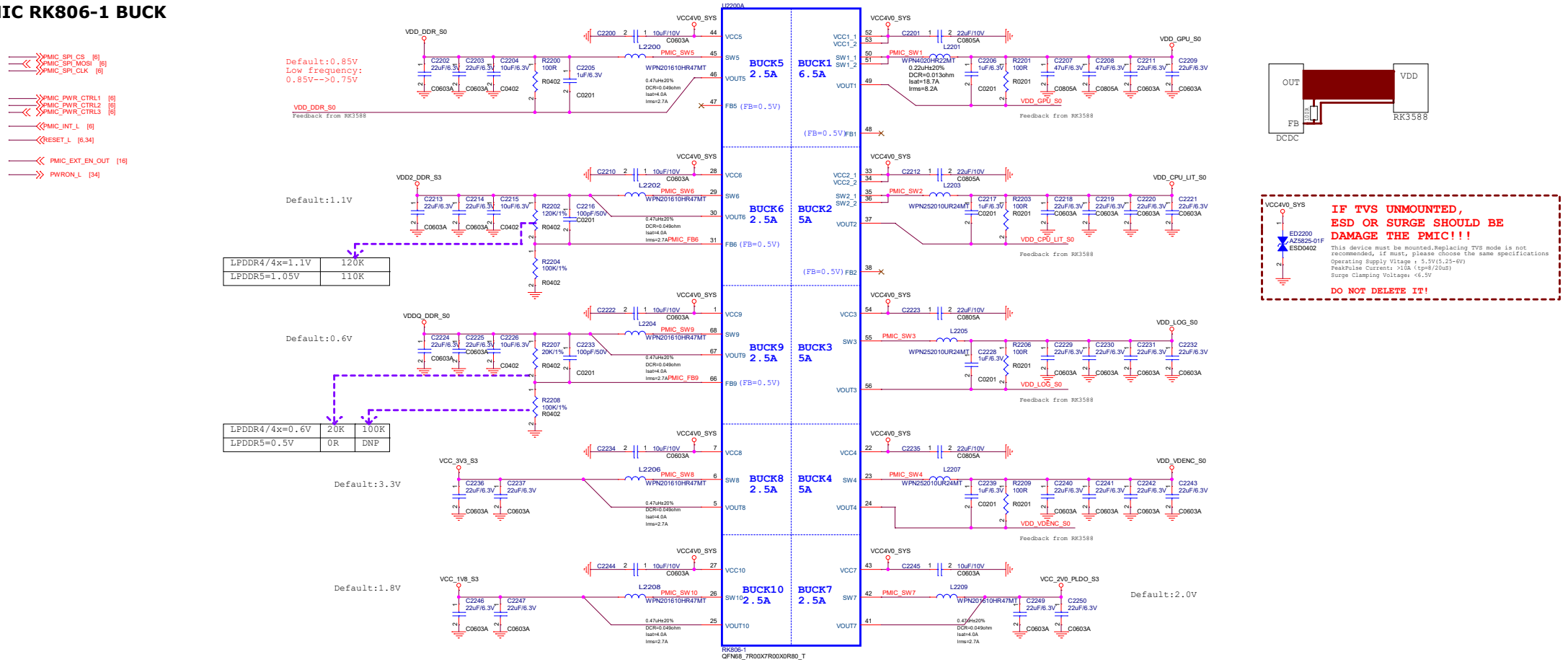
PMIC RK806-1 BUCK



VCC4V0_SYS

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

ED2200 AZ5825-01F ESD0402

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications

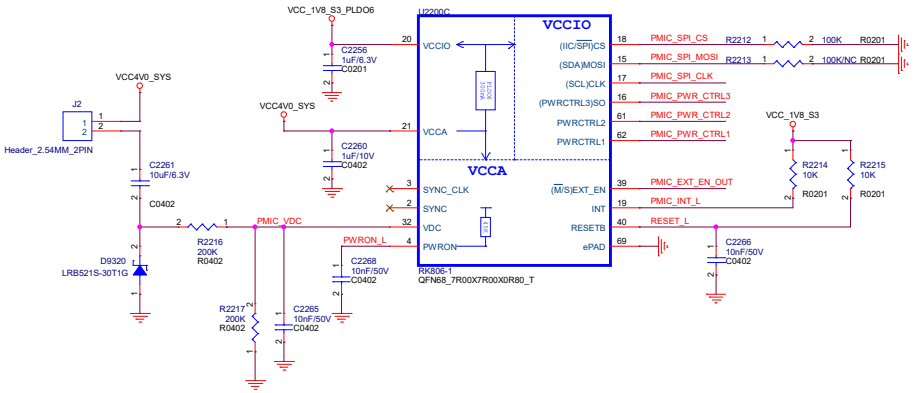
Operating Supply Vltage : 5.5V(5.25-6V)

PeakPulse Current: >10A (tp=8/20uS)

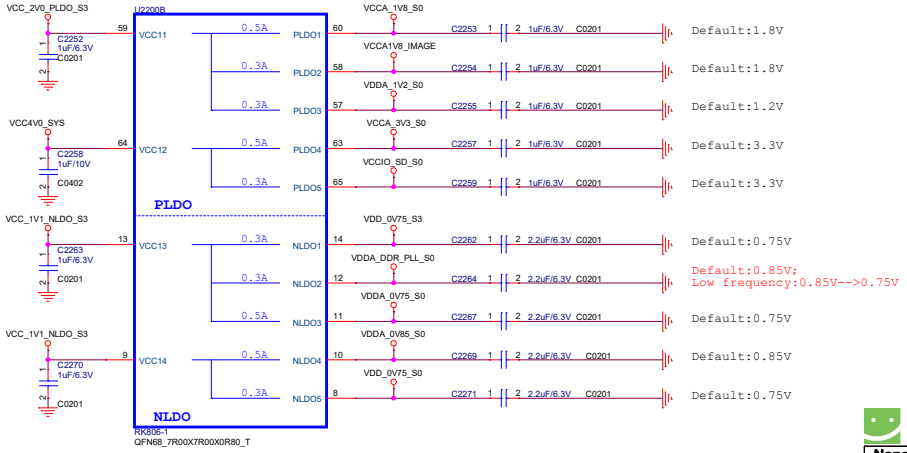
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

PMIC RK806-1 Managerment



PMIC RK806-1 LDO



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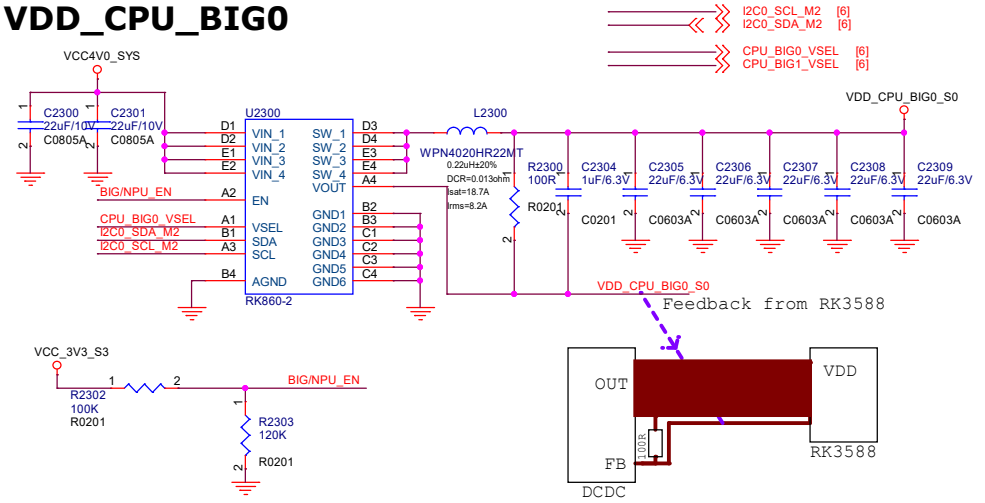
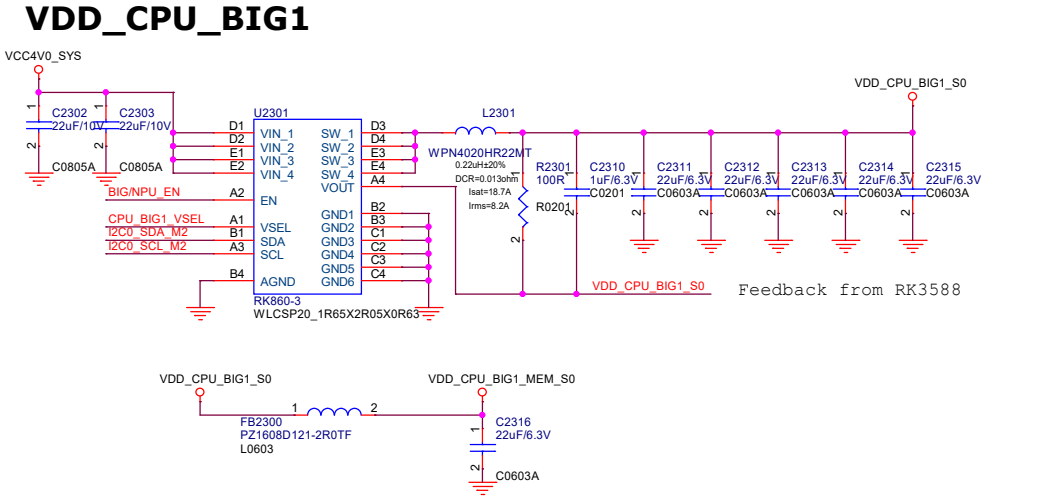
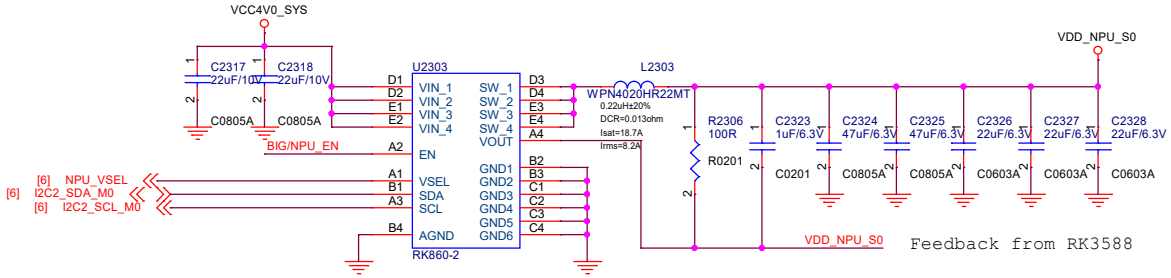
VDD_CPU_BIG0



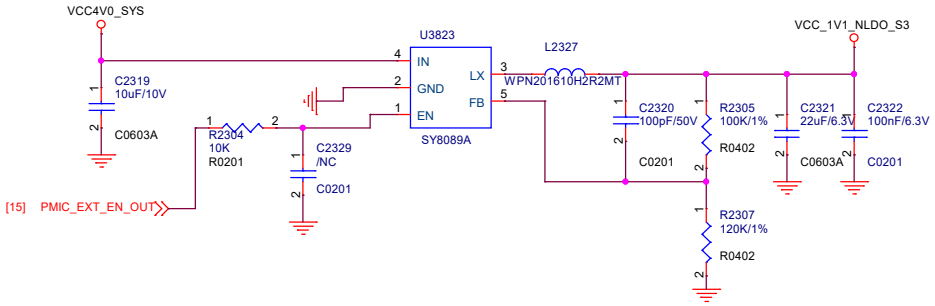
VDD_CPU_BIG1



VDD_NPU



VCC_1V1_NLDO_S3



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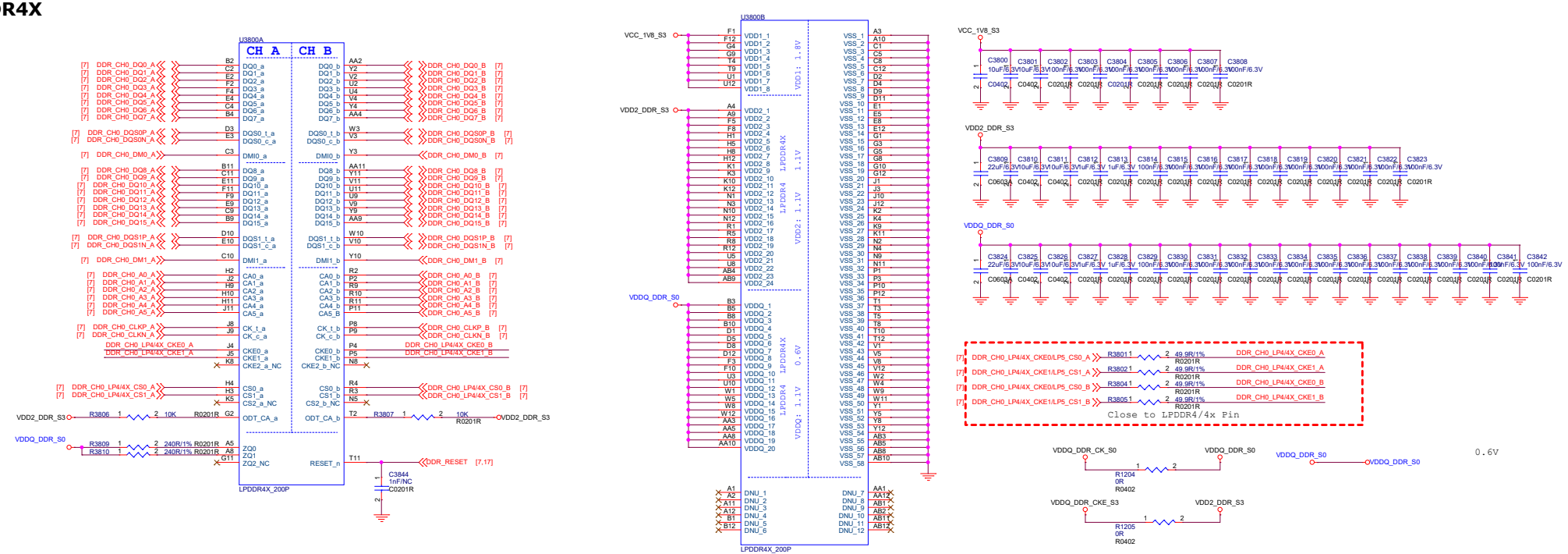
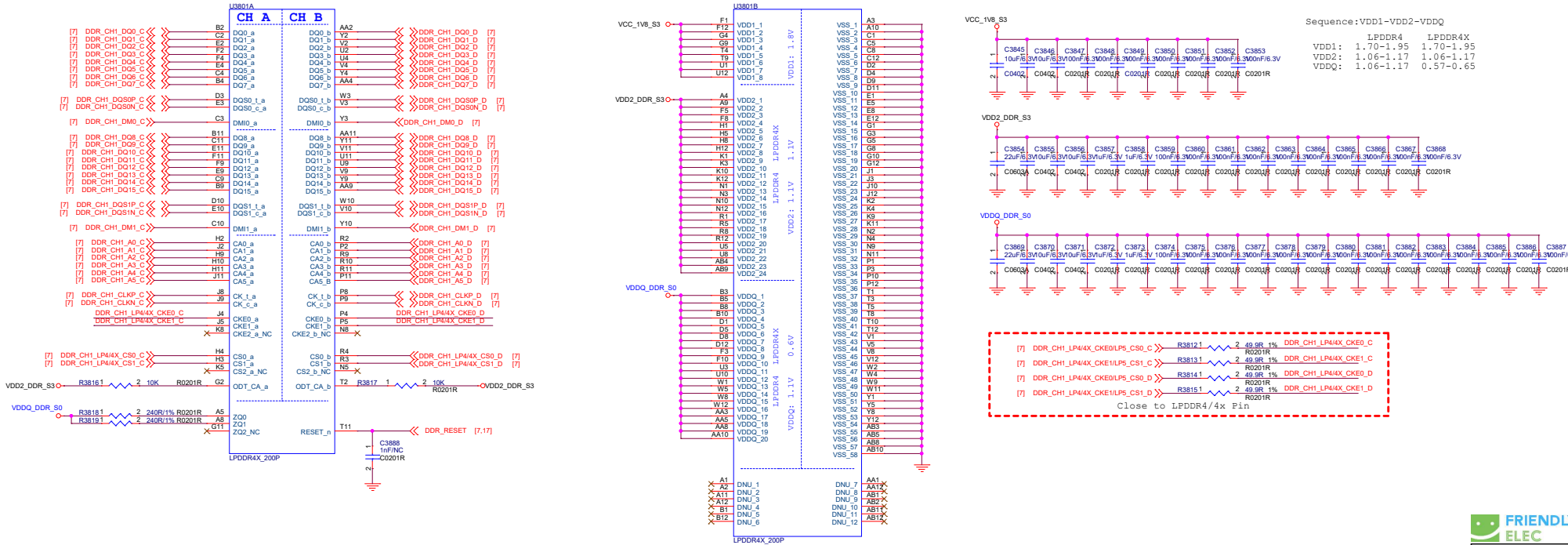
LPDDR4X





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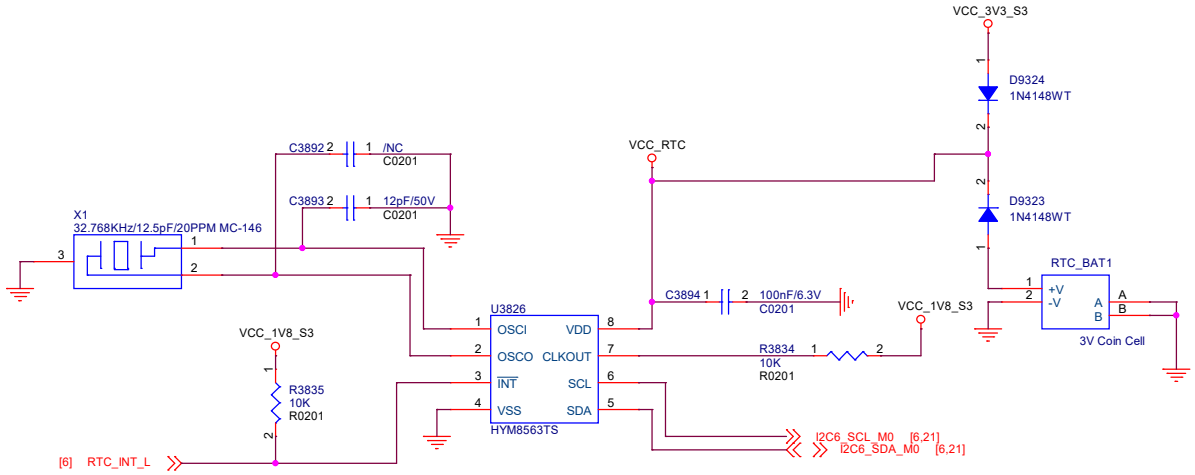
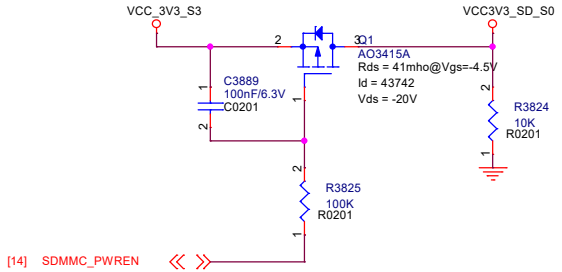
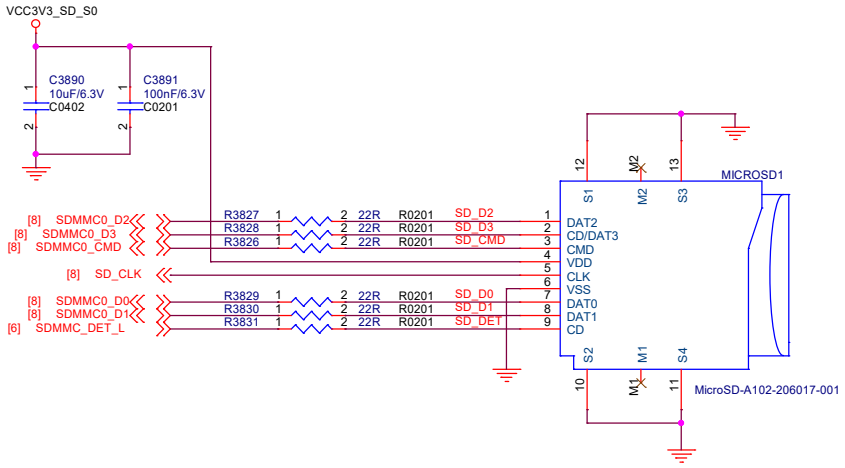
RTC

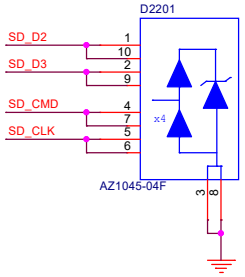


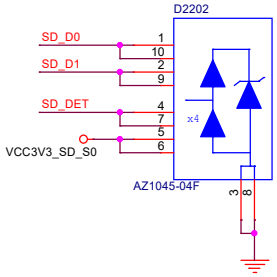
Address:Read A3H, Write A2H
7bit address: 0x51

microSD









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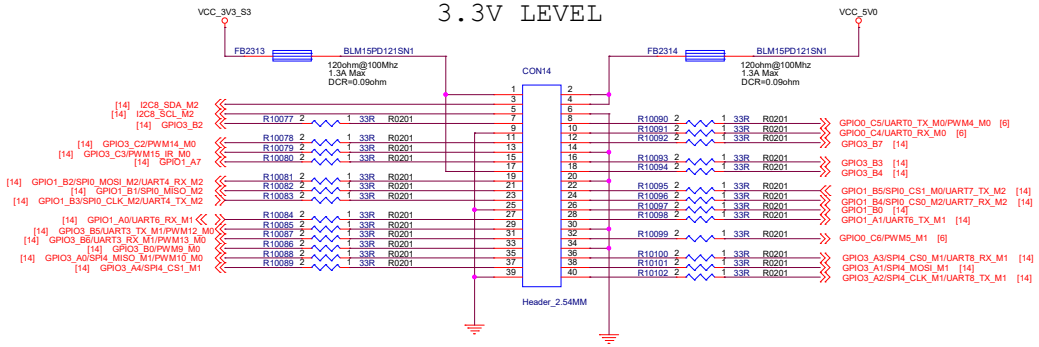
GPIO



UART0	3.3V	GPIO	UART9	/	NC
UART1	/	NC			
UART2	3.3V	Debug Console			
UART3	3.3V	GPIO			
UART4	3.3V	GPIO			
UART5	/	NC			
UART6	3.3V	GPIO			
UART7	3.3V	GPIO			
UART8	3.3V	GPIO			

SPI0	3.3V	GPIO
SPI1	/	NC
SPI2	/	NC
SPI3	/	NC
SPI4	3.3V	GPIO

I2S0	1.8V	ALC5616 Codec
I2S1	/	NC
I2S2	3.3V	GPIO
I2S3	3.3V	GPIO

I2C0	3.3V	RK860-3(CPU0),RK860-2(CPU1)
I2C1	/	NC
I2C2	3.3V	RK860-2(NPU)
I2C3	1.8V	MIPI CSI 1
I2C4	3.3V	MIPI DSI 2 Touch
I2C5	3.3V	MIPI DSI 1 Touch
I2C6	3.3V	24AA025E48T-I/OT, HYM8563TS, FUSB302MPX
I2C7	1.8V	Codec, MIPI CSI 2
I2C8	3.3V	GPIO

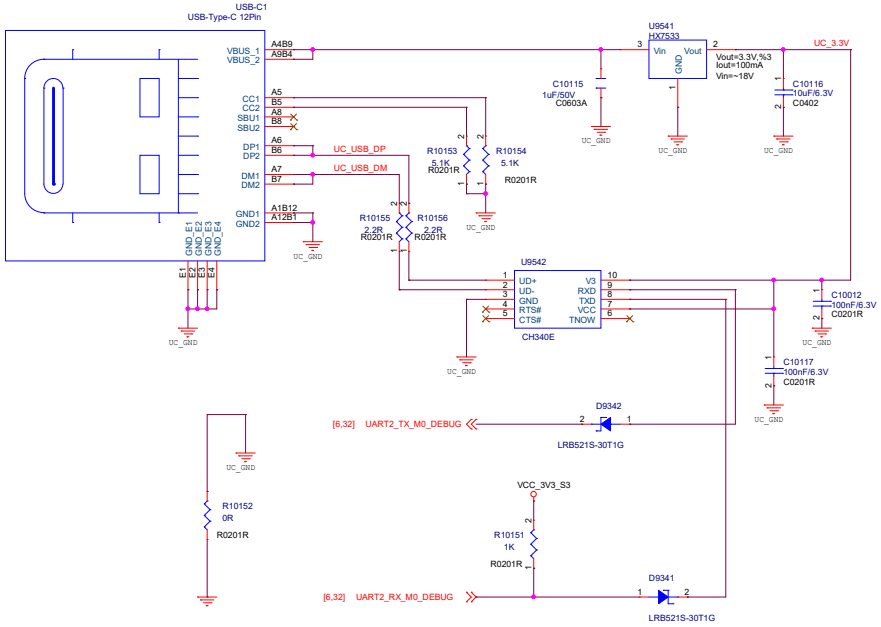
CAN0	/	NC
CAN1	3.3V	GPIO
CAN2	/	NC

SPDIF0	/	NC
SPDIF1	/	NC

SDIO	/	NC

PWM0	/	NC	PWM9	3.3V	GPIO
PWM1	1.8V	FAN	PWM10	3.3V	GPIO
PWM2	3.3V	LCD BL PWM	PWM11	3.3V	LCD2 BL PWM
PWM3	3.3V	IR	PWM12	3.3V	GPIO
PWM4	3.3V	GPIO	PWM13	3.3V	GPIO
PWM5	3.3V	GPIO	PWM14	3.3V	GPIO
PWM6	/	NC	PWM15	3.3V	GPIO
PWM7	/	NC			
PWM8	/	NC			

Debug UART



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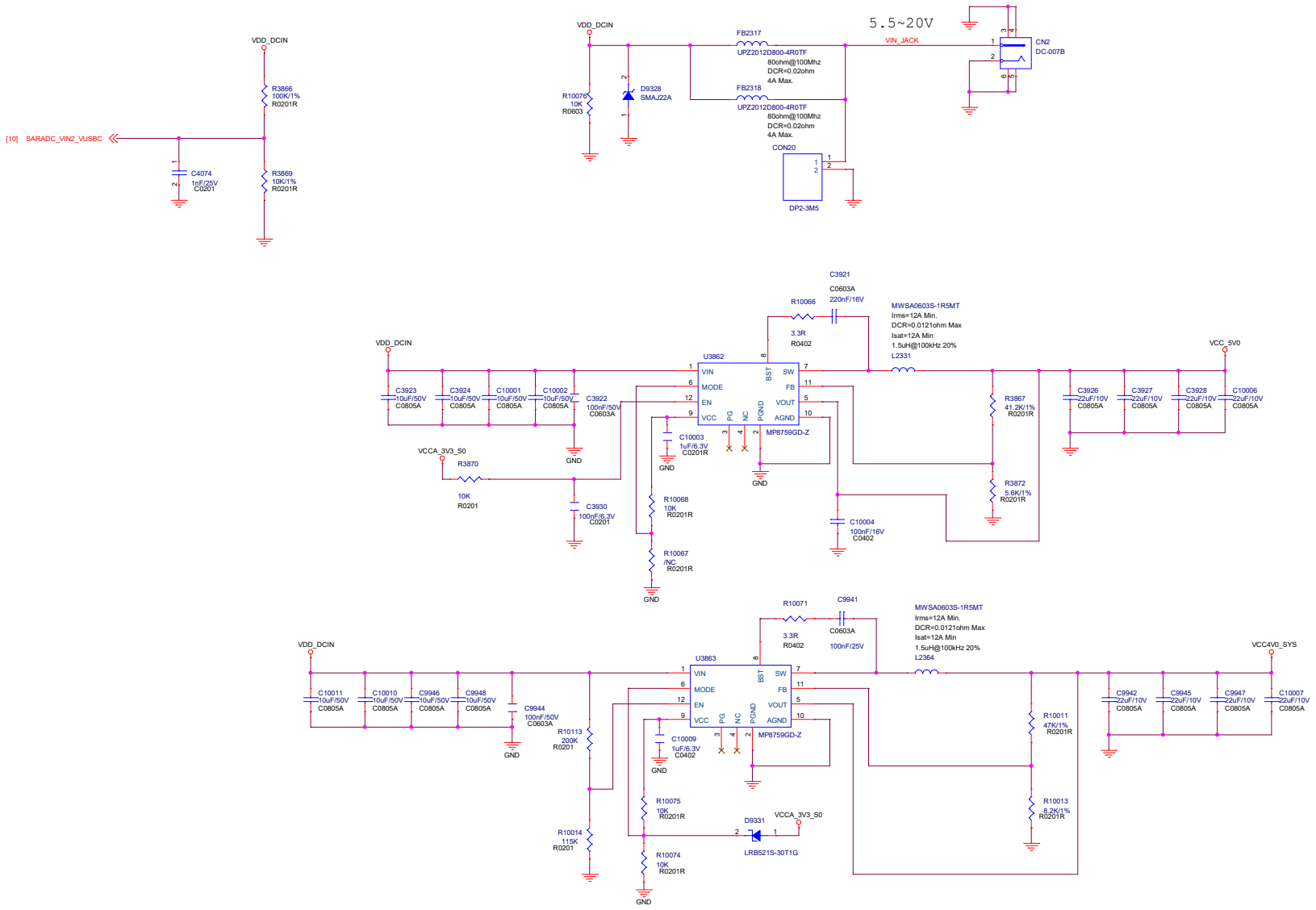
Power IN



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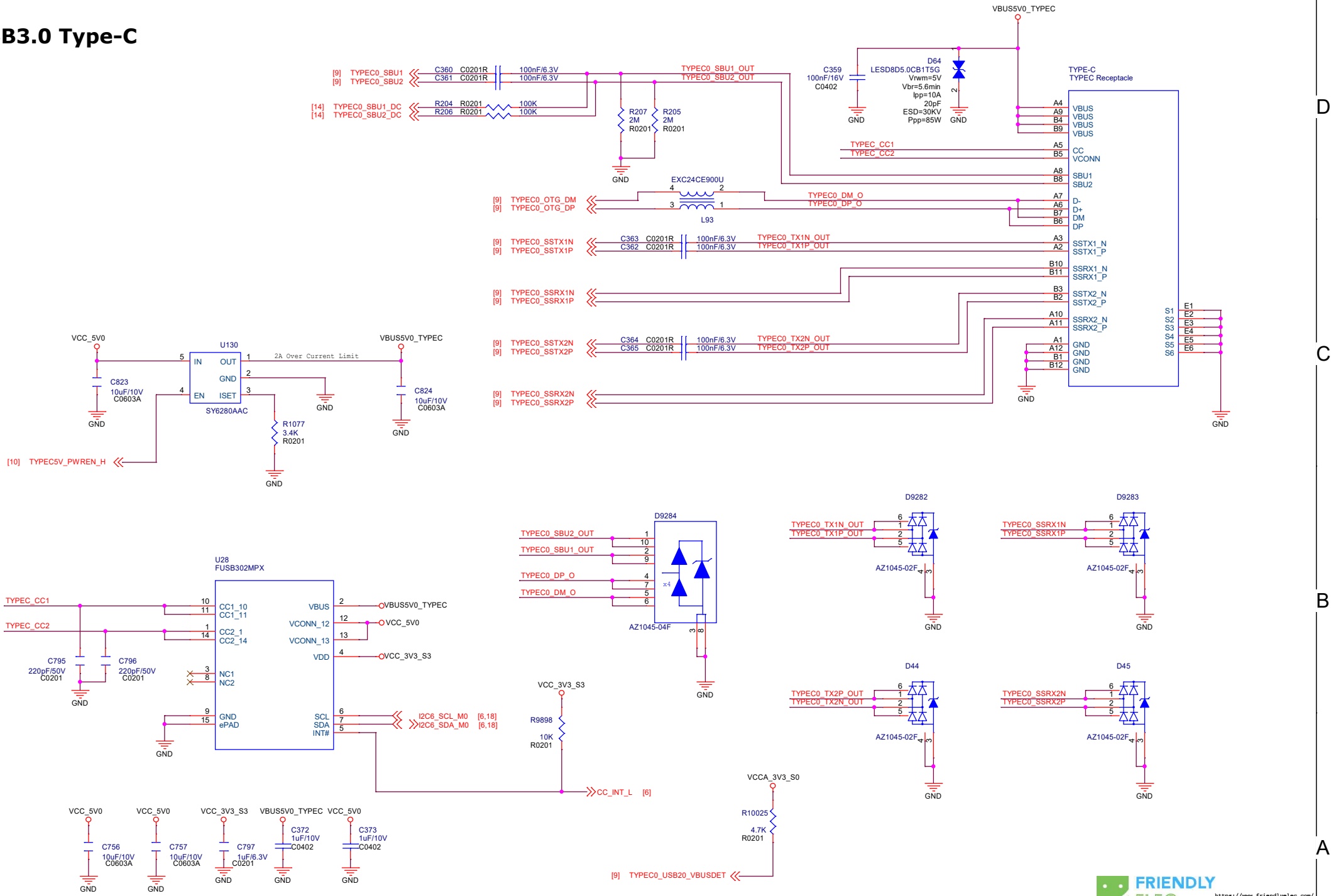
USB3.0 Type-C



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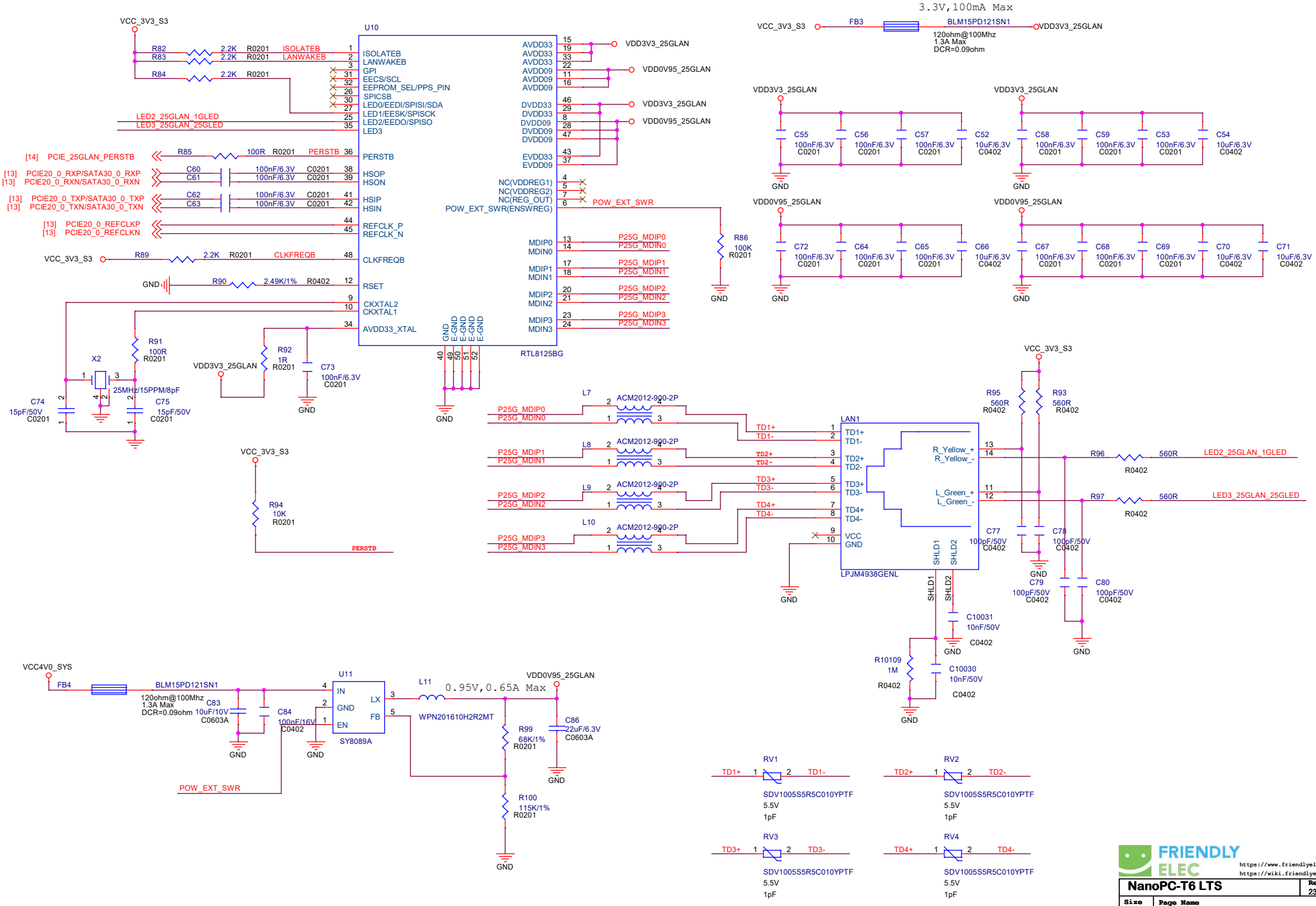
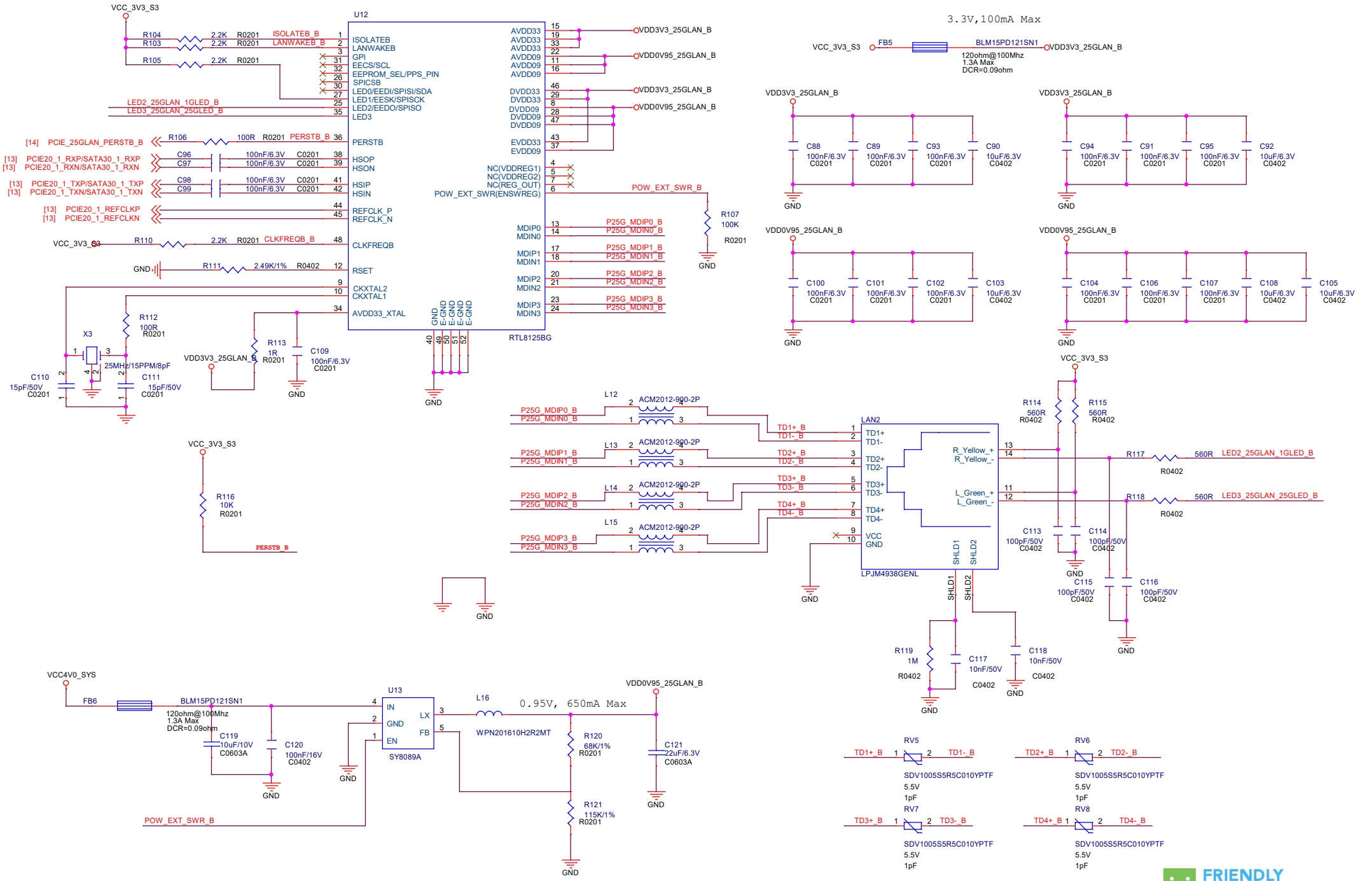
2.5G Ethernet A



2.5G Ethernet B



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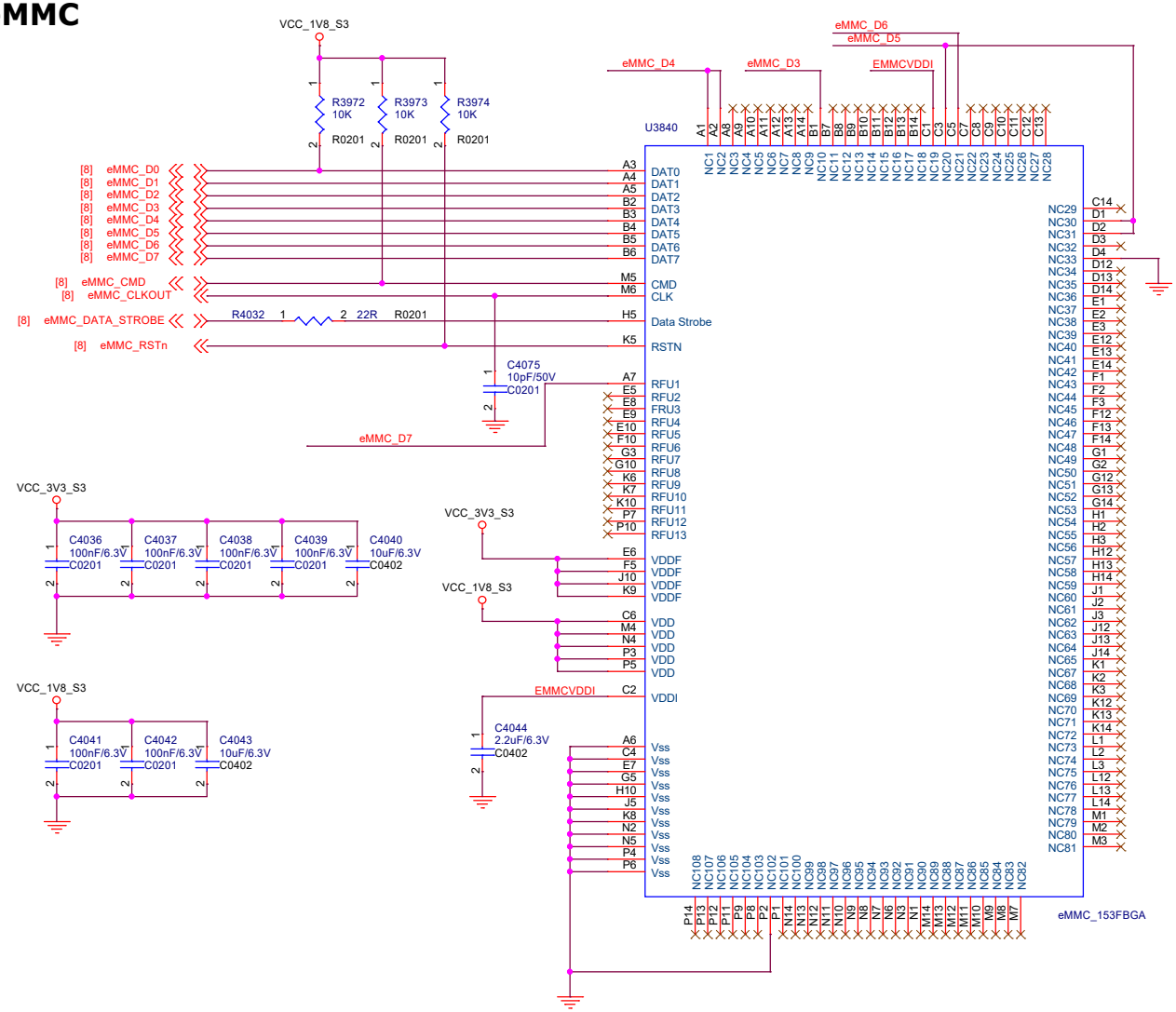
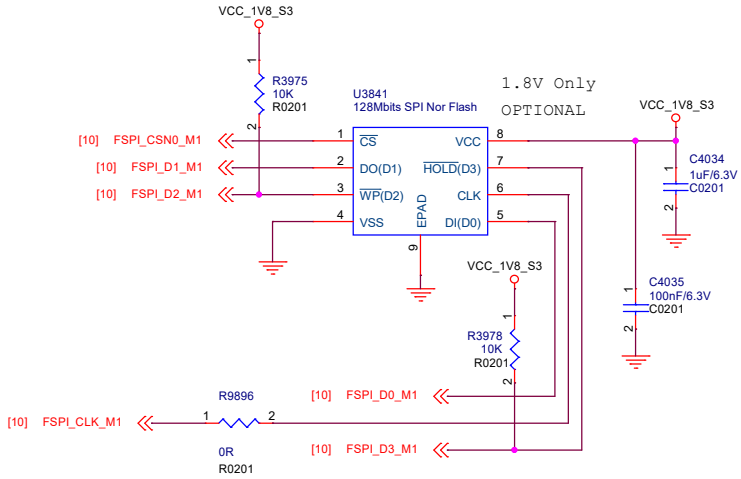
eMMC



SPI Nor Flash



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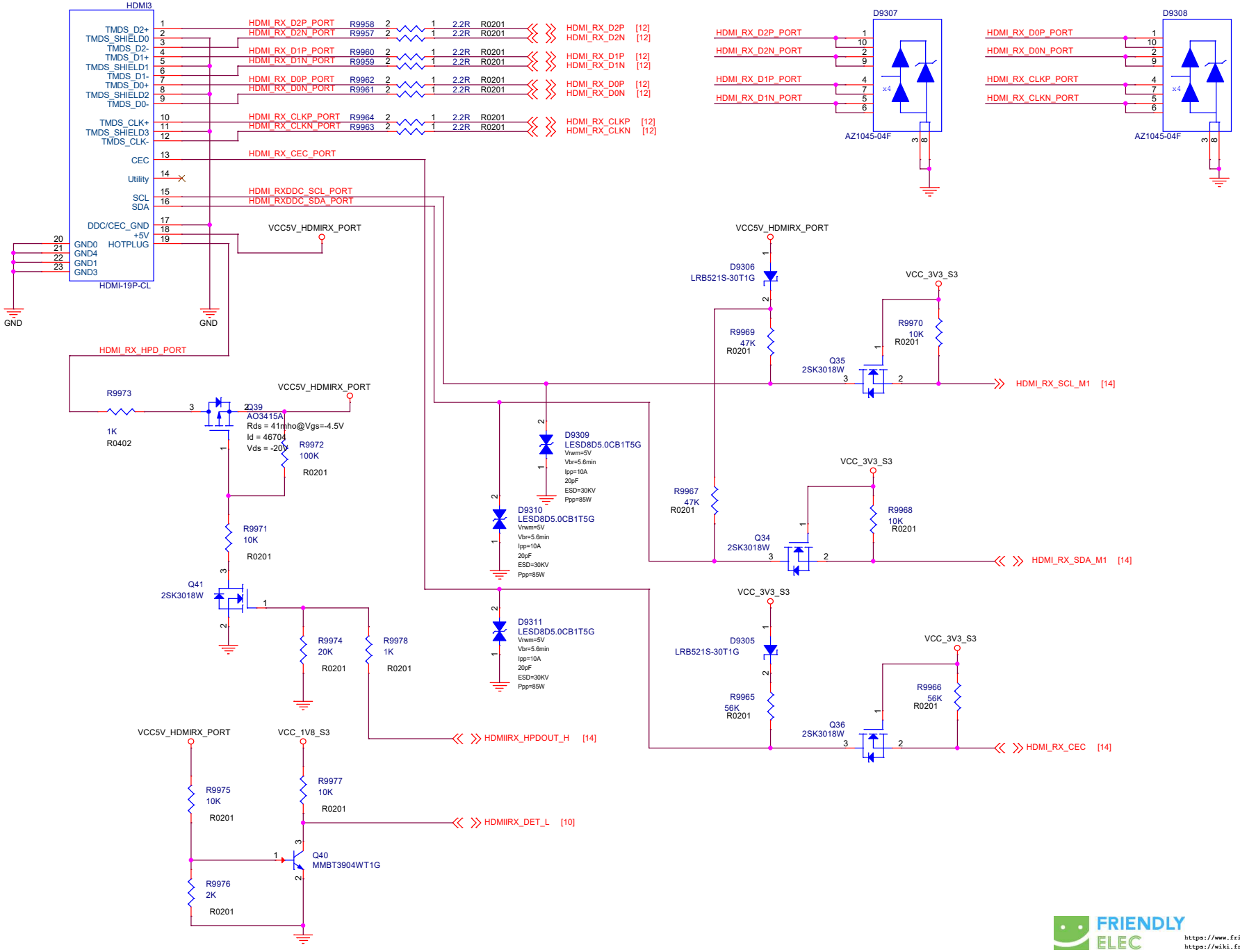
HDMI RX



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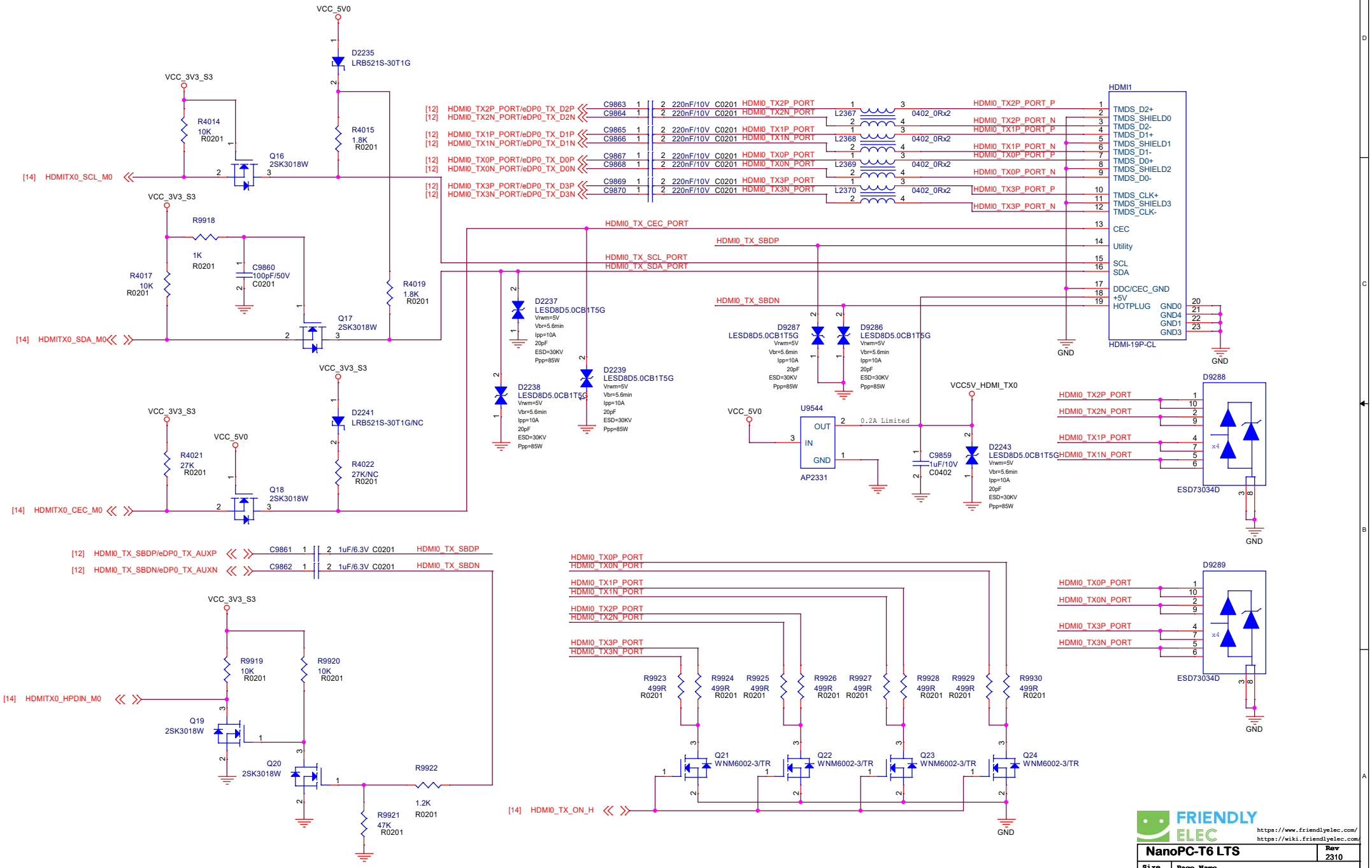
HDMI TX0



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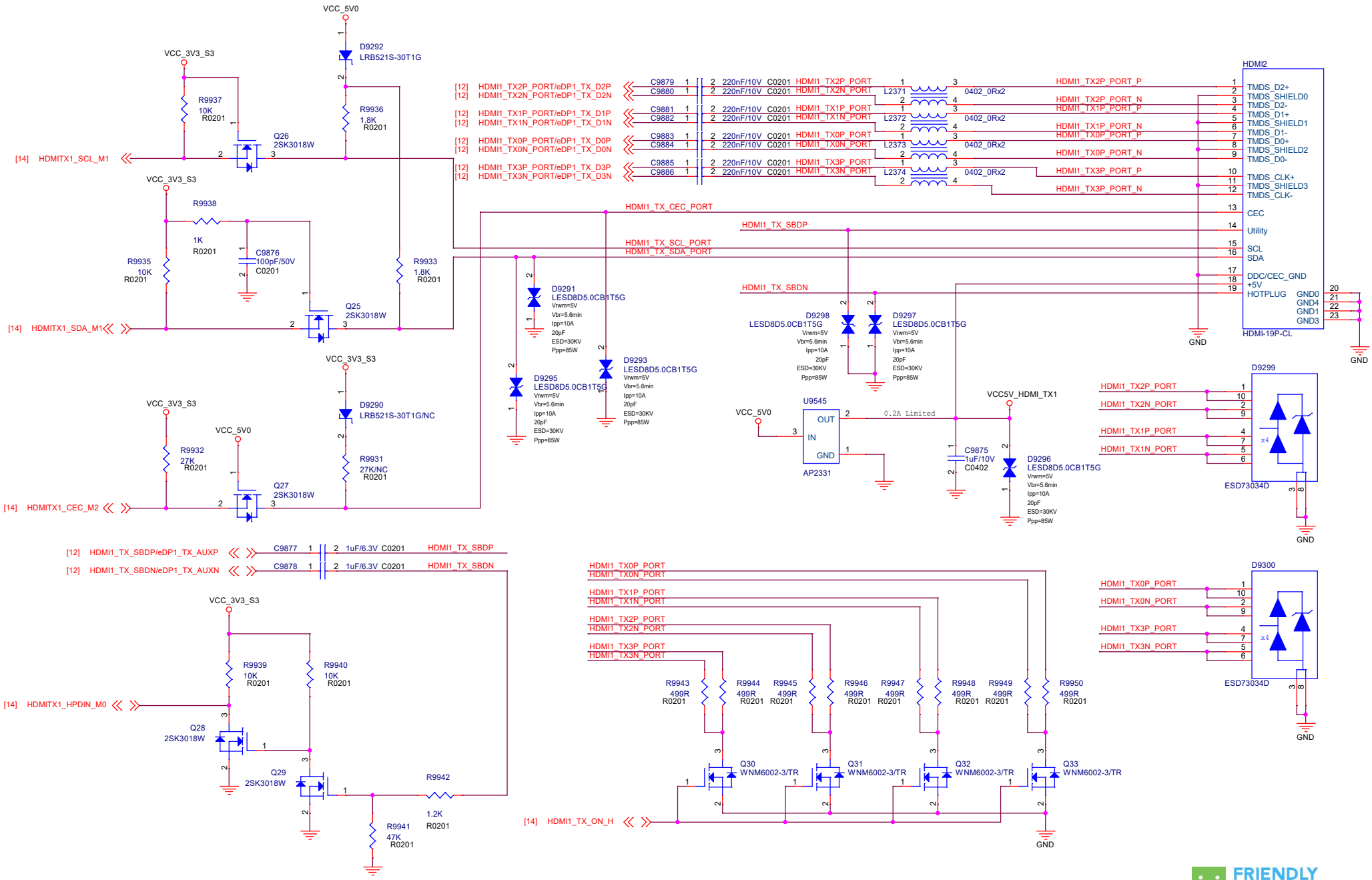
HDMI TX1



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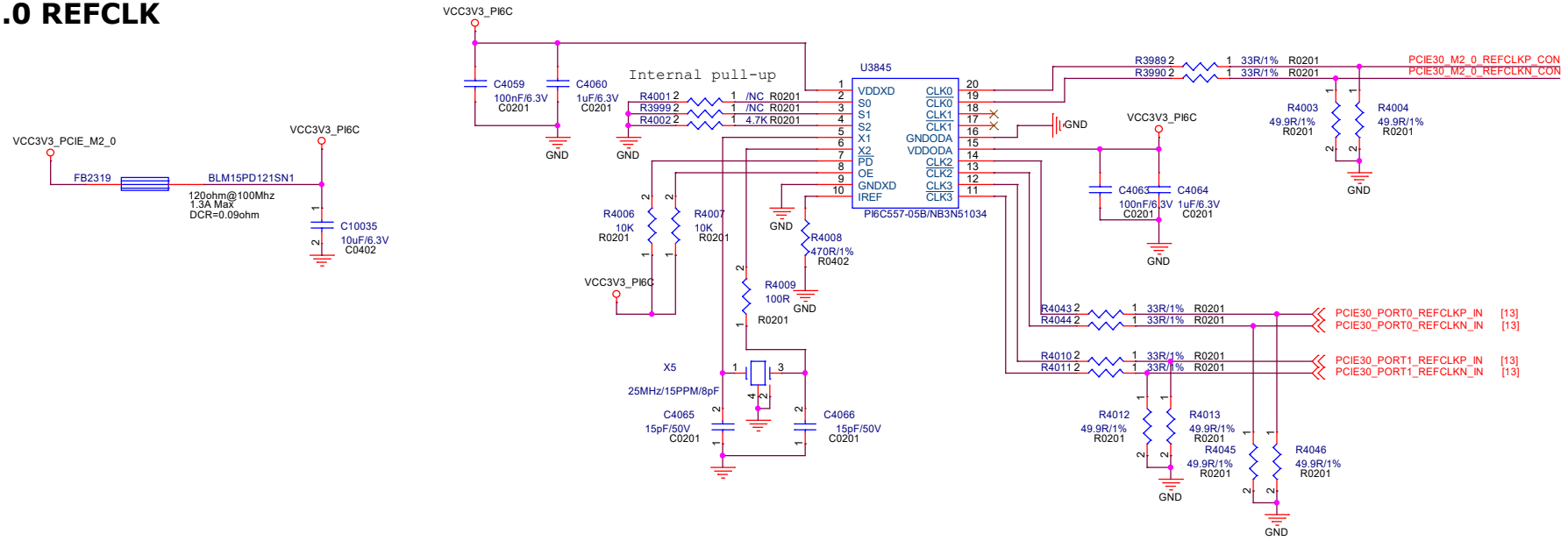
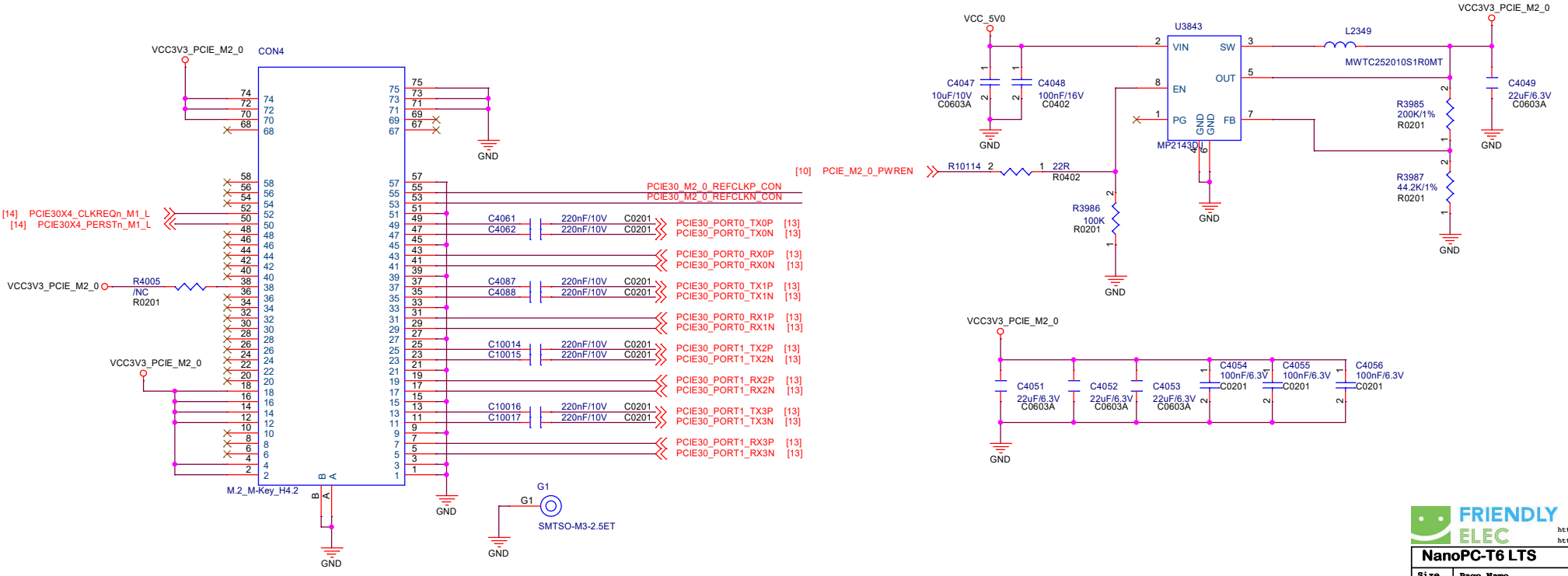
PCIe 3.0 REFCLK



M.2 PCIe 3.0 x4



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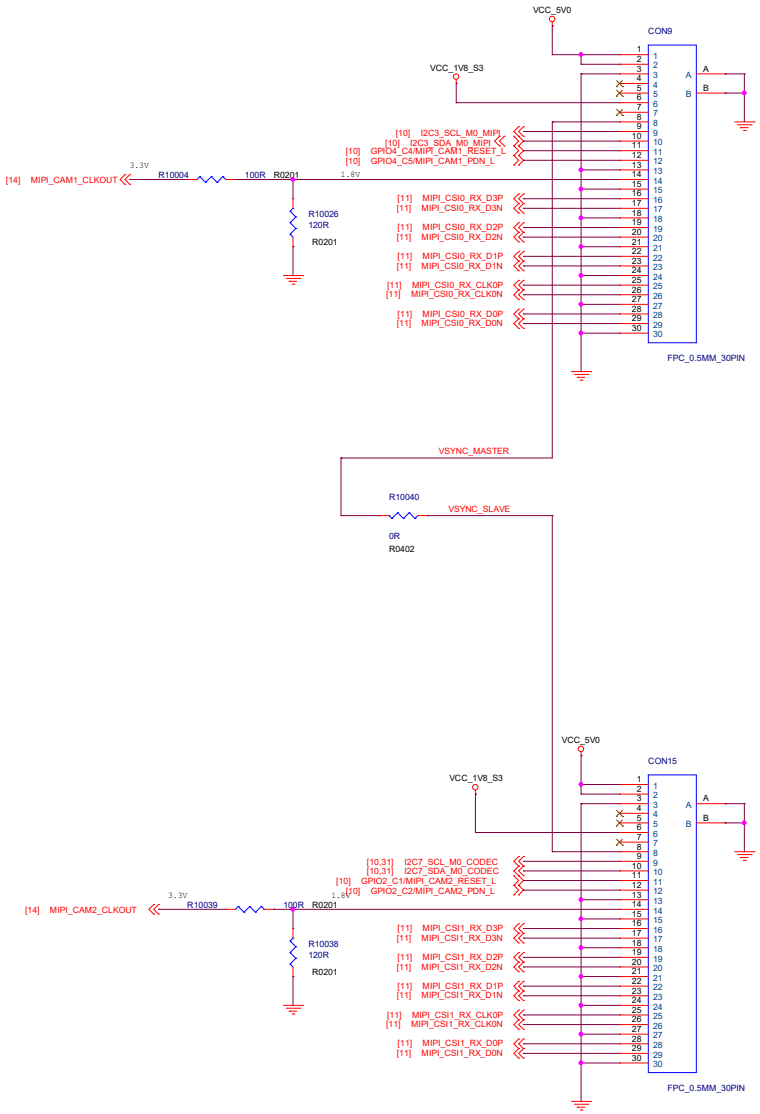
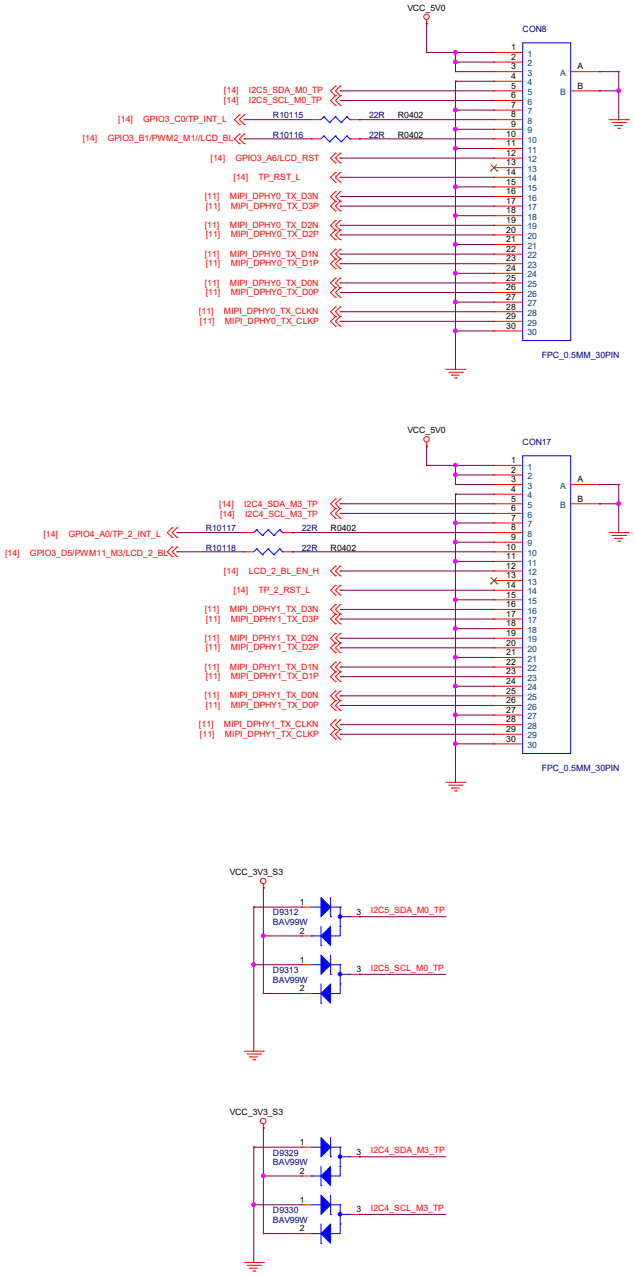
MIPI-CSI



MIPI-DSI



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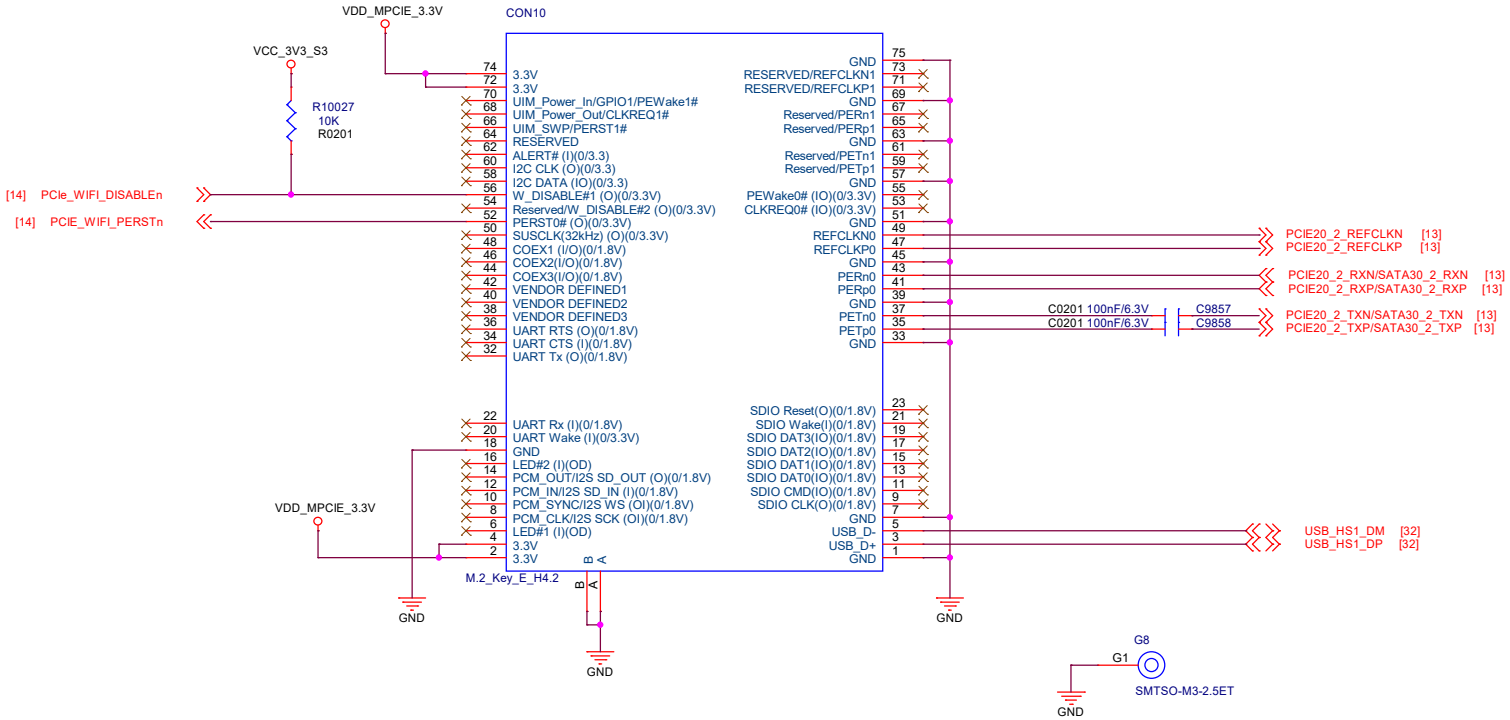
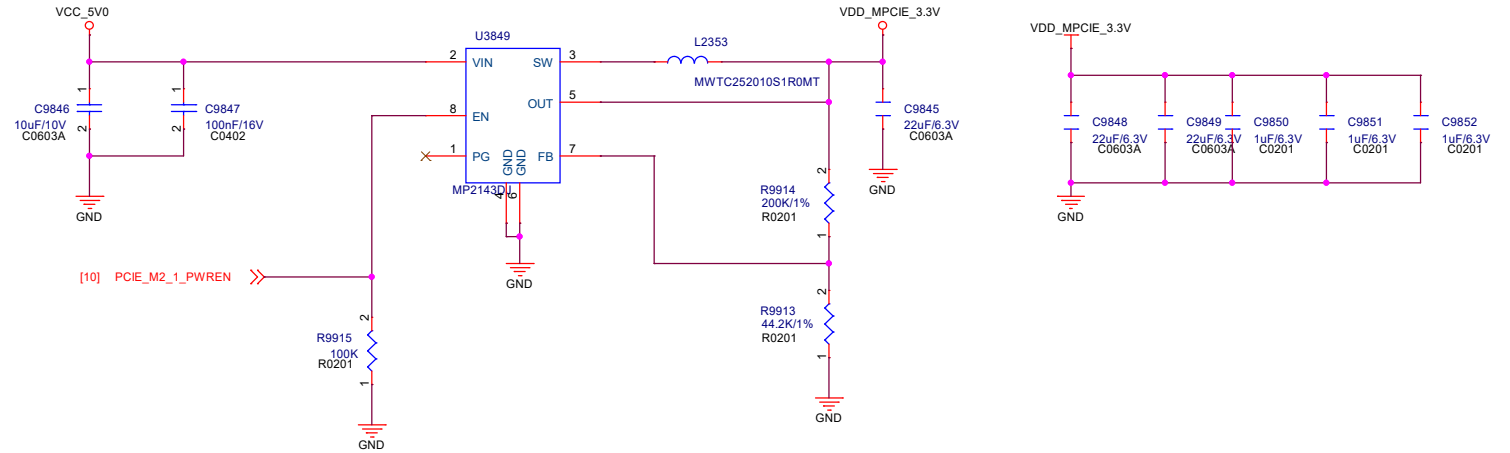
M.2 Key E





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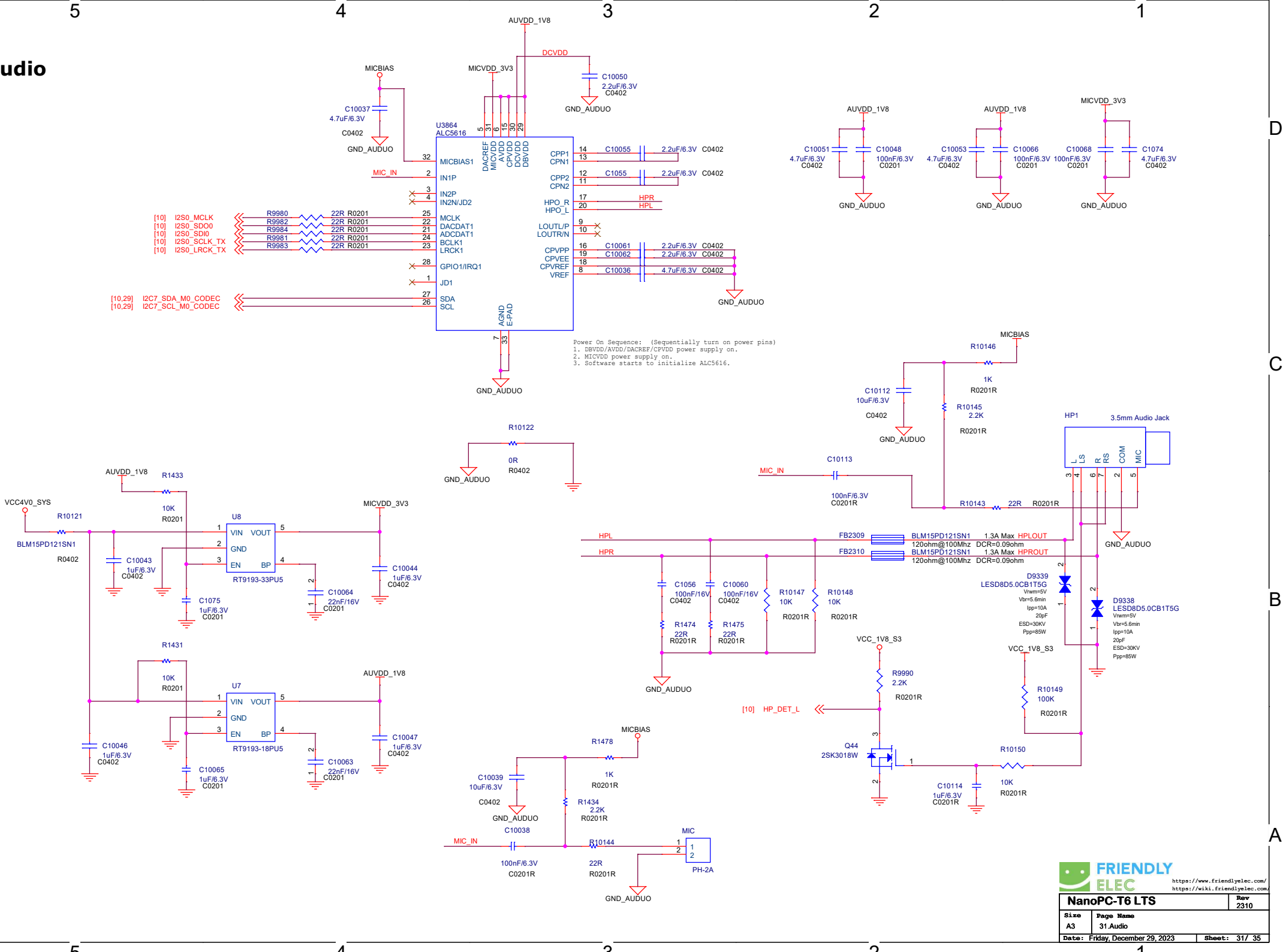
Audio



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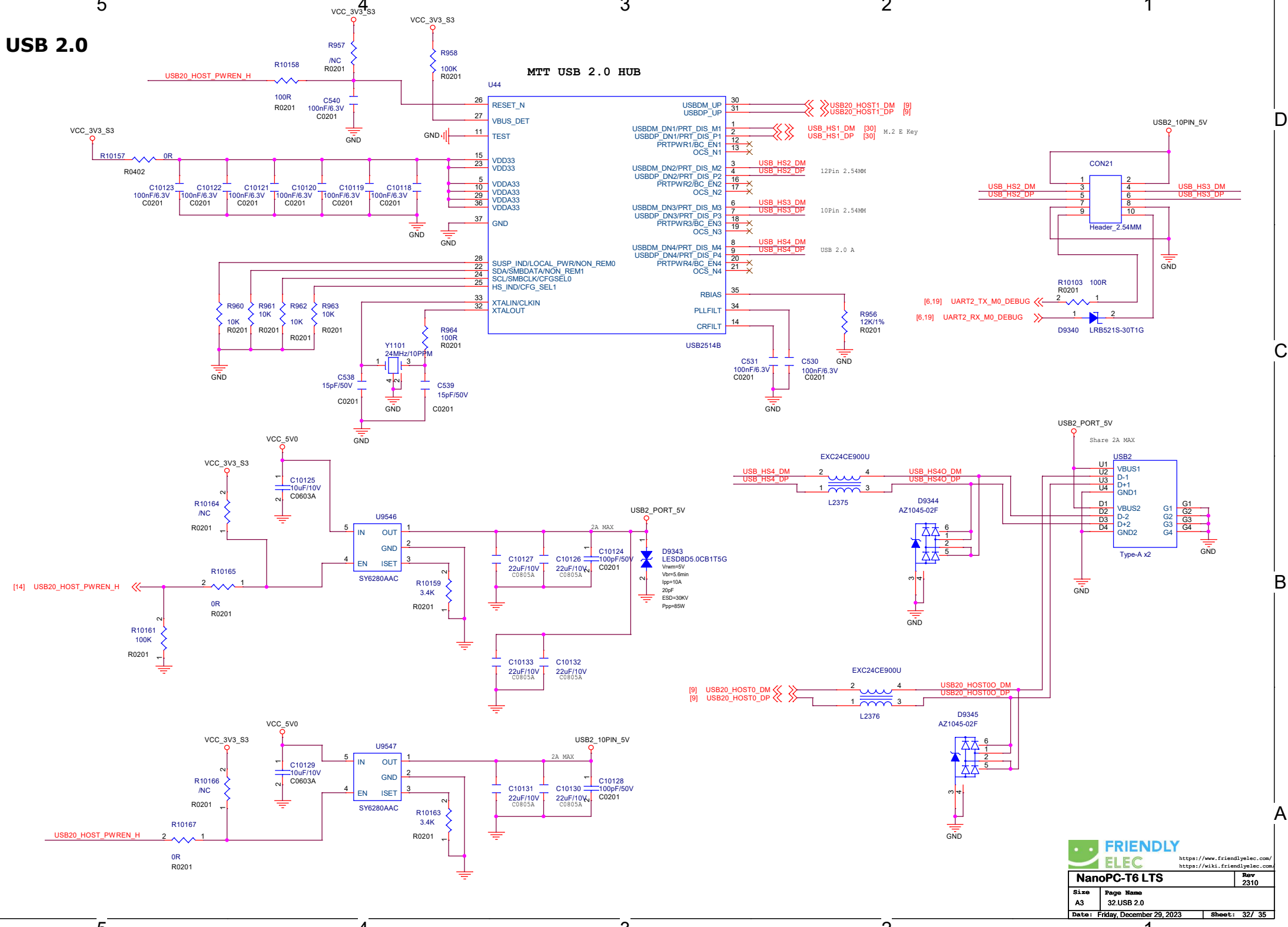
USB 2.0



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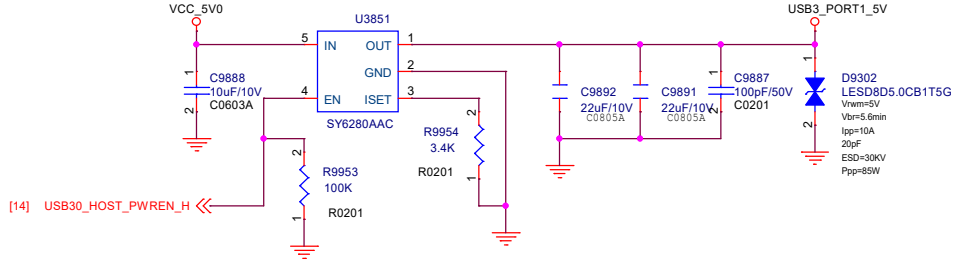
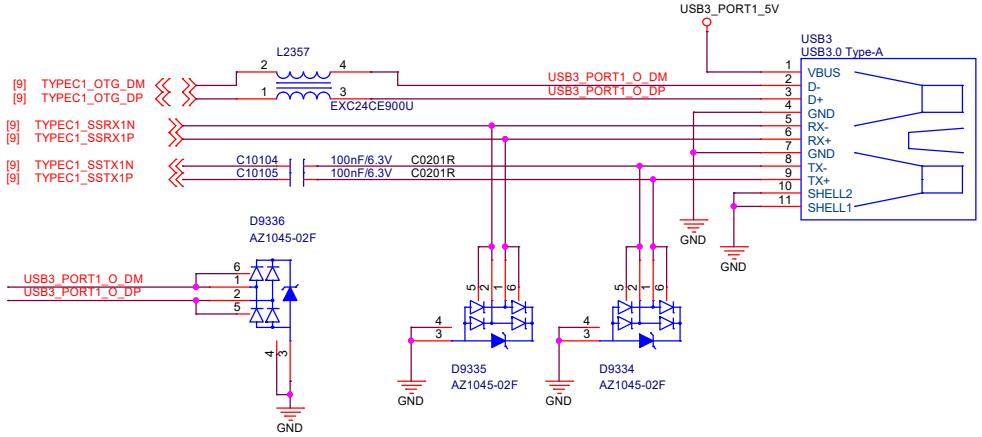
USB 3.0





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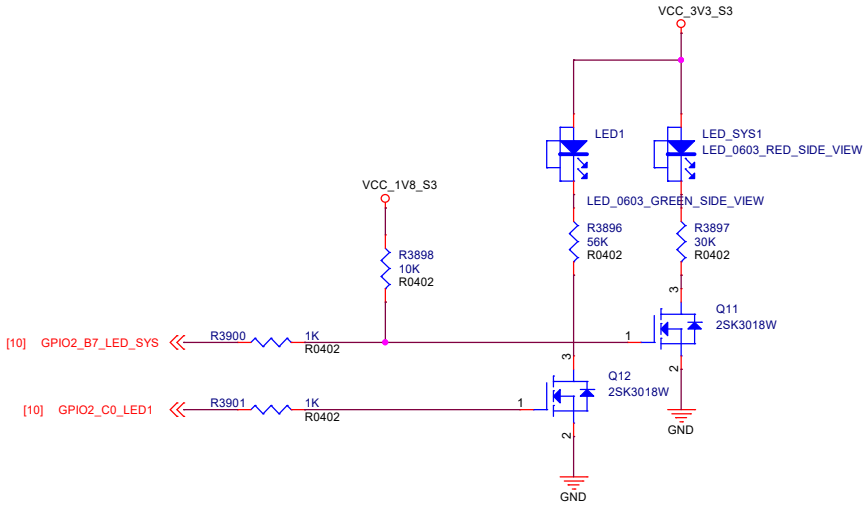
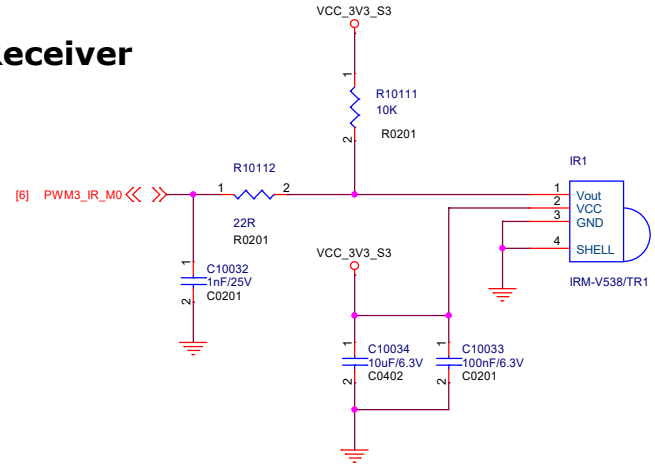
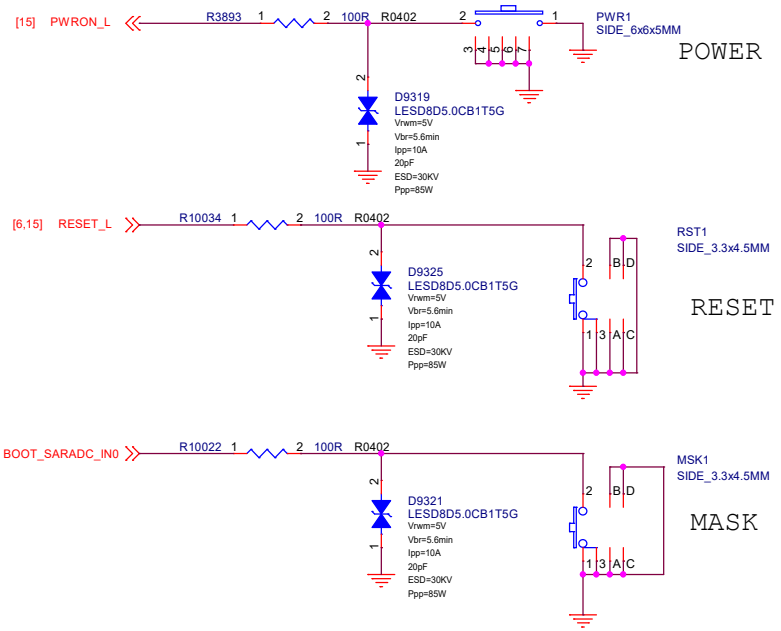
LEDs



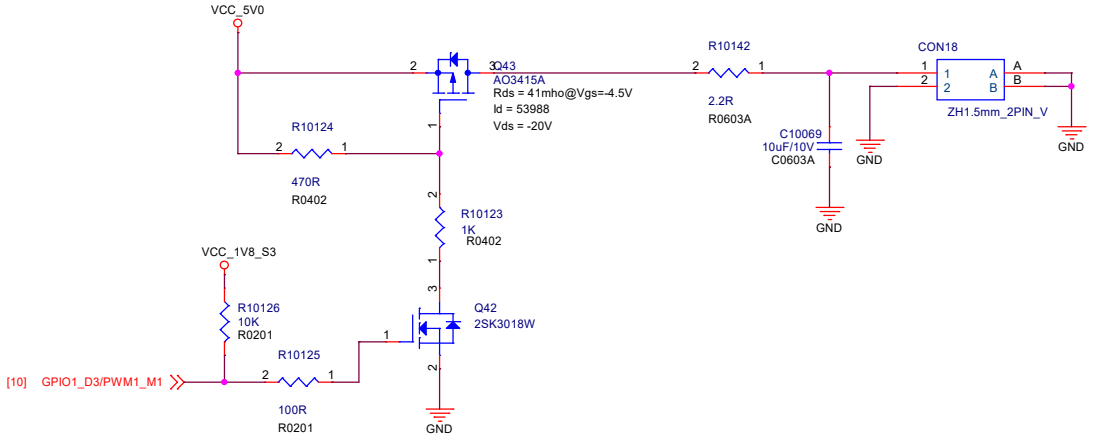
IR Receiver



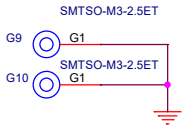
Buttons



5V FAN



Holes



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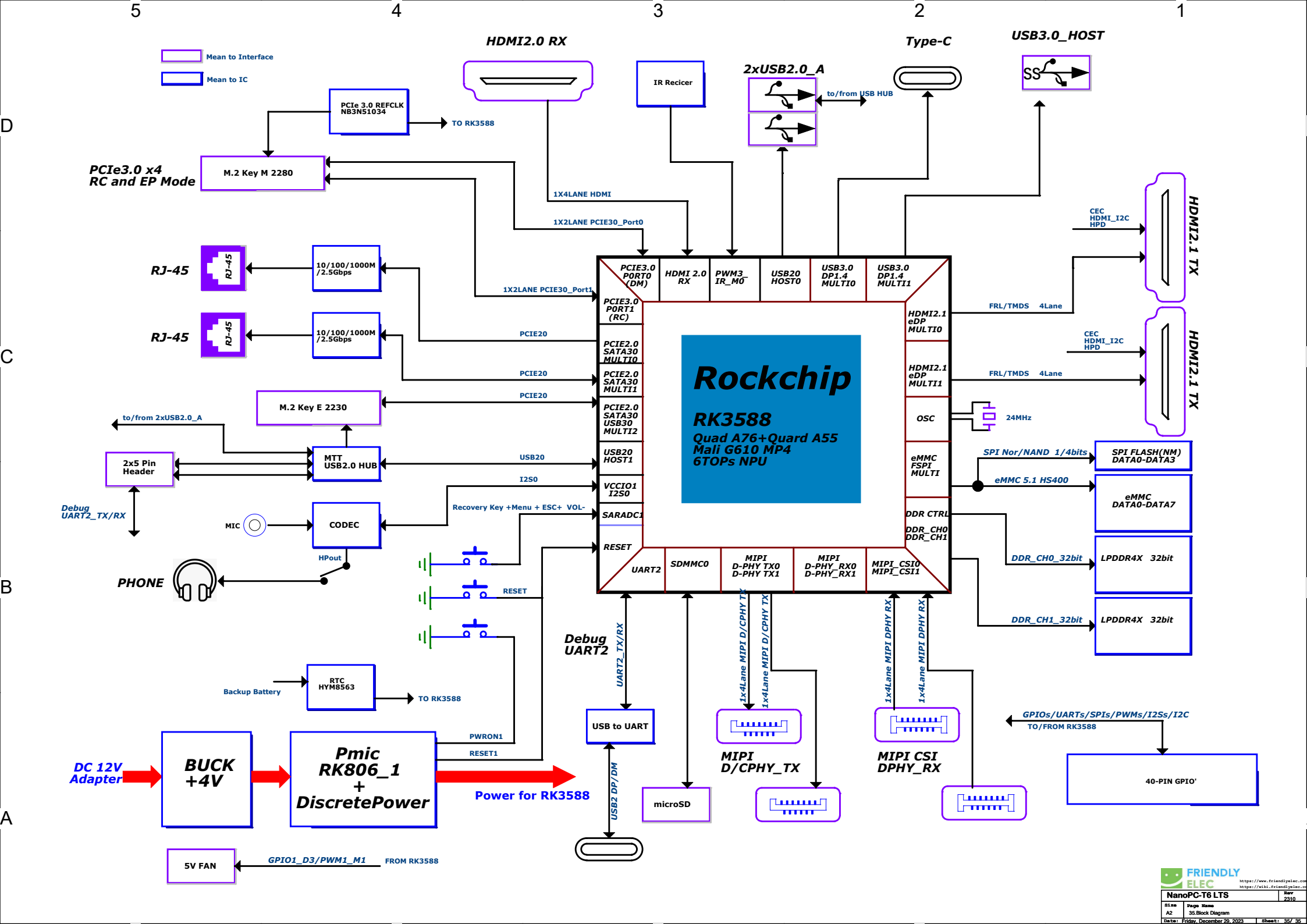
Mean to Interface
Mean to IC
HDMI2.0 RX
IR Recicer
2xUSB2.0_A
to/from USB HUB
Type-C
USB3.0_HOST
PCIe 3.0 REFCLK NB3N51034
TO RK3588
PCIe3.0 x4 RC and EP Mode
M.2 Key M 2280
1X4LANE HDMI
1X2LANE PCIE30_Port0
1X2LANE PCIE30_Port1
PCIE20
RJ-45
10/100/1000M /2.5Gbps
M.2 Key E 2230
to/from 2xUSB2.0_A
2x5 Pin Header
MTT USB2.0 HUB
USB20
I2S0
Debug UART2_TX/RX
MIC
CODEC
Recovery Key +Menu + ESC+ VOL-
HPout
PHONE
RESET
Backup Battery
RTC HYM8563
TO RK3588
PWRON1
RESET1
DC 12V Adapter
BUCK +4V
Pmic RK806_1 + DiscretePower
Power for RK3588
5V FAN
GPIO1_D3/PWM1_M1
FROM RK3588
PCIE3.0 P0RT0 (DM)
HDMI 2.0 RX
PWM3_ IR_M0
USB20 HOST0
USB3.0 DP1.4 MULTI0
USB3.0 DP1.4 MULTI1
PCIE3.0 P0RT1 (RC)
PCIE2.0 SATA30 MULTI0
PCIE2.0 SATA30 MULTI1
PCIE2.0 SATA30 USB30 MULTI2
USB20 HOST1
VCCIO1 I2S0
SARADC1
RESET
UART2
SDMMC0
MIPI D-PHY TX0 D-PHY TX1
MIPI D-PHY_RX0 D-PHY_RX1
MIPI_CSI0 MIPI_CSI1
HDMI2.1 eDP MULTI0
HDMI2.1 eDP MULTI1
OSC
eMMC FSPI MULTI
DDR CTRL
DDR_CH0 DDR_CH1
Rockchip
RK3588
Quad A76+Quard A55
Mali G610 MP4
6TOPs NPU
CEC HDMI_I2C HPD
HDMI2.1 TX
FRL/TMDS 4Lane
24MHz
SPI Nor/NAND 1/4bits
SPI FLASH(NM) DATA0-DATA3
eMMC 5.1 HS400
eMMC DATA0-DATA7
DDR_CH0_32bit
LPDDR4X 32bit
DDR_CH1_32bit
Debug UART2
UART2_TX/RX
USB to UART
USB2 DP/DM
microSD
1x4Lane MIPI D/CPHY TX
MIPI D/CPHY_TX
1x4Lane MIPI DPHY RX
MIPI CSI DPHY_RX
GPIOs/UARTs/SPIs/PWMs/I2Ss/I2C
TO/FROM RK3588
40-PIN GPIO'
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