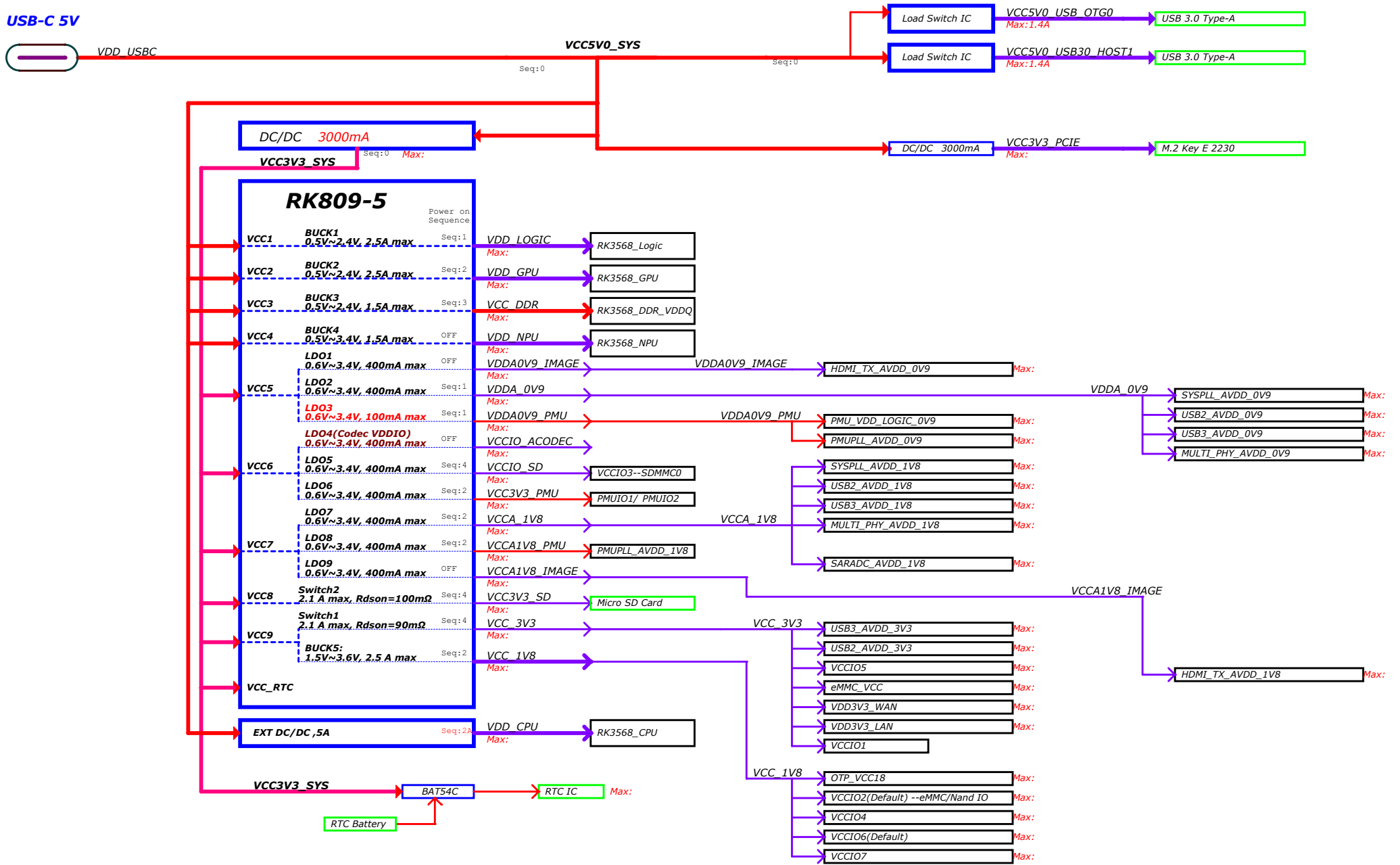
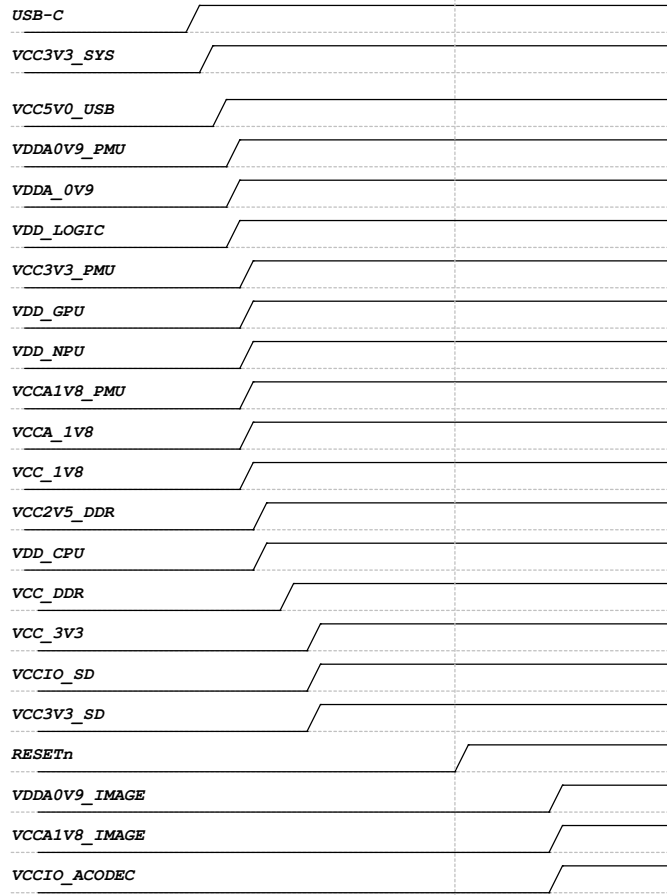


Power Diagram



Power Sequence



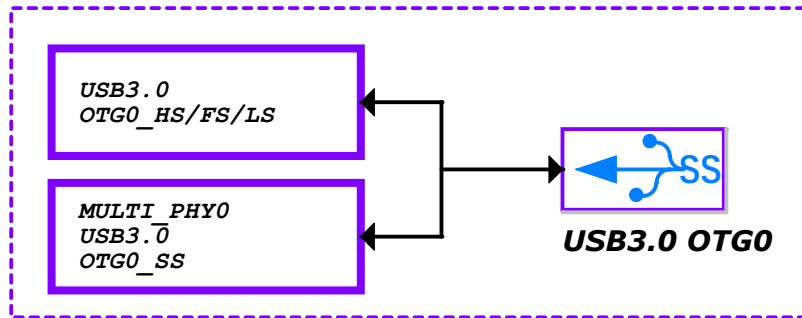
I2C5, 7bit address
 - 0x51, HYM8563TS, RTC IC
 - 0x53, 24AA025E48T, EUI-48 Node Identity

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	100mohm								
VCC3V3_SYS	RK809_SW1	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	90mohm								
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETr			Slot:4+5					
VDD_USB	EXT BUCK	4.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYSP	Slot:0	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD

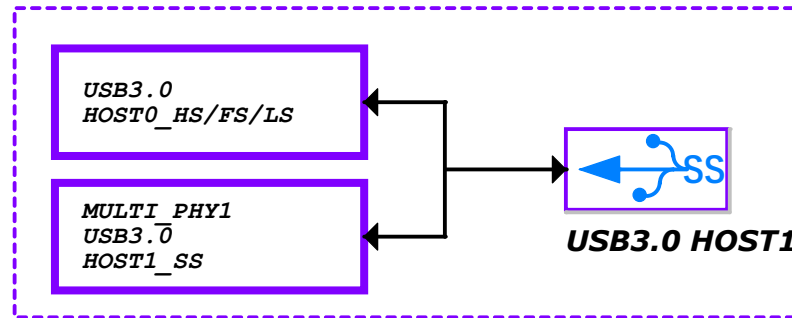
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V, FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

USB3.0 OTGO



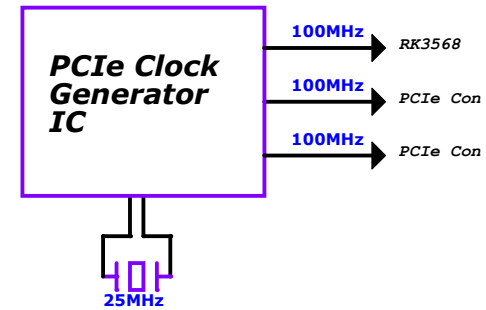
USB3.0 HOST1



PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIe30_REFCLK (RC/EP:input)	PCIe30_TX0 PCIe30_RX0 PCIe30_TX1 PCIe30_RX1	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIe30_REFCLK (RC:input)	PCIe30_TX0 PCIe30_RX0	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	Only RC
			PCIe30_TX1 PCIe30_RX1	PCIe30X1_CLKREQn PCIe30X1_WAKEn PCIe30X1_PERSTn PCIe30X1_BUTTONRSTn	Only RC

PCIe REFCLK

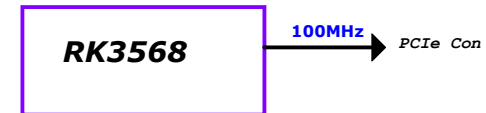


Configured to PCIe 2.0

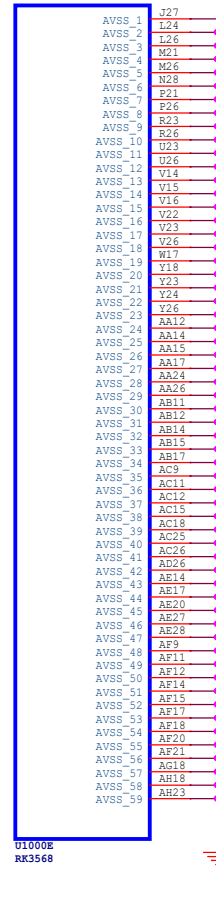
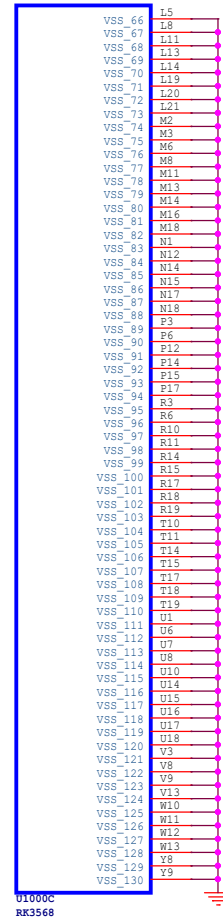
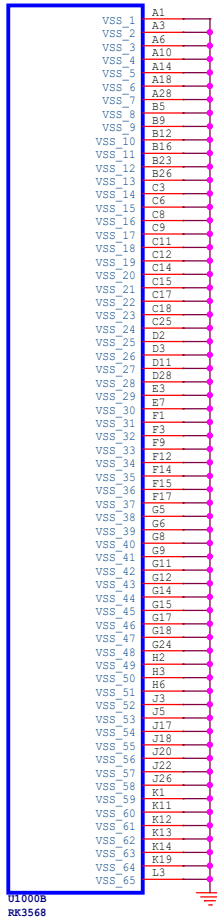
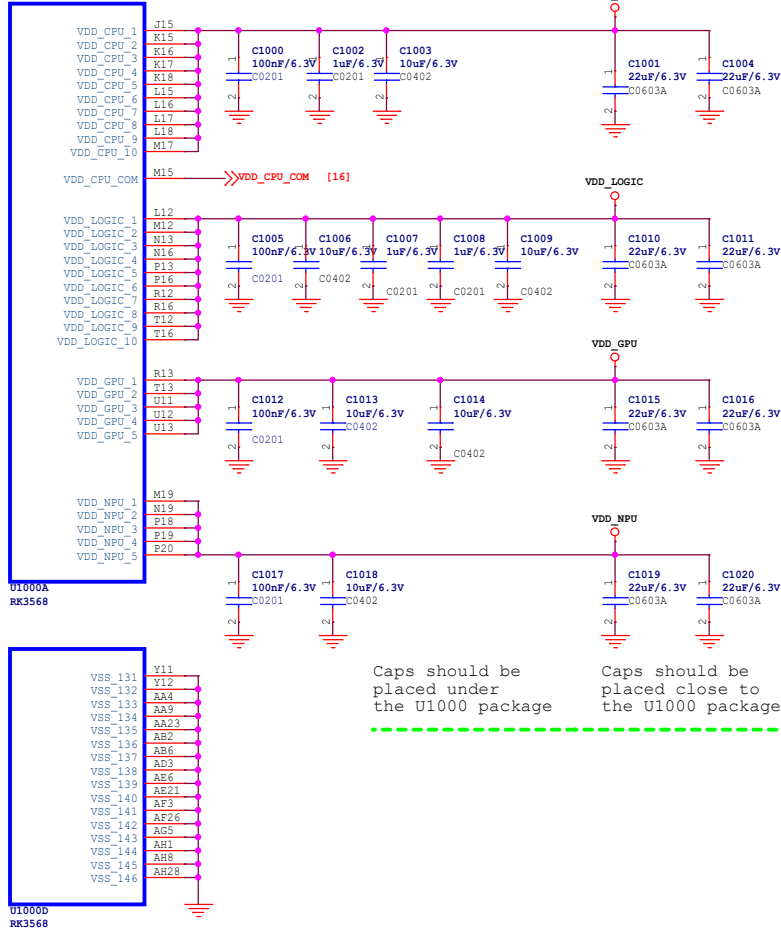
PCIe2.0 PHY

MULTI_PHY2	PCIe2.0 x1Lane	PCIe20_REFCLK (RC:output)	PCIe20_TX PCIe20_RX	PCIe20_CLKREQn PCIe20_WAKEn PCIe20_PERSTn PCIe20_BUTTONRSTn	Only RC
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PCIe2.0 REFCLK



RK3568_ABCDE (Power&Gnd)



Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

RK3568_F (DDR PHY)

	DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3						
[14] LPDDR4_DQ0_A	DDR_DQ0 A	F2	DDR_DQ0 A / DDR4_DQ0 A	LPDDR4_DQ0 A	DDR3_DQ0	LPDDR3_DQ0	DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC0	B6	AC0	LPDDR4_CLKP_B [14]
[14] LPDDR4_DQ1_A	DDR_DQ1 A	E1	DDR_DQ1 A / DDR4_DQ1 A	LPDDR4_DQ1 A	DDR3_DQ1	LPDDR3_DQ1	DDR4_A1	---	---	---	AC1	B1	AC2	LPDDR4_A1_A [14]
[14] LPDDR4_DQ2_A	DDR_DQ2 A	E2	DDR_DQ2 A / DDR4_DQ2 A	LPDDR4_DQ2 A	DDR3_DQ2	LPDDR3_DQ2	DDR4_A2	LPDDR4_CLKN_B	DDR3_A8	LPDDR3_A6	AC2	F4	AC3	LPDDR4_CKE1_A [14]
[14] LPDDR4_DQ3_A	DDR_DQ3 A	D1	DDR_DQ3 A / DDR4_DQ3 A	LPDDR4_DQ3 A	DDR3_DQ3	LPDDR3_DQ3	DDR4_A3	LPDDR4_CKE1_A	DDR3_A7	---	AC3			
[14] LPDDR4_DQ4_A	DDR_DQ4 A	J1	DDR_DQ4 A / DDR4_DQ4 A	LPDDR4_DQ4 A	DDR3_DQ4	LPDDR3_DQ4	DDR4_A4	---	---	---	AC4	D9	AC4	LPDDR4_A3_B [14]
[14] LPDDR4_DQ5_A	DDR_DQ5 A	J2	DDR_DQ5 A / DDR4_DQ5 A	LPDDR4_DQ5 A	DDR3_DQ5	LPDDR3_DQ5	DDR4_A5	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4	E7	AC5	LPDDR4_A5_B [14]
[14] LPDDR4_DQ6_A	DDR_DQ6 A	H1	DDR_DQ6 A / DDR4_DQ6 A	LPDDR4_DQ6 A	DDR3_DQ6	LPDDR3_DQ6	DDR4_A6	LPDDR4_A1_B	DDR3_A11	LPDDR3_A2	AC5	A7	AC6	LPDDR4_A1_B [14]
[14] LPDDR4_DQ7_A	DDR_DQ7 A	H4	DDR_DQ7 A / DDR4_DQ7 A	LPDDR4_DQ7 A	DDR3_DQ7	LPDDR3_DQ7	DDR4_A7	LPDDR4_A1_B	DDR3_A10	LPDDR3_A1	AC6	A8	AC7	LPDDR4_ODT0_CA_B [14]
[14] LPDDR4_DQ0_A	DDR_DM0 A	H5	DDR_DM0 A / DDR4_DM0 A	LPDDR4_DM0 A	DDR3_DM0	LPDDR3_DM1	DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A9	---	AC7			
[14] LPDDR4_DQ80P_A	DDR_DQ80P A	G1	DDR_DQ80P A / DDR4_DQ80P A	LPDDR4_DQ80P A	DDR3_DQ80P	LPDDR3_DQ81P	DDR4_A8	LPDDR4_ODT0_CA_B	DDR3_A6	LPDDR3_A9	AC8	C1	AC8	LPDDR4_ODT0_CA_A [14]
[14] LPDDR4_DQ80N_A	DDR_DQ80N A	G2	DDR_DQ80N A / DDR4_DQ80N A	LPDDR4_DQ80N A	DDR3_DQ80N	LPDDR3_DQ81N	DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC8	A5	AC9	LPDDR4_CLKN_B [14]
[14] LPDDR4_DQ8_A	DDR_DQ8 A	M1	DDR_DQ8 A / DDR4_DQ8 A	LPDDR4_DQ8 A	DDR3_DQ8	LPDDR3_DQ8	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10	D6	AC10	LPDDR4_CKE0_B [14]
[14] LPDDR4_DQ9_A	DDR_DQ9 A	N2	DDR_DQ9 A / DDR4_DQ9 A	LPDDR4_DQ9 A	DDR3_DQ9	LPDDR3_DQ9	DDR4_A11	LPDDR4_A0_A	DDR3_A7	---	AC11	C2	AC11	LPDDR4_A0_A [14]
[14] LPDDR4_DQ10_A	DDR_DQ10 A	L7	DDR_DQ10 A / DDR4_DQ10 A	LPDDR4_DQ10 A	DDR3_DQ10	LPDDR3_DQ10	DDR4_A12	---	---	---	AC12	C4	AC12	LPDDR4_A3_A [14]
[14] LPDDR4_DQ11_A	DDR_DQ11 A	L6	DDR_DQ11 A / DDR4_DQ11 A	LPDDR4_DQ11 A	DDR3_DQ11	LPDDR3_DQ11	DDR4_A13	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC12	B8	AC13	LPDDR4_A0_B [14]
[14] LPDDR4_DQ12_A	DDR_DQ12 A	K2	DDR_DQ12 A / DDR4_DQ12 A	LPDDR4_DQ12 A	DDR3_DQ12	LPDDR3_DQ12	DDR4_A14	LPDDR4_A4_A	DDR3_A10	---	AC13	C5	AC14	LPDDR4_A4_A [14]
[14] LPDDR4_DQ13_A	DDR_DQ13 A	K6	DDR_DQ13 A / DDR4_DQ13 A	LPDDR4_DQ13 A	DDR3_DQ13	LPDDR3_DQ13	DDR4_A15	LPDDR4_A4_A	DDR3_A10	---	AC14	E4	AC15	LPDDR4_A2_A [14]
[14] LPDDR4_DQ14_A	DDR_DQ14 A	J7	DDR_DQ14 A / DDR4_DQ14 A	LPDDR4_DQ14 A	DDR3_DQ14	LPDDR3_DQ14	DDR4_A16	RASN	LPDDR4_A5_A	DDR3_RASN	LPDDR3_A7	D5	AC16	LPDDR4_A5_A [14]
[14] LPDDR4_DQ15_A	DDR_DQ15 A	L4	DDR_DQ15 A / DDR4_DQ15 A	LPDDR4_DQ15 A	DDR3_DQ15	LPDDR3_DQ15	DDR4_A17	LPDDR4_CKE1_B	DDR3_CAS	---	AC17	E11	AC18	LPDDR4_A2_B [14]
[14] LPDDR4_DM1_A	DDR_DM1 A	J4	DDR_DM1 A / DDR4_DM1 A	LPDDR4_DM1 A	DDR3_DM1	LPDDR3_DM3	DDR4_A18	LPDDR4_CKE1_B	DDR3_CAS	---	AC18	E9	AC19	LPDDR4_A4_B [14]
[14] LPDDR4_DQ81P_A	DDR_DQ81P A	L2	DDR_DQ81P A / DDR4_DQ81P A	LPDDR4_DQ81P A	DDR3_DQ81P	LPDDR3_DQ83P	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ81N_A	DDR_DQ81N A	L1	DDR_DQ81N A / DDR4_DQ81N A	LPDDR4_DQ81N A	DDR3_DQ81N	LPDDR3_DQ83N	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ0_B	DDR_DQ0 B	B10	DDR_DQ0 B / DDR4_DQ0 B	LPDDR4_DQ0 B	DDR3_DQ16	LPDDR3_DQ1	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ1_B	DDR_DQ1 B	A9	DDR_DQ1 B / DDR4_DQ1 B	LPDDR4_DQ1 B	DDR3_DQ17	LPDDR3_DQ2	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ2_B	DDR_DQ2 B	D12	DDR_DQ2 B / DDR4_DQ2 B	LPDDR4_DQ2 B	DDR3_DQ18	LPDDR3_DQ3	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ3_B	DDR_DQ3 B	E12	DDR_DQ3 B / DDR4_DQ3 B	LPDDR4_DQ3 B	DDR3_DQ19	LPDDR3_DQ4	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ4_B	DDR_DQ4 B	A12	DDR_DQ4 B / DDR4_DQ4 B	LPDDR4_DQ4 B	DDR3_DQ20	LPDDR3_DQ5	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ5_B	DDR_DQ5 B	D15	DDR_DQ5 B / DDR4_DQ5 B	LPDDR4_DQ5 B	DDR3_DQ21	LPDDR3_DQ6	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ6_B	DDR_DQ6 B	E15	DDR_DQ6 B / DDR4_DQ6 B	LPDDR4_DQ6 B	DDR3_DQ22	LPDDR3_DQ7	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ7_B	DDR_DQ7 B	E14	DDR_DQ7 B / DDR4_DQ7 B	LPDDR4_DQ7 B	DDR3_DQ23	LPDDR3_DQ8	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DM0_B	DDR_DM0 B	D14	DDR_DM0 B / DDR4_DM0 B	LPDDR4_DM0 B	DDR3_DM2	LPDDR3_DM0	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ80P_B	DDR_DQ80P B	A11	DDR_DQ80P B / DDR4_DQ80P B	LPDDR4_DQ80P B	DDR3_DQ24	LPDDR3_DQ18	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ80N_B	DDR_DQ80N B	B11	DDR_DQ80N B / DDR4_DQ80N B	LPDDR4_DQ80N B	DDR3_DQ25	LPDDR3_DQ19	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ8_B	DDR_DQ8 B	A16	DDR_DQ8 B / DDR4_DQ8 B	LPDDR4_DQ8 B	DDR3_DQ26	LPDDR3_DQ20	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ9_B	DDR_DQ9 B	B17	DDR_DQ9 B / DDR4_DQ9 B	LPDDR4_DQ9 B	DDR3_DQ27	LPDDR3_DQ21	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ10_B	DDR_DQ10 B	A17	DDR_DQ10 B / DDR4_DQ10 B	LPDDR4_DQ10 B	DDR3_DQ28	LPDDR3_DQ22	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ11_B	DDR_DQ11 B	B18	DDR_DQ11 B / DDR4_DQ11 B	LPDDR4_DQ11 B	DDR3_DQ29	LPDDR3_DQ23	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ12_B	DDR_DQ12 B	B13	DDR_DQ12 B / DDR4_DQ12 B	LPDDR4_DQ12 B	DDR3_DQ30	LPDDR3_DQ24	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ13_B	DDR_DQ13 B	A13	DDR_DQ13 B / DDR4_DQ13 B	LPDDR4_DQ13 B	DDR3_DQ31	LPDDR3_DQ25	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ14_B	DDR_DQ14 B	D17	DDR_DQ14 B / DDR4_DQ14 B	LPDDR4_DQ14 B	DDR3_DQ32	LPDDR3_DQ26	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ15_B	DDR_DQ15 B	B14	DDR_DQ15 B / DDR4_DQ15 B	LPDDR4_DQ15 B	DDR3_DQ33	LPDDR3_DQ27	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DM1_B	DDR_DM1 B	E17	DDR_DM1 B / DDR4_DM1 B	LPDDR4_DM1 B	DDR3_DM3	LPDDR3_DM2	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ81P_B	DDR_DQ81P B	B15	DDR_DQ81P B / DDR4_DQ81P B	LPDDR4_DQ81P B	DDR3_DQ34	LPDDR3_DQ28	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ81N_B	DDR_DQ81N B	A15	DDR_DQ81N B / DDR4_DQ81N B	LPDDR4_DQ81N B	DDR3_DQ35	LPDDR3_DQ29	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ8_B	DDR_DQ8 B	M4	DDR_DQ8 B / DDR4_DQ8 B	LPDDR4_DQ8 B	DDR3_DQ36	LPDDR3_DQ30	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ9_B	DDR_DQ9 B	M5	DDR_DQ9 B / DDR4_DQ9 B	LPDDR4_DQ9 B	DDR3_DQ37	LPDDR3_DQ31	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ10_B	DDR_DQ10 B	R5	DDR_DQ10 B / DDR4_DQ10 B	LPDDR4_DQ10 B	DDR3_DQ38	LPDDR3_DQ32	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ11_B	DDR_DQ11 B	M7	DDR_DQ11 B / DDR4_DQ11 B	LPDDR4_DQ11 B	DDR3_DQ39	LPDDR3_DQ33	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ12_B	DDR_DQ12 B	E7	DDR_DQ12 B / DDR4_DQ12 B	LPDDR4_DQ12 B	DDR3_DQ40	LPDDR3_DQ34	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ13_B	DDR_DQ13 B	E4	DDR_DQ13 B / DDR4_DQ13 B	LPDDR4_DQ13 B	DDR3_DQ41	LPDDR3_DQ35	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ14_B	DDR_DQ14 B	R4	DDR_DQ14 B / DDR4_DQ14 B	LPDDR4_DQ14 B	DDR3_DQ42	LPDDR3_DQ36	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ15_B	DDR_DQ15 B	E1	DDR_DQ15 B / DDR4_DQ15 B	LPDDR4_DQ15 B	DDR3_DQ43	LPDDR3_DQ37	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DM1_B	DDR_DM1 B	P7	DDR_DM1 B / DDR4_DM1 B	LPDDR4_DM1 B	DDR3_DM3	LPDDR3_DM2	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ81P_B	DDR_DQ81P B	E2	DDR_DQ81P B / DDR4_DQ81P B	LPDDR4_DQ81P B	DDR3_DQ44	LPDDR3_DQ38	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			
[14] LPDDR4_DQ81N_B	DDR_DQ81N B	E1	DDR_DQ81N B / DDR4_DQ81N B	LPDDR4_DQ81N B	DDR3_DQ45	LPDDR3_DQ39	DDR4_BA1	LPDDR4_A2_A	DDR3_A10	---	AC19			

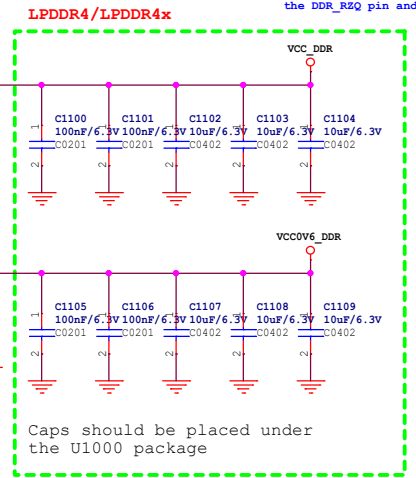
Note: Sequences can not be swap

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_REQ pin and VSS pin

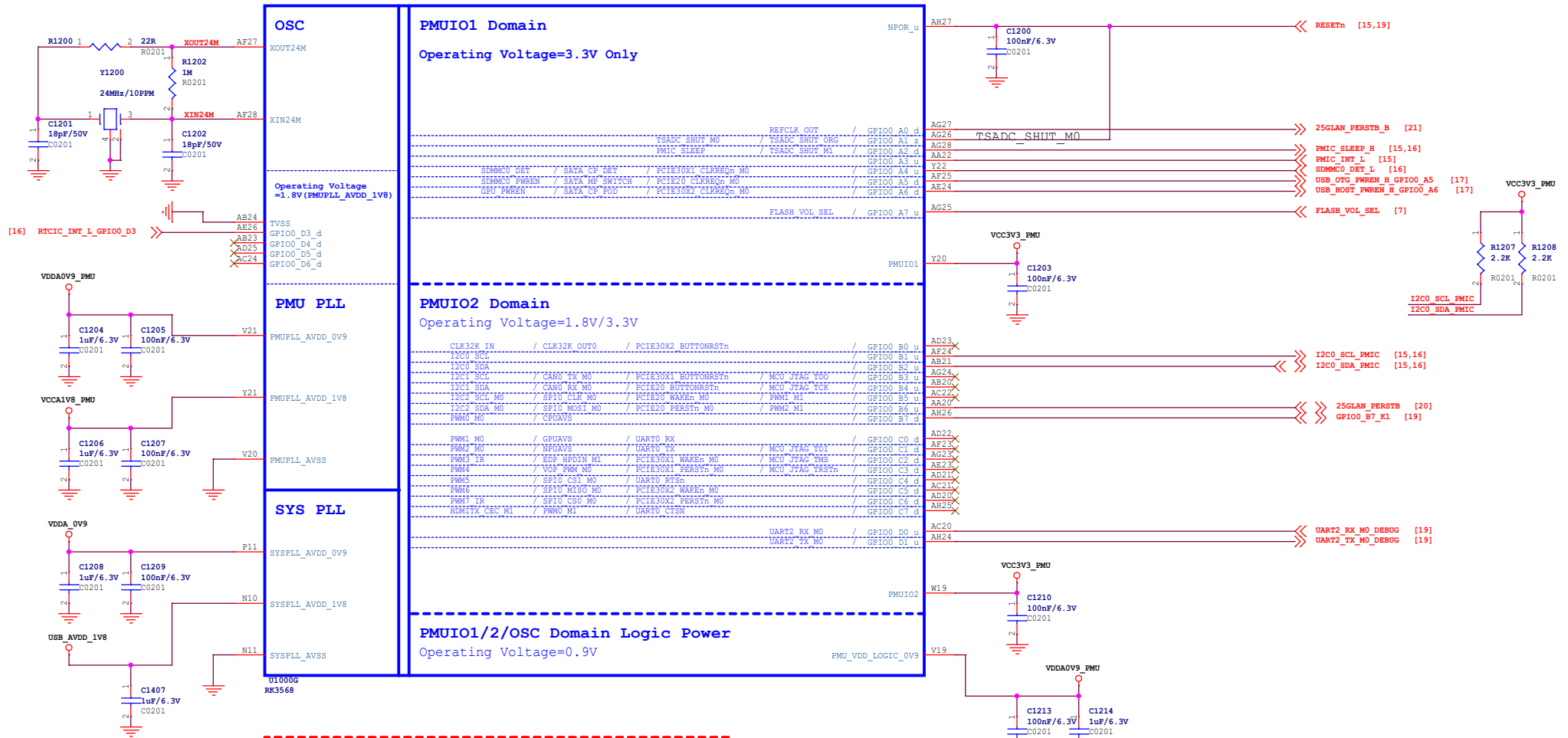
For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_REQ pin and DDRPHY_VDDQ pin

DDR3L = 1.35V	DDRPHY_VDDQ_1	H9
DDR3 = 1.5V	DDRPHY_VDDQ_2	H12
DDR4 = 1.2V	DDRPHY_VDDQ_3	H14
LPDDR3 = 1.2V	DDRPHY_VDDQ_4	H15
LPDDR4 = 1.1V	DDRPHY_VDDQ_5	J9
LPDDR4x = 1.1V	DDRPHY_VDDQ_6	L9
	DDRPHY_VDDQ_7	M9
	DDRPHY_VDDQ_8	
DDR3L = 1.35V	DDRPHY_VDDQ_1	J11
DDR3 = 1.5V	DDRPHY_VDDQ_2	J12
DDR4 = 1.2V	DDRPHY_VDDQ_3	J14
LPDDR3 = 1.2V	DDRPHY_VDDQ_4	K10
LPDDR4 = 1.1V	DDRPHY_VDDQ_5	L10
LPDDR4x = 0.6V	DDRPHY_VDDQ_6	M10

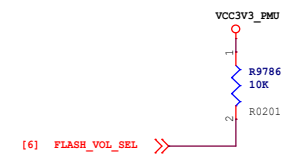
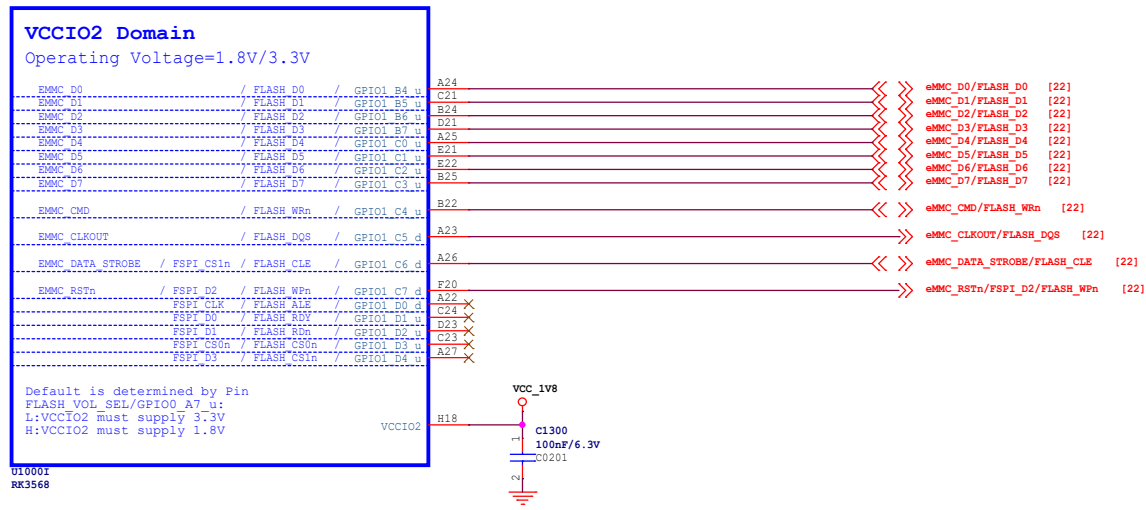
Note: Except DDR3, other DQ sequences can not be swap



RK3568_G (OSC/PLL/PMUIO1/2)

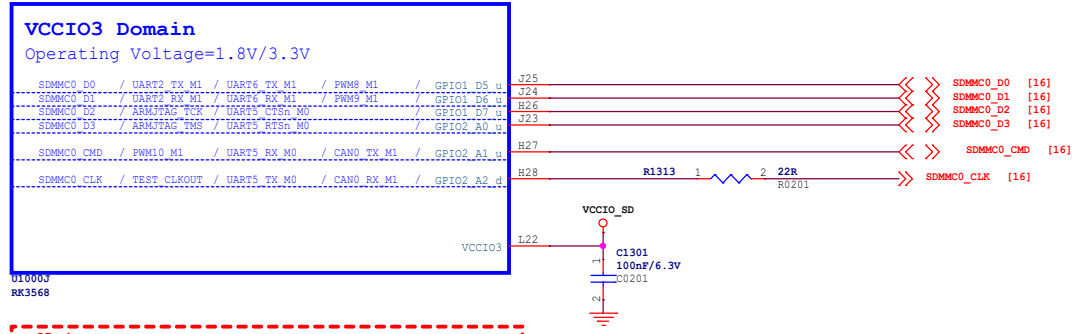


RK3568_I (VCCIO2 Domain)



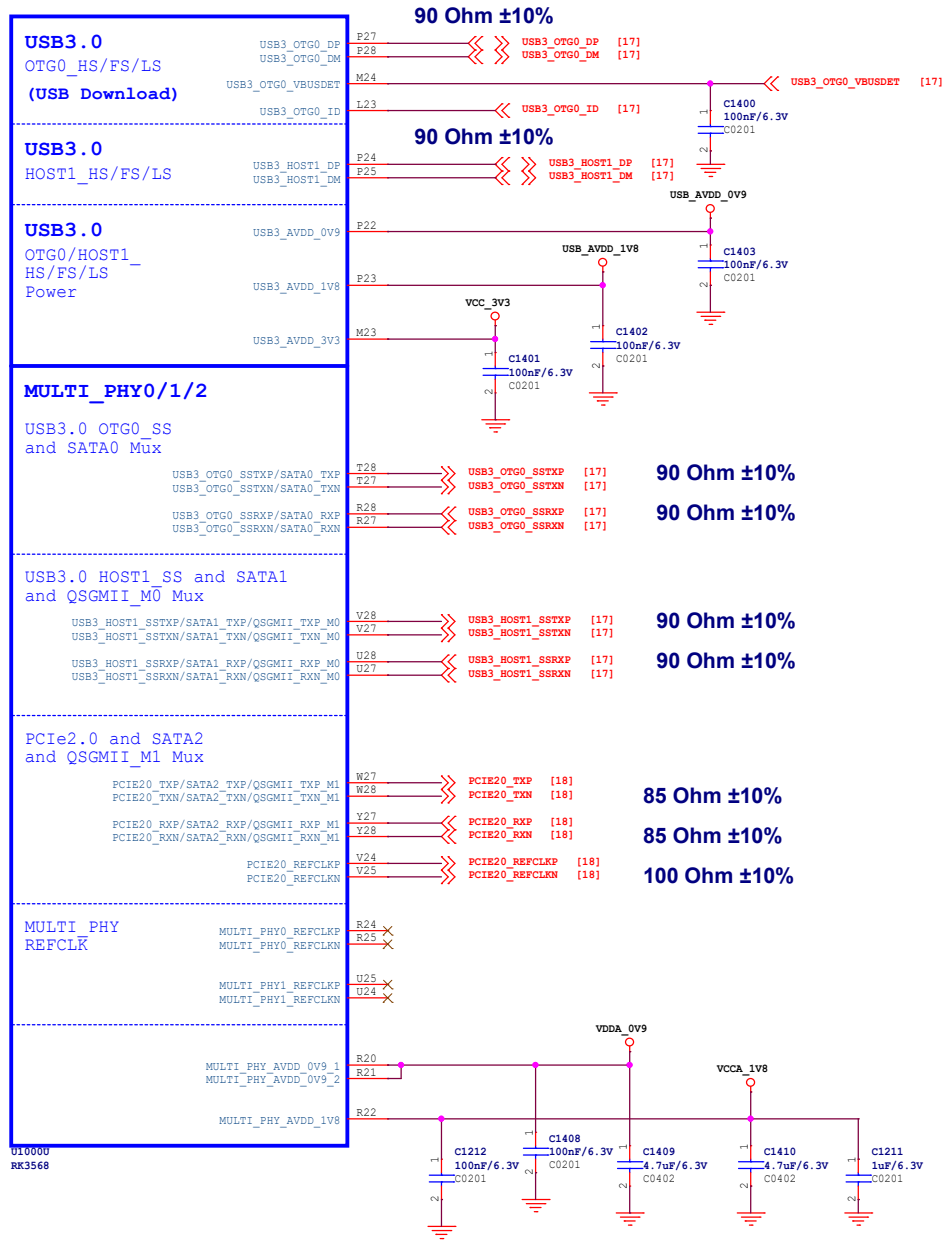
Note:
FLASH VOL_SEL state decided to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

RK3568_J (VCCIO3 Domain)



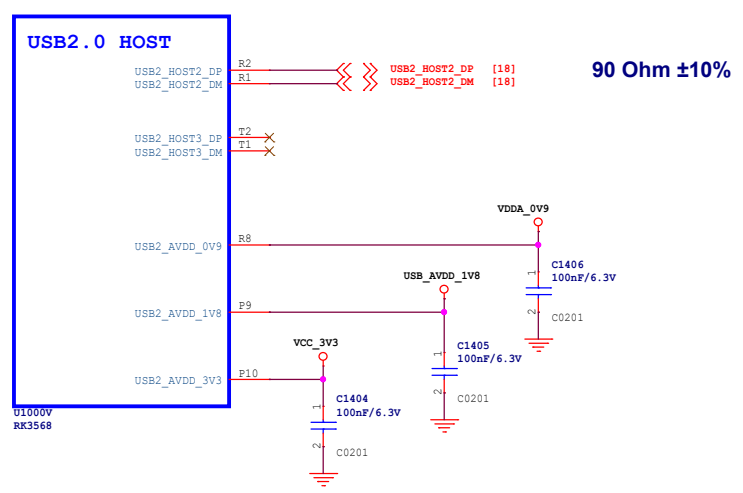
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_U (USB3.0/SATA/QSGMII/PCIE2.0 x1)

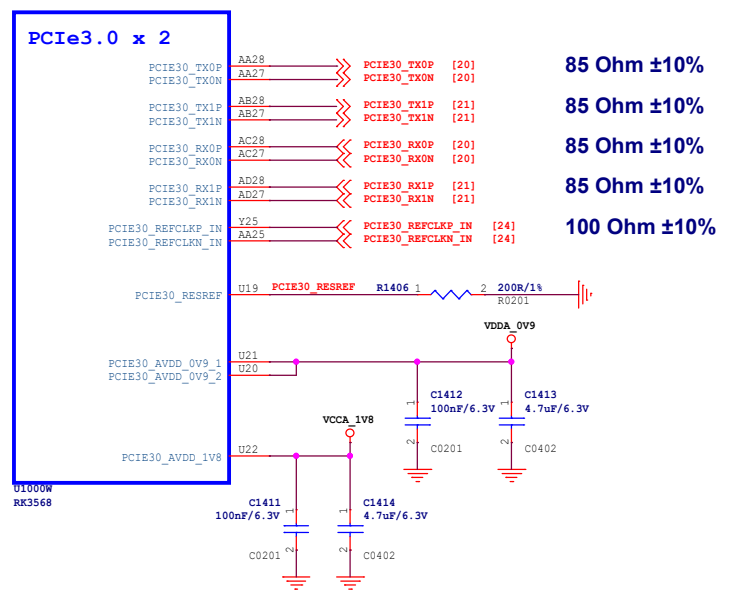


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

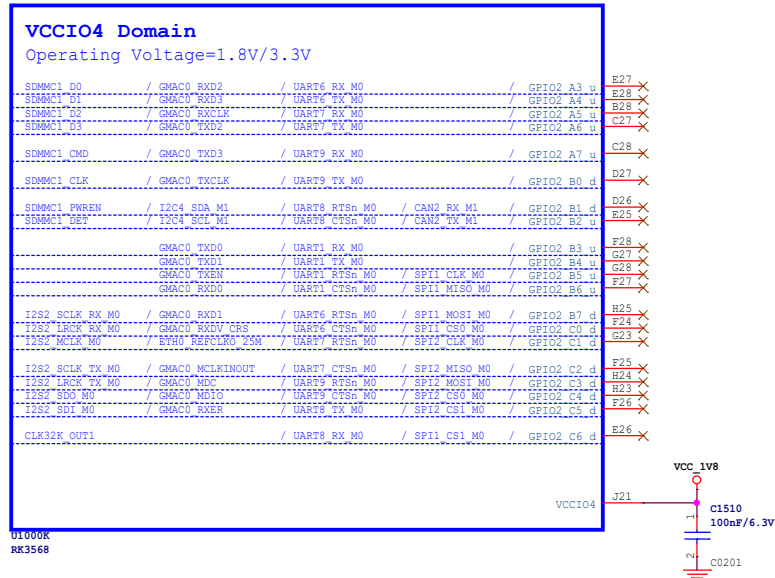
RK3568_V (USB2.0 HOST)



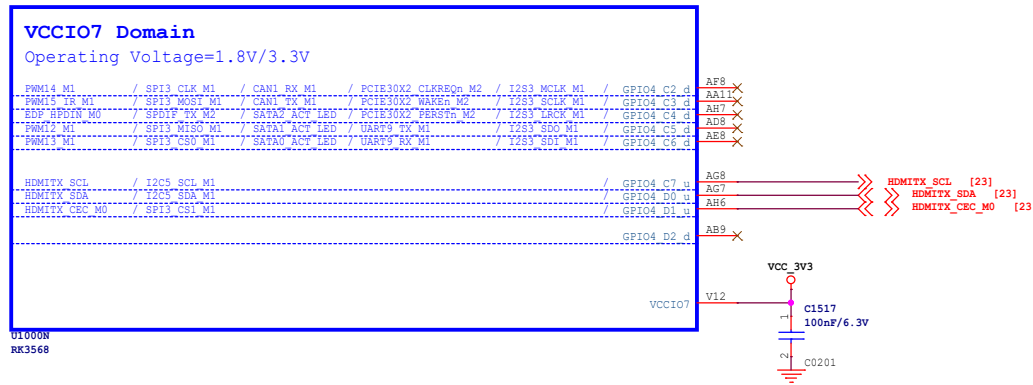
RK3568_W (PCIe3.0 x2)



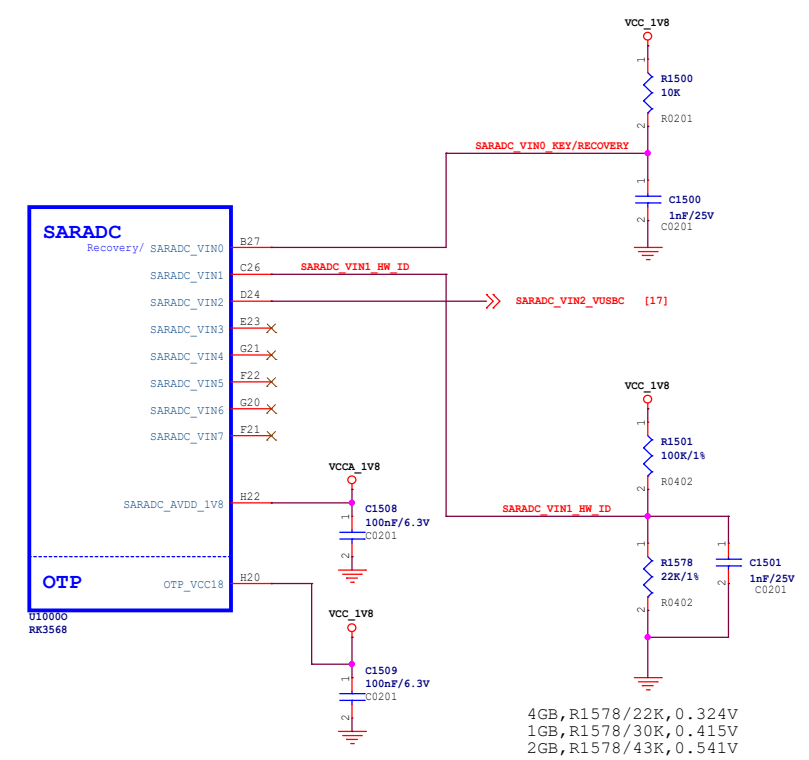
RK3568_K (VCCIO4 Domain)



RK3568_N (VCCIO7 Domain)

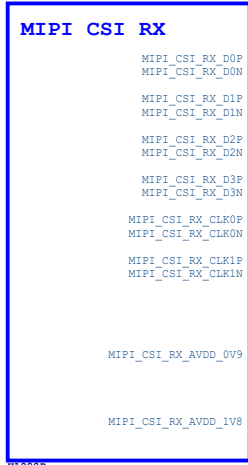


RK3568_O (SARADC/OTP)

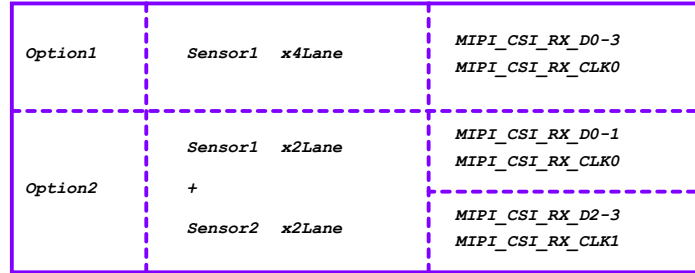


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_P (MIPI_CSI_RX)

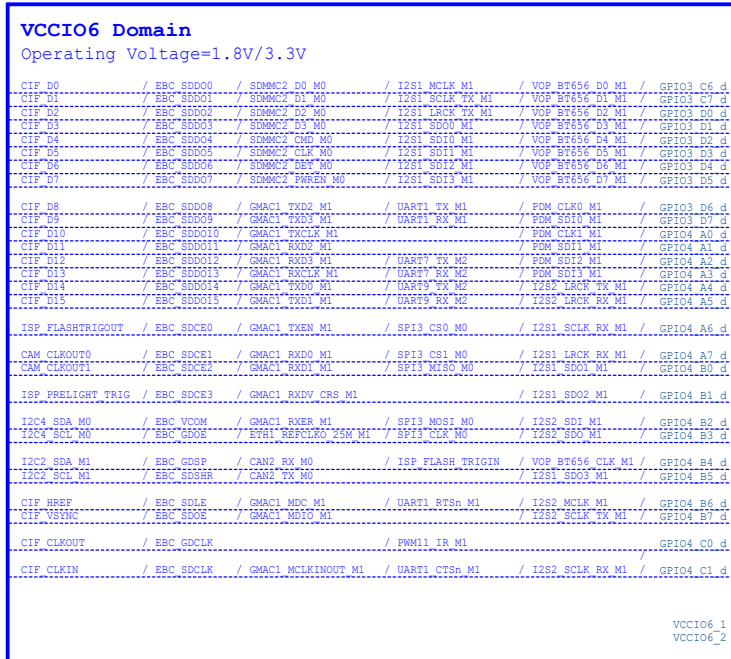


MIPI_CSI_RX
100 Ohm ±10%

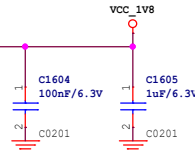


U1000P
RK3568

RK3568_M (VCCIO6 Domain)



U1000M
RK3568



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

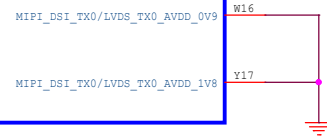
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_R (MIPI_DSI_TX0/LVDS_TX0)

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P AH17
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N AG17
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P AH16
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N AG16
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P AH14
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N AG14
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P AH13
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N AG13
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP AH15
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN AG15

MIPI_DSI_TX0/LVDS_TX0
100 Ohm ±10%



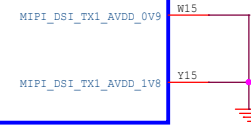
U1000R
RK3568

RK3568_S (MIPI_DSI_TX1)

MIPI DSI TX1

MIPI_DSI_TX1_D0P AD18
MIPI_DSI_TX1_D0N AB18
MIPI_DSI_TX1_D1P AD17
MIPI_DSI_TX1_D1N AC17
MIPI_DSI_TX1_D2P AD14
MIPI_DSI_TX1_D2N AC14
MIPI_DSI_TX1_D3P AD12
MIPI_DSI_TX1_D3N AB12
MIPI_DSI_TX1_CLKP AD15
MIPI_DSI_TX1_CLKN AB15

MIPI_DSI_TX1
100 Ohm ±10%

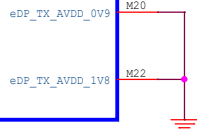


U1000S
RK3568

RK3568_T (eDP TX)

eDP_TX

eDP_TX_D0P J28
eDP_TX_D0N K27
eDP_TX_D1P K28
eDP_TX_D1N L27
eDP_TX_D2P L28
eDP_TX_D2N M27
eDP_TX_D3P M28
eDP_TX_D3N N27
eDP_TX_AUXP L25
eDP_TX_AUXN M25



U1000T
RK3568

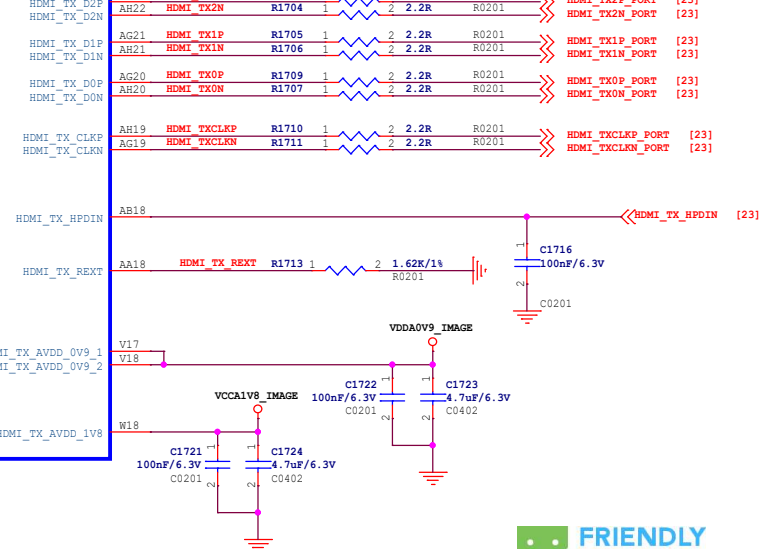
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q (HDMI2.0 TX)

HDMI2.0 TX

HDMI TMDs trace
100 Ohm ±10%



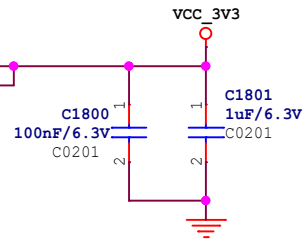
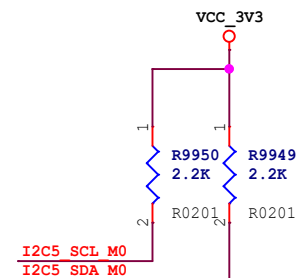
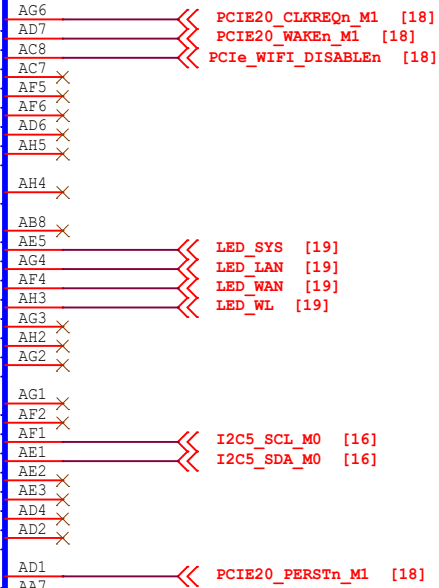
U1000Q
RK3568

RK3568_L (VCCIO5 Domain)

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREOn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREOn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREOn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 D5	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D6	/ GMAC1 RXCLK M0	/ I2S3 SDI M0	/ SDMMC2 DET M1	/ GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0	/ I2S3 SDI M0	/ SDMMC2 PWREN M1	/ GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d



U1000L
RK3568

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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Size A4	Page Name 12.RK3568_VO Interface_2	
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RK3568_H (VCCIO1 Domain)

VCCIO1 Domain

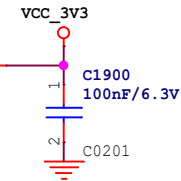
Operating Voltage=1.8V/3.3V

I2C3 SDA M0	/	UART3 RX M0	/	CAN1 RX M0	/	AUDIOPWM LOUT P	/	ACODEC ADC DATA	/	GPI01 A0 u	D18
I2C3 SCL M0	/	UART3 TX M0	/	CAN1 TX M0	/	AUDIOPWM LOUT N	/	ACODEC ADC CLK	/	GPI01 A1 u	E18
I2S1 MCLK M0	/	UART3 RTSn M0	/	SCR CLK	/	PCIE30X1 PERSTn M2	/		/	GPI01 A2 d	A19
I2S1 SCLK TX M0	/	UART3 CTSn M0	/	SCR IO	/	PCIE30X1 WAKEn M2	/	ACODEC DAC CLK	/	GPI01 A3 d	B19
I2S1 SCLK RX M0	/	UART4 RX M0	/	PDM CLK1 M0	/	SPDIF TX M0	/		/	GPI01 A4 d	F18
I2S1 LRCK TX M0	/	UART4 RTSn M0	/	SCR RST	/	PCIE30X1 CLKREOn M2	/	ACODEC DAC SYNC	/	GPI01 A5 d	A20
I2S1 LRCK RX M0	/	UART4 TX M0	/	PDM CLK0 M0	/	AUDIOPWM ROUT P	/		/	GPI01 A6 d	C20
I2S1 SDO0 M0	/	UART4 CTSn M0	/	SCR DET	/	AUDIOPWM ROUT N	/	ACODEC DAC DATAL	/	GPI01 A7 d	B20
I2S1 SDO1 M0	/	I2S1 SDI3 M0	/	PDM SDI3 M0	/	PCIE20 CLKREOn M2	/	ACODEC DAC DATAR	/	GPI01 B0 d	D20
I2S1 SDO2 M0	/	I2S1 SDI2 M0	/	PDM SDI2 M0	/	PCIE20 WAKEn M2	/	ACODEC ADC SYNC	/	GPI01 B1 d	E20
I2S1 SDO3 M0	/	I2S1 SDI1 M0	/	PDM SDI1 M0	/	PCIE20 PERSTn M2	/		/	GPI01 B2 d	A21
		I2S1 SDI0 M0	/	PDM SDI0 M0	/		/		/	GPI01 B3 d	B21

U1000H
RK3568

VCCIO1

D18
E18
A19
B19
F18
A20
C20
B20
D20
E20
A21
B21



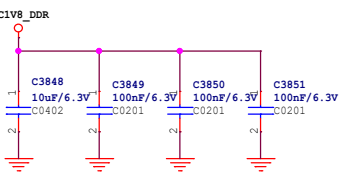
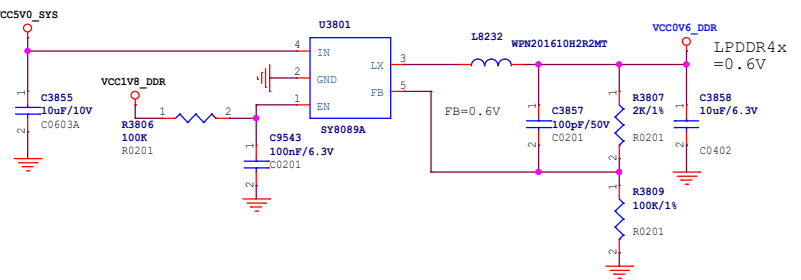
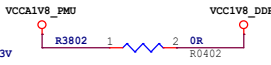
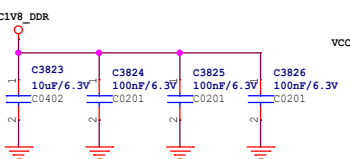
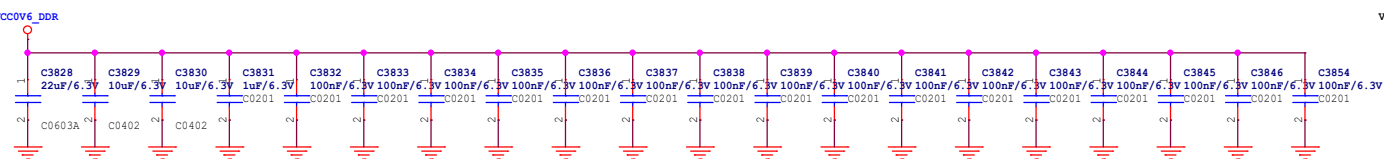
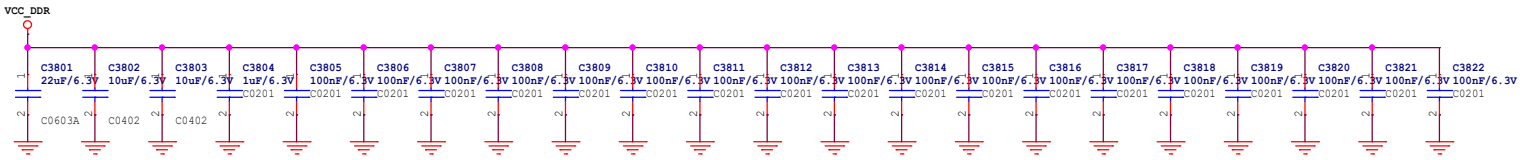
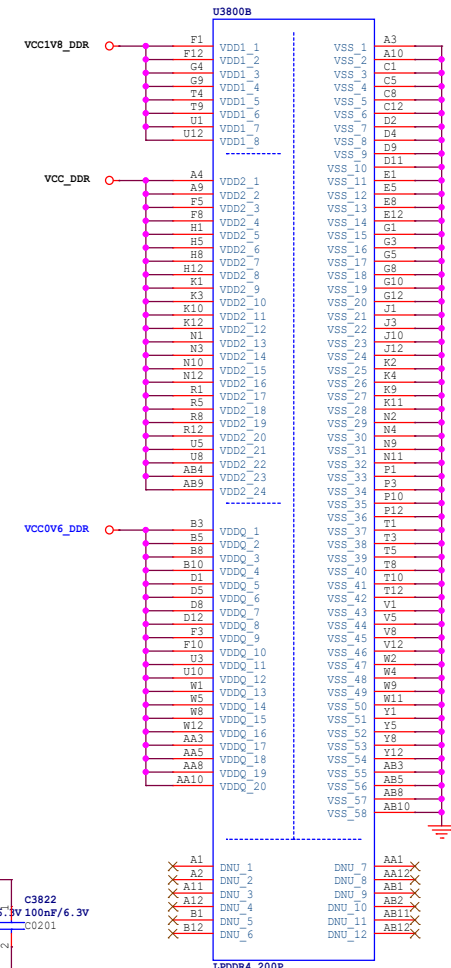
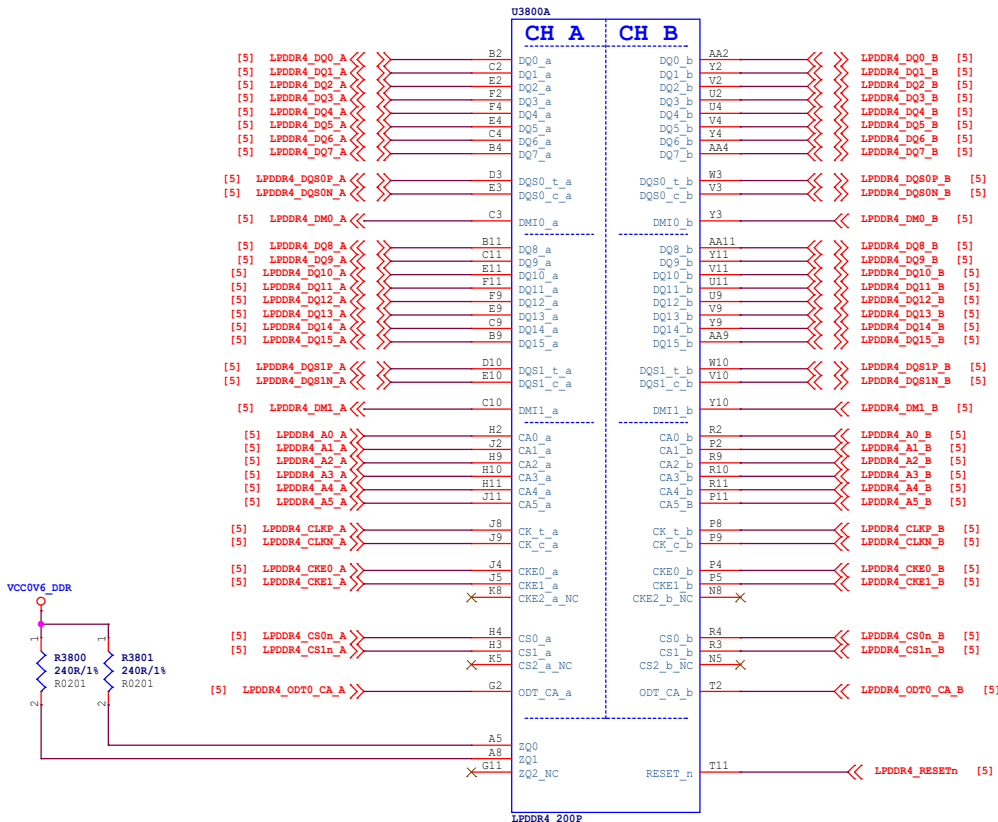
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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NanoPi R5C		Rev 2209
Size A4	Page Name 13.RK3568 Audio Interface	
Date: Thursday, November 17, 2024 Sheet: 13 / 24		



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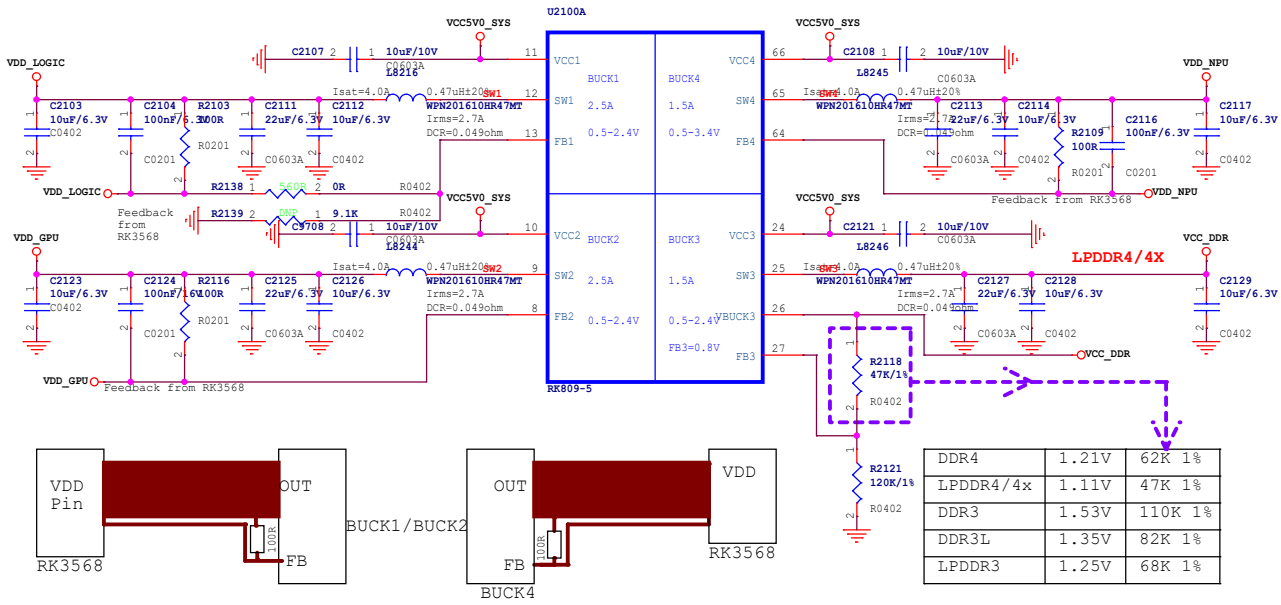
<https://www.friendlyelec.com/>
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NanoPi R5C

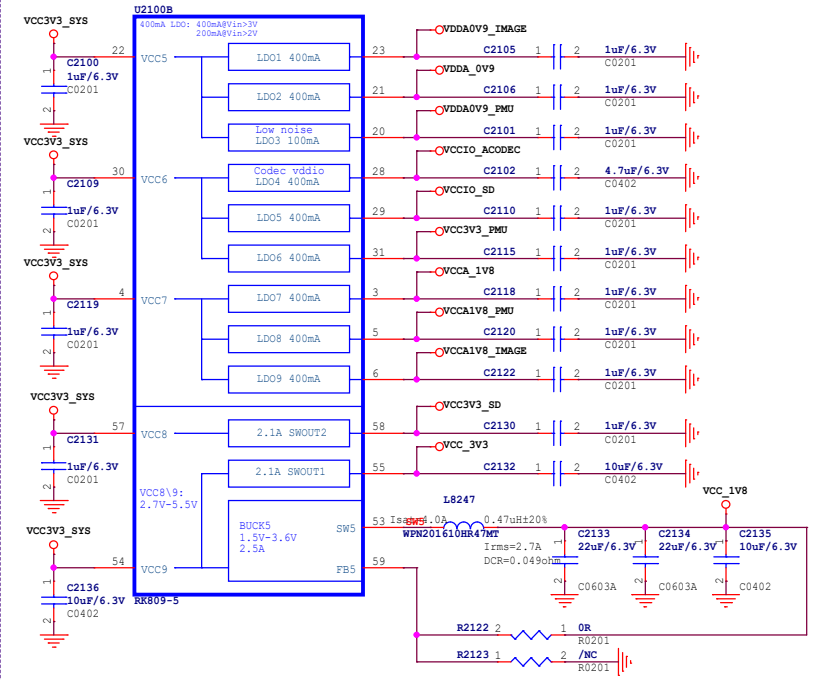
Size	Page Name	Rev
A3	14.DRAM-LPDDR4X_1X32bit_200P	2209

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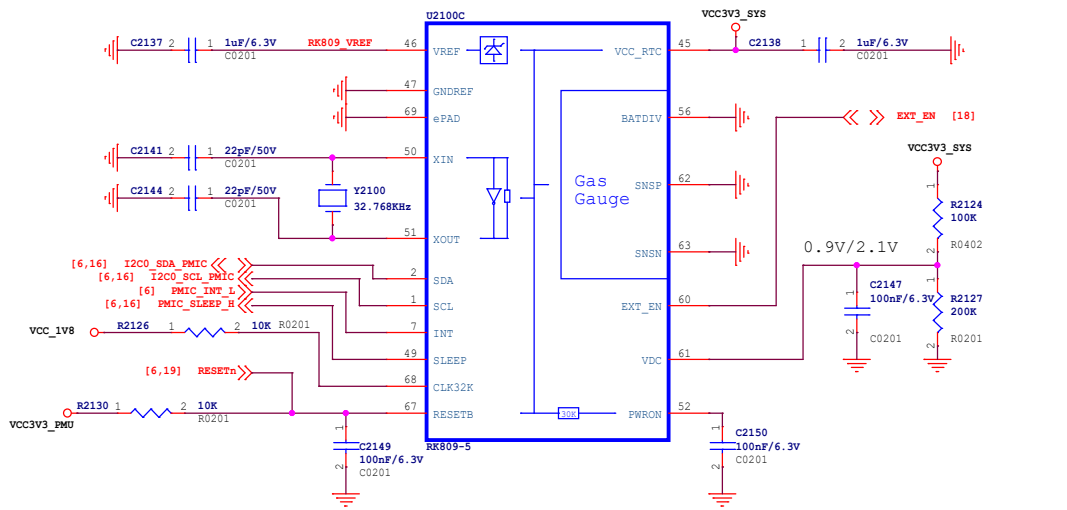
PMIC RK809 DCDC



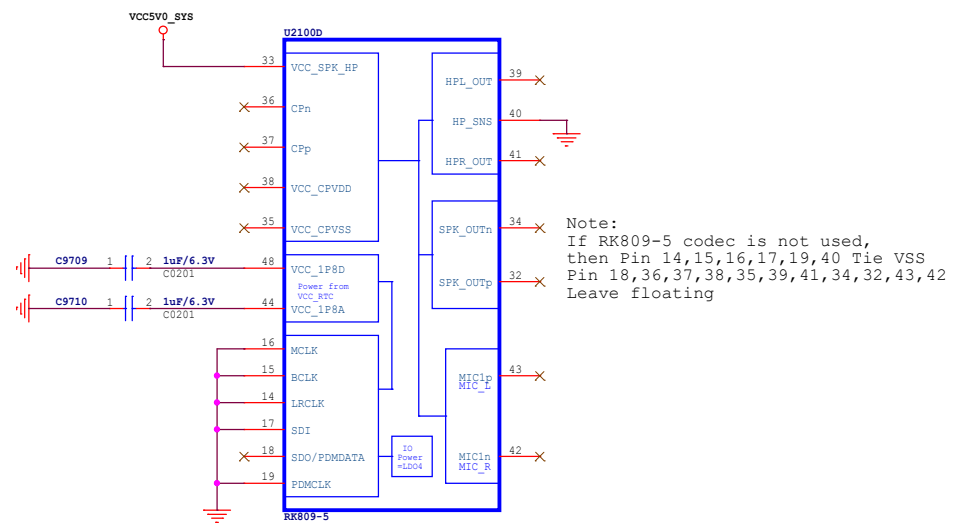
PMIC RK809 LDO



PMIC RK809 Management

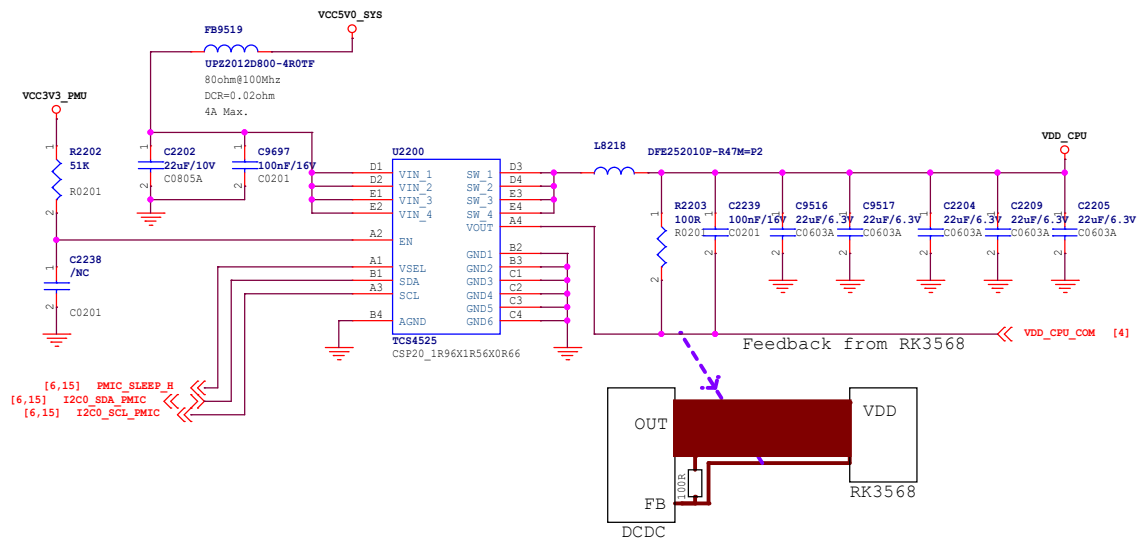


PMIC RK809 CODEC



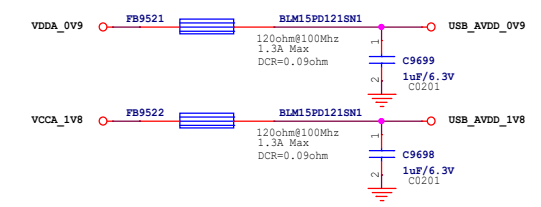
Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

VDD_CPU

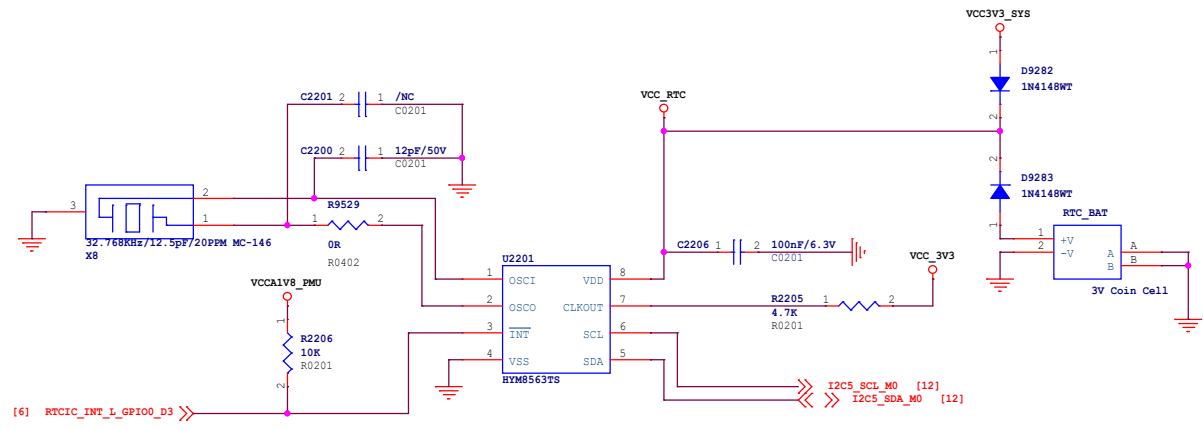


[6,15] PMIC_SLEEP_H
 [6,15] I2C0_SDA_PMIC
 [6,15] I2C0_SCL_PMIC

VDD_USB

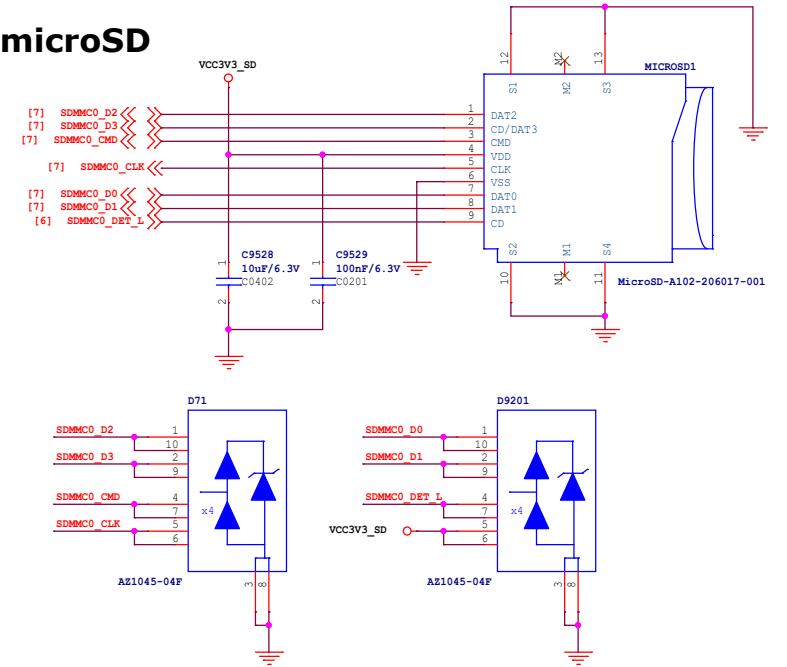


RTC

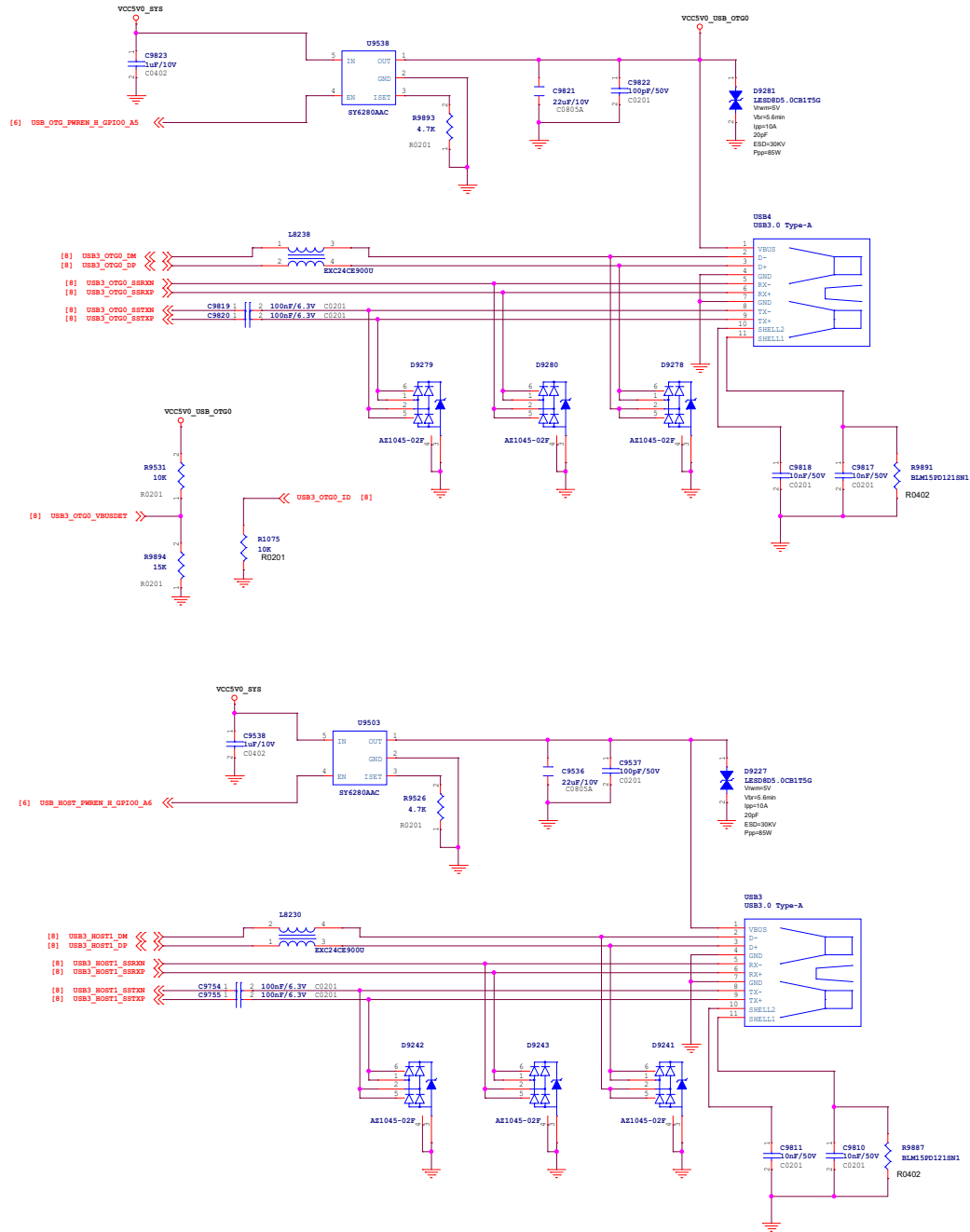


Address:Read A3H, Write A2H
 7bit address: 0x51

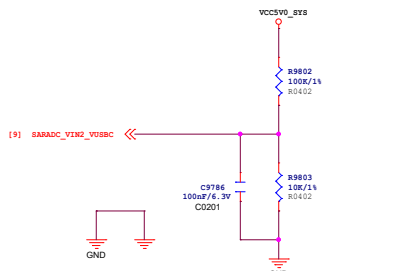
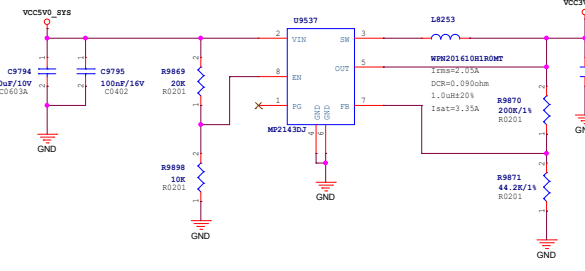
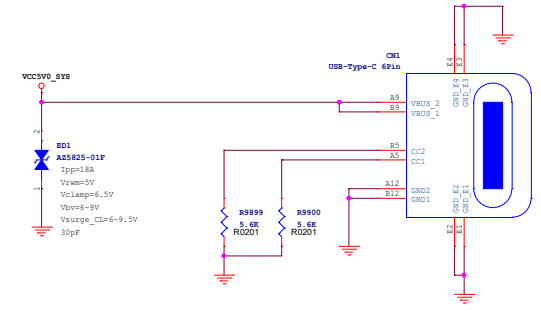
microSD



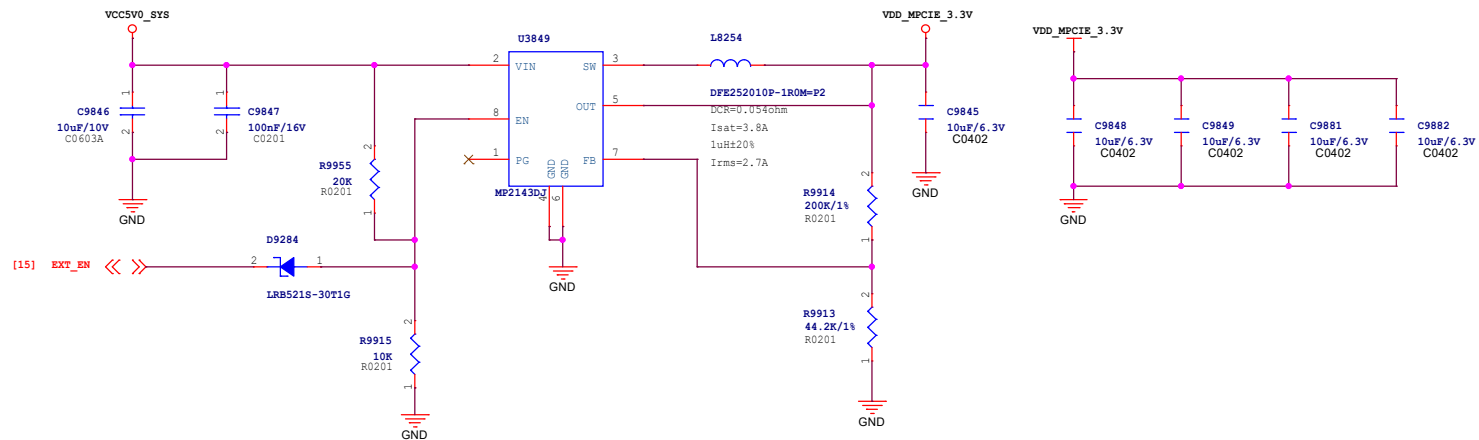
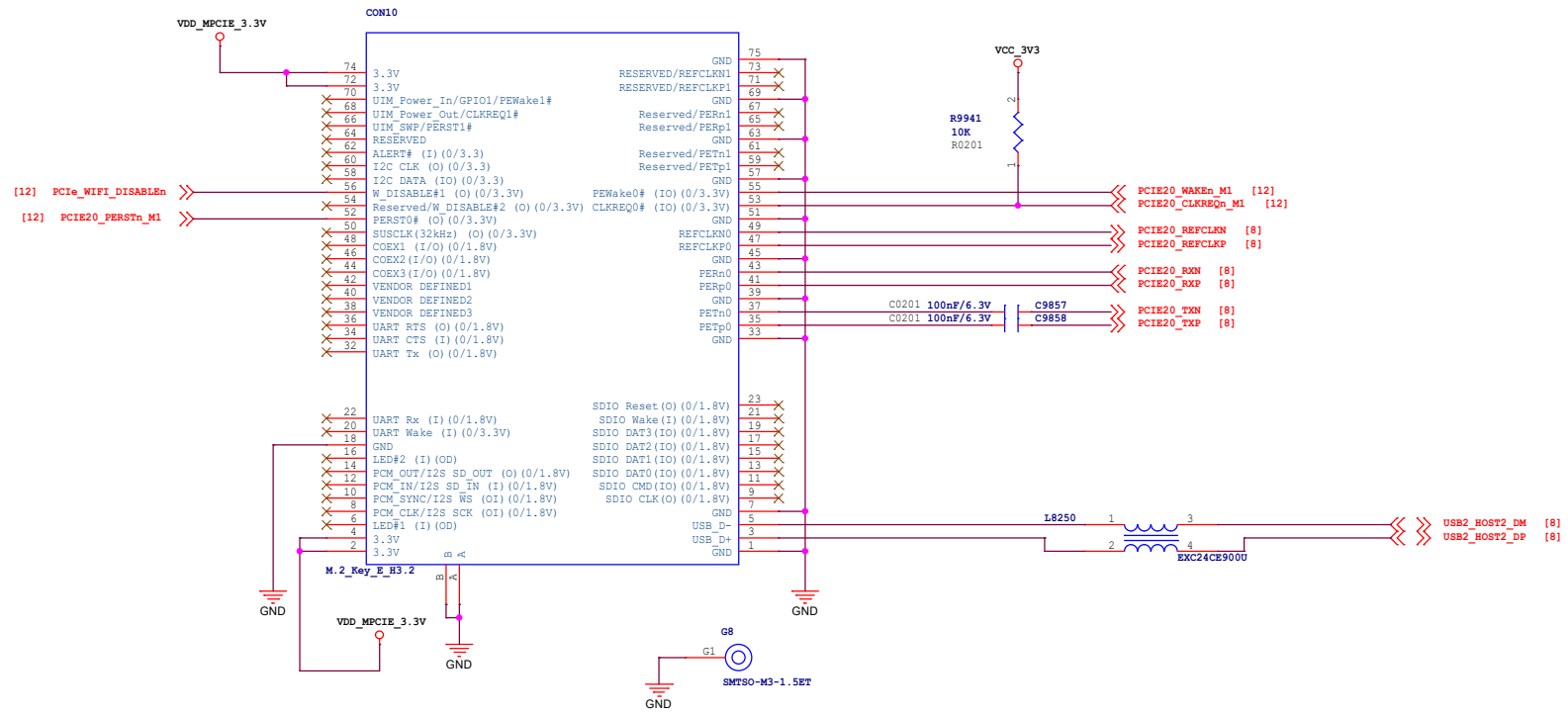
USB 3.0/ADB/MASK



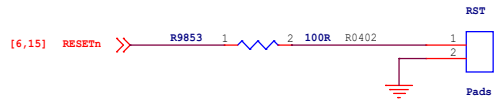
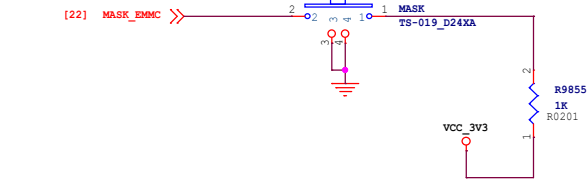
Power IN



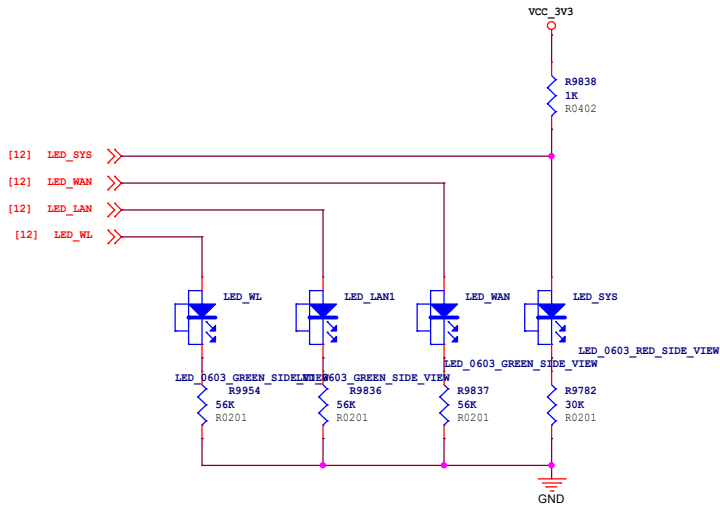
M.2 Key E 2230



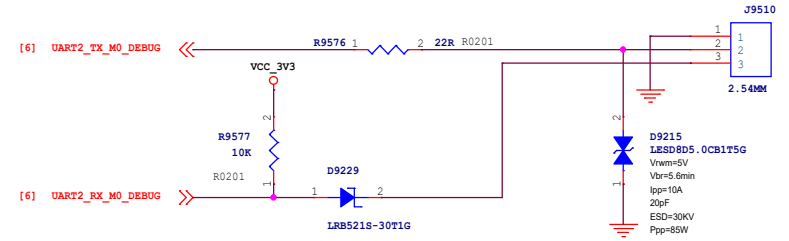
MASK Button



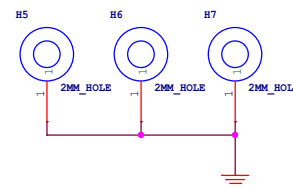
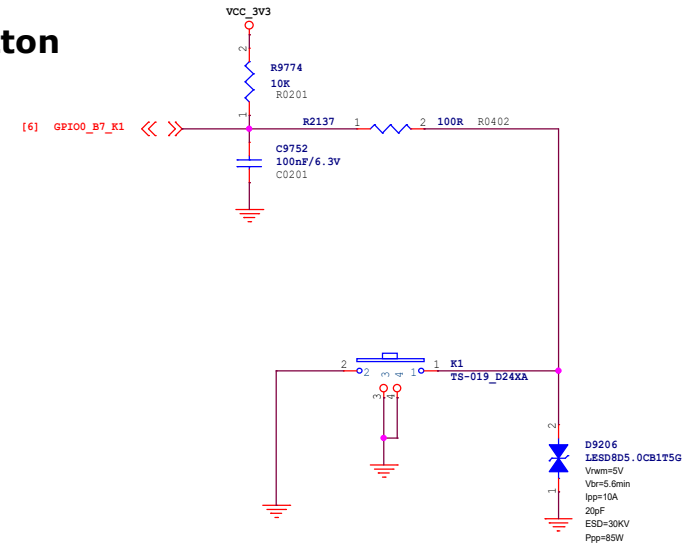
LED



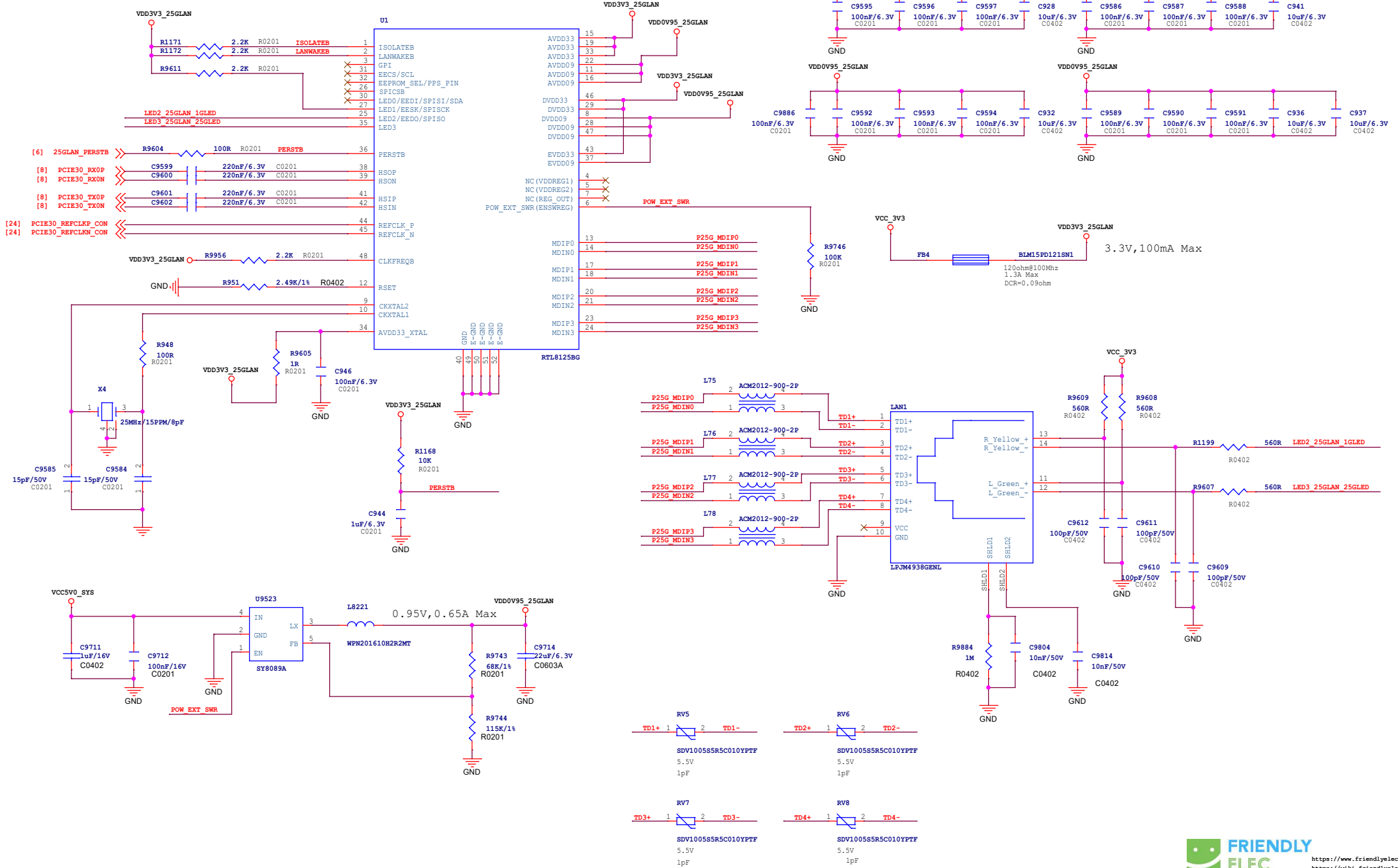
Debug UART



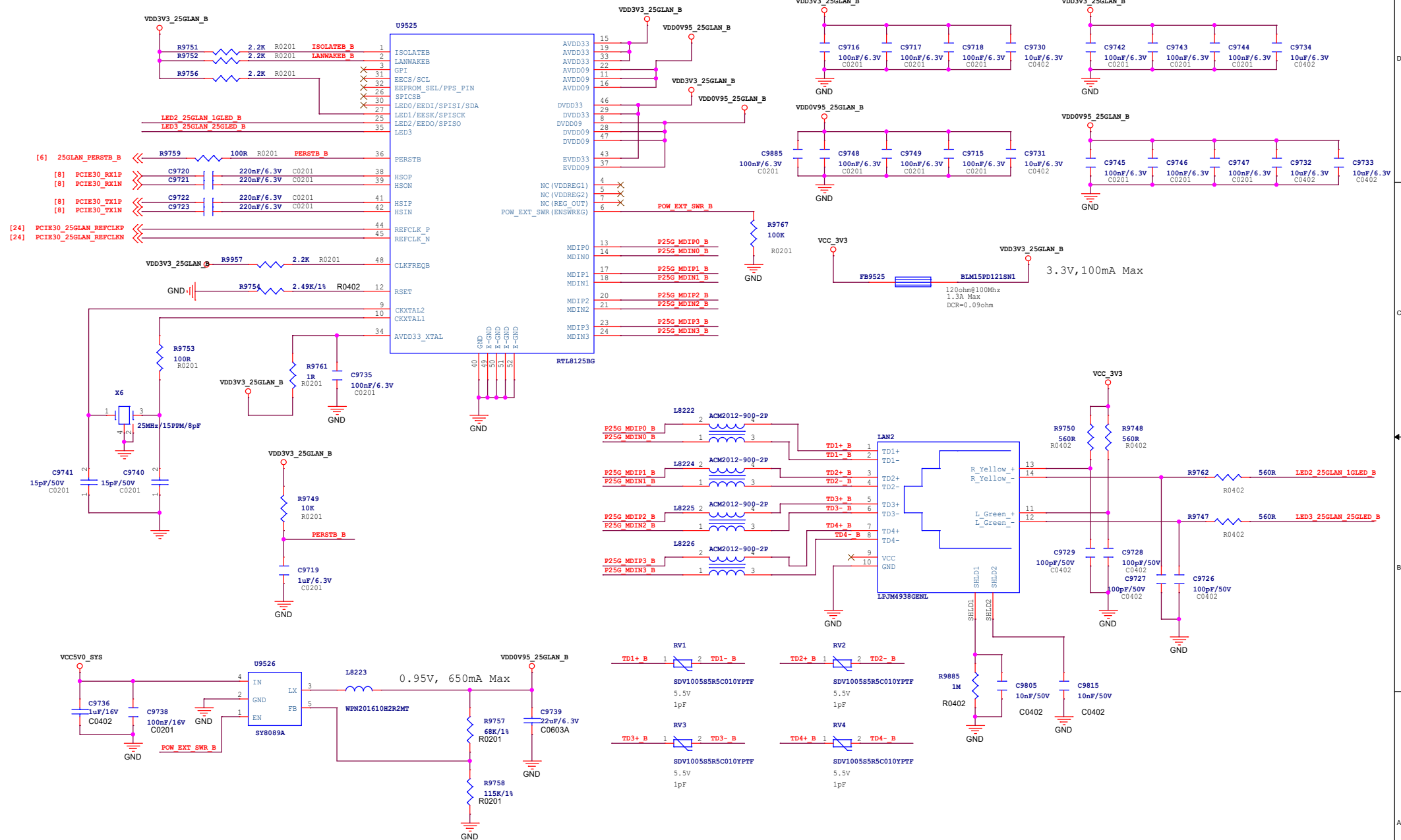
User Button



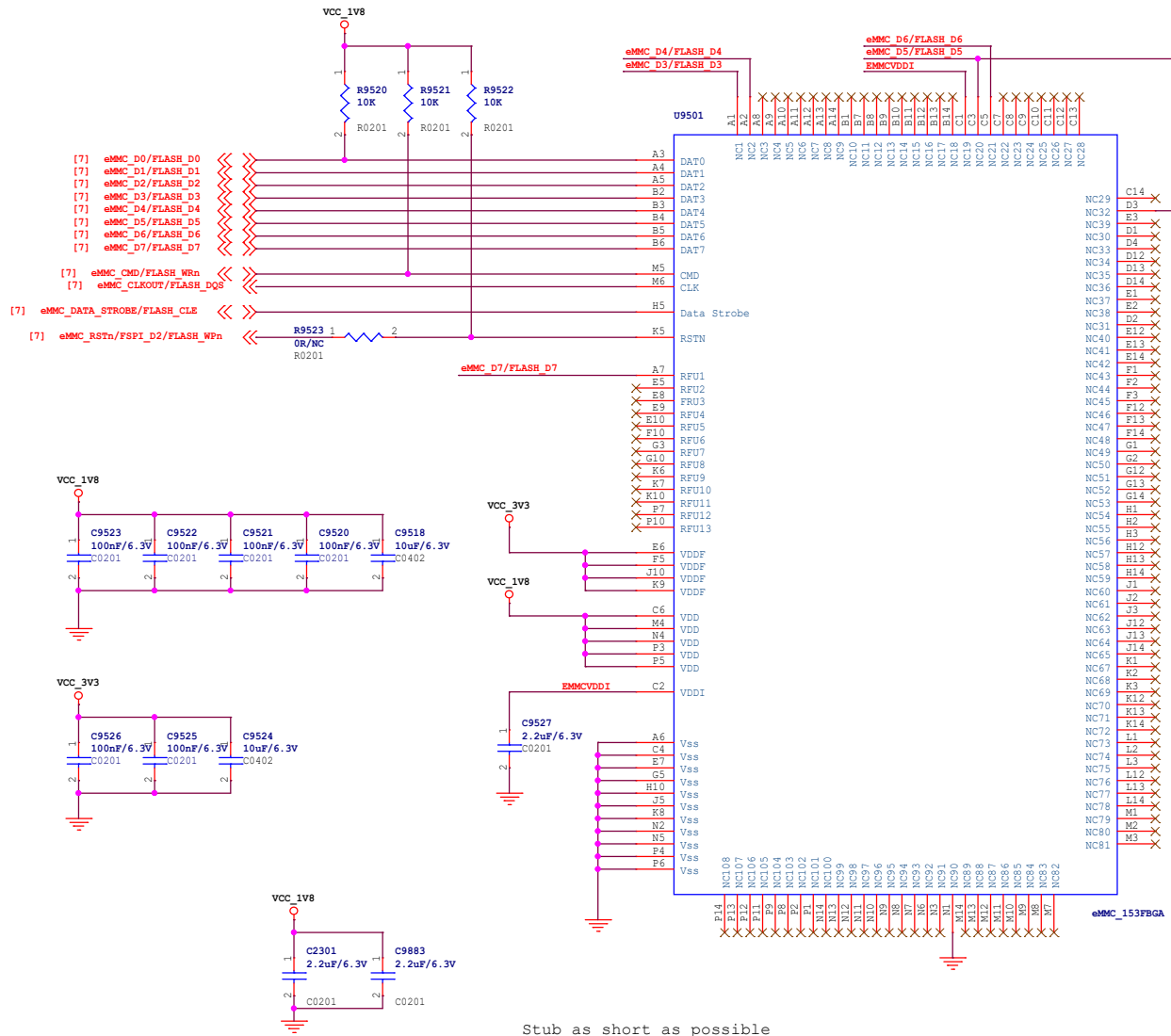
2.5Gbps Ethernet



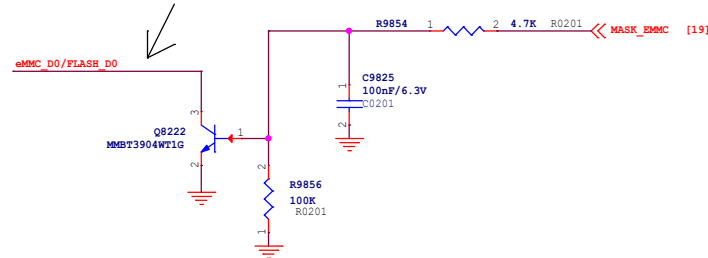
2.5Gbps Ethernet



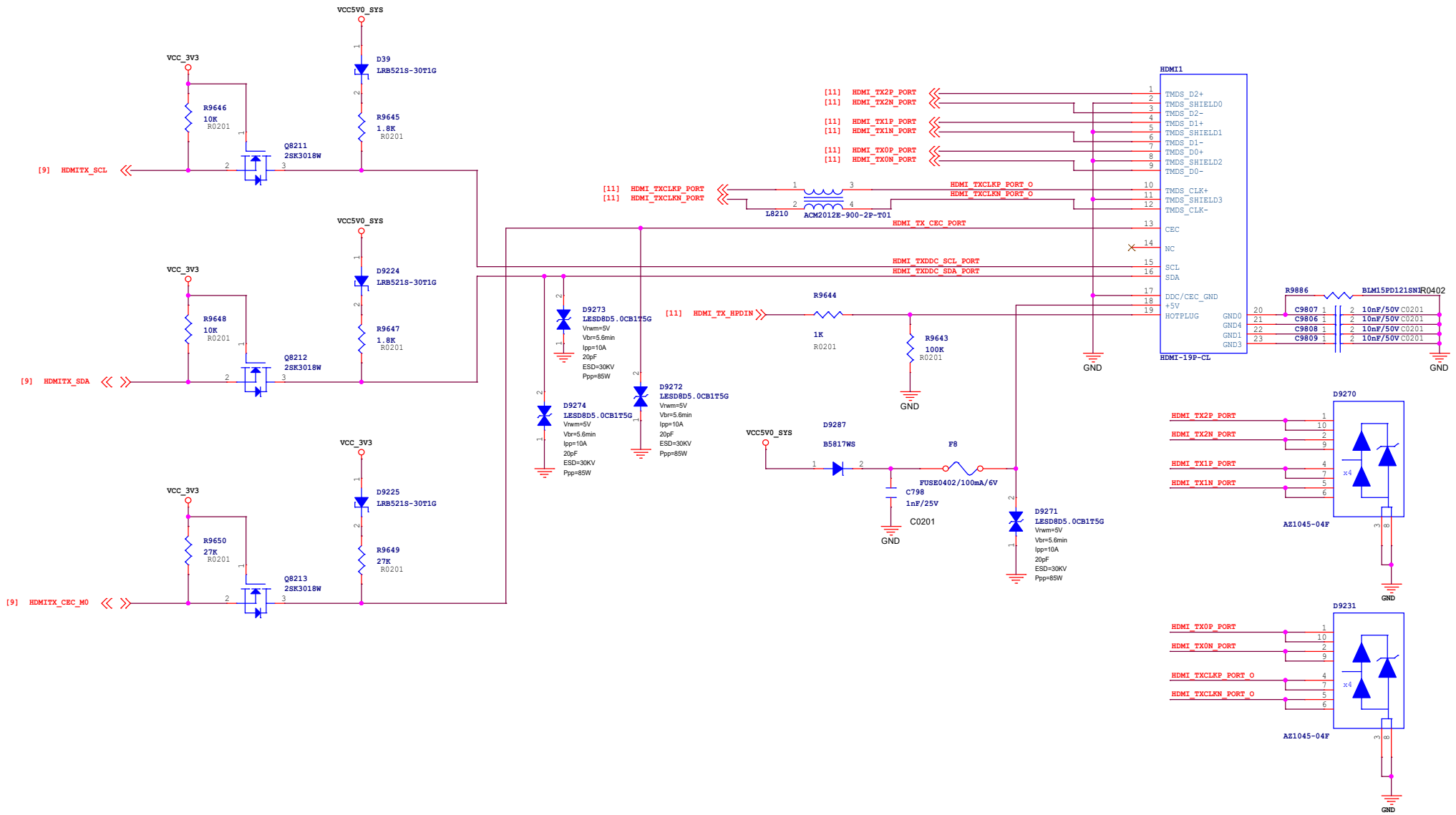
eMMC



Stub as short as possible



HDMI 2.0 TX



PCIe REFCLK

