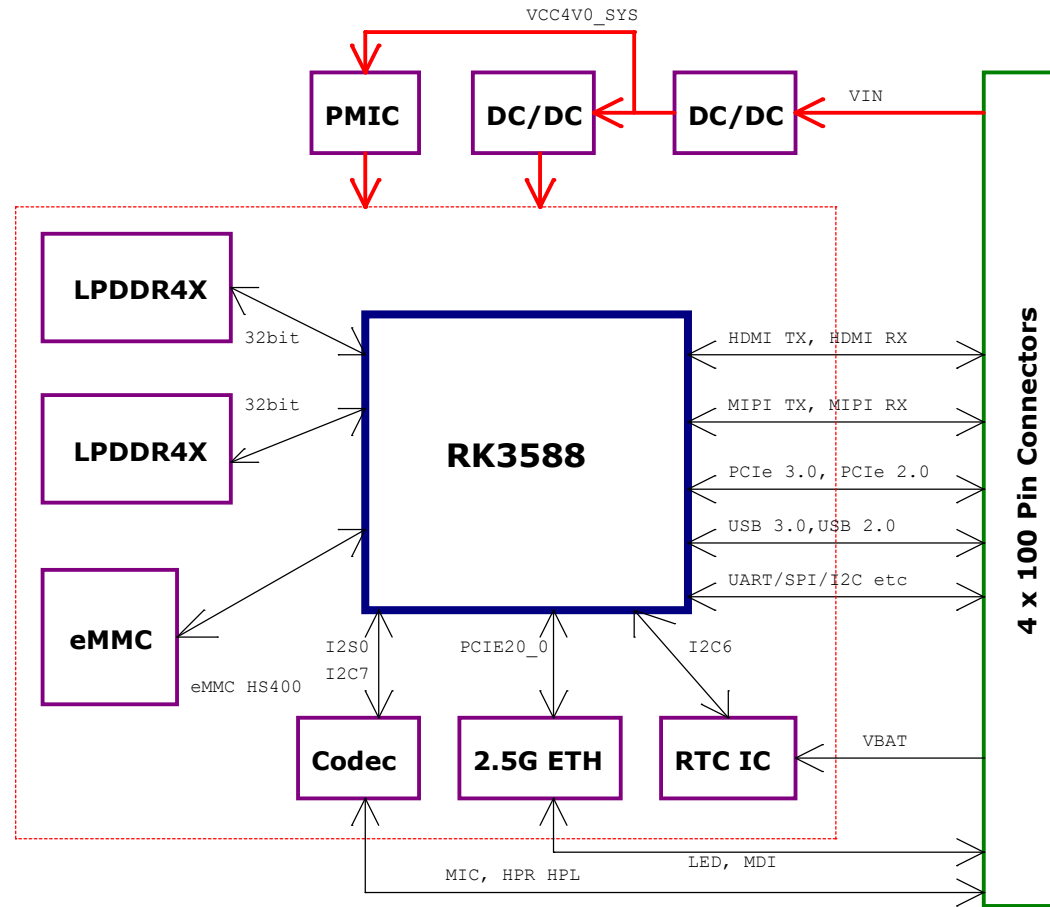
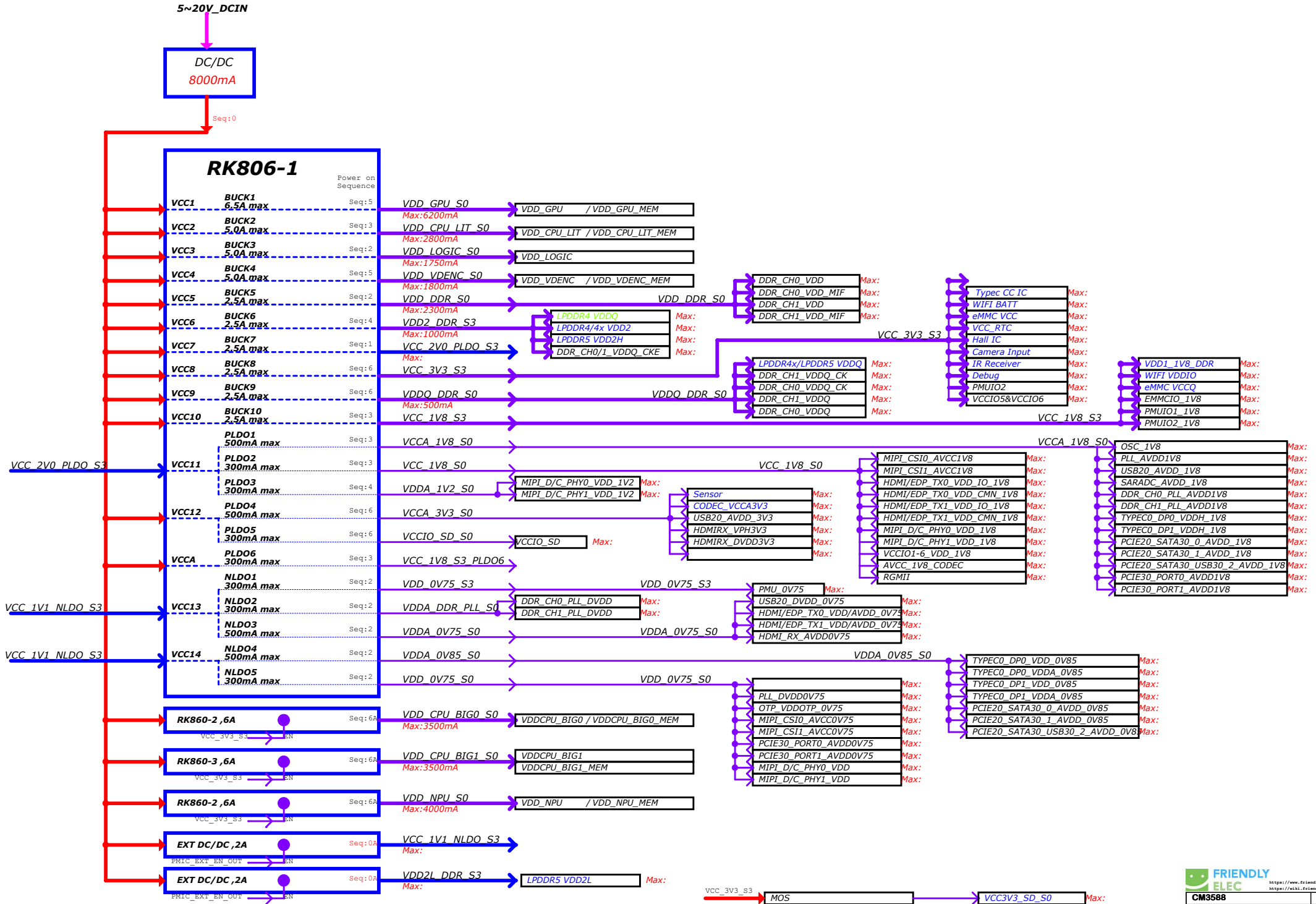


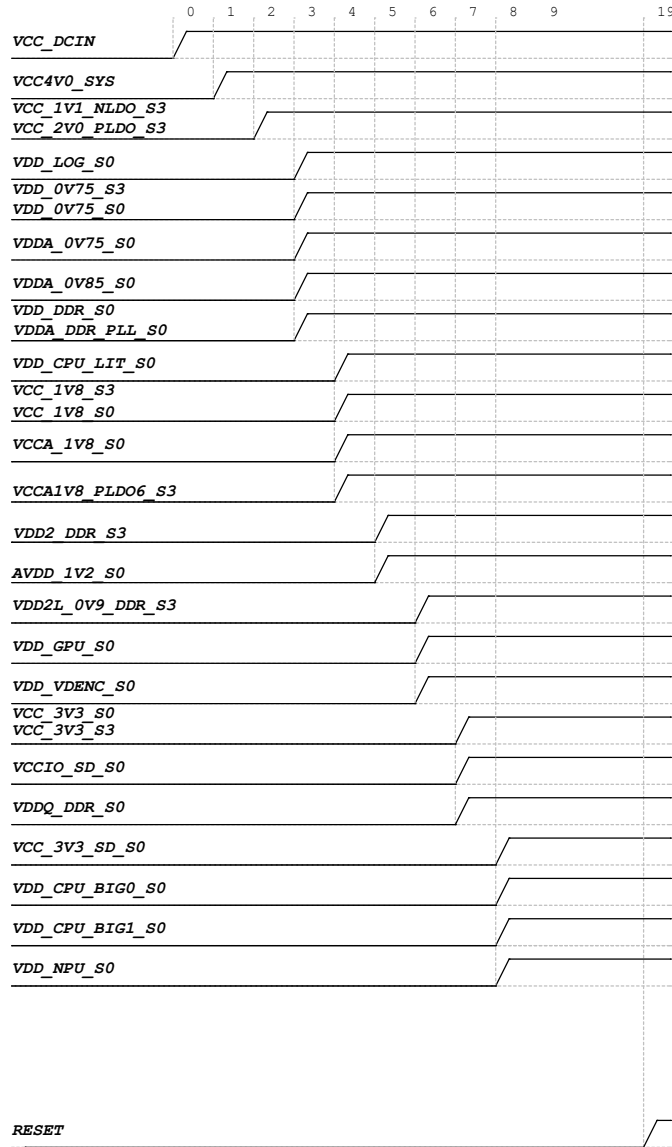
CM3588



Power Tree



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_OV75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_OV75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_OV85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_OV75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_OV9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD

IO Power Domain Map

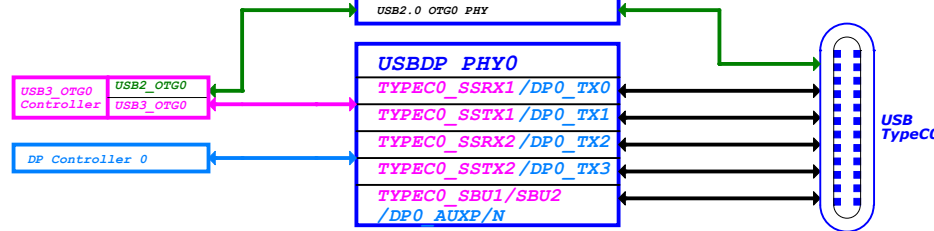
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_3V3_S3	3.3V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

USB Controller Configure Table

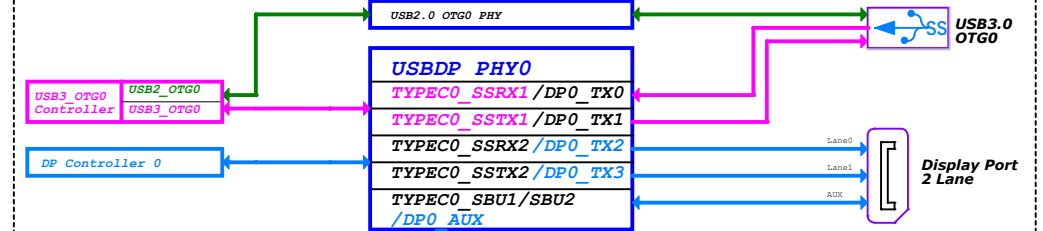
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB3.0 OTG+DPx2Lane Function		USB2.0 OTG+DPx2Lane Function		USB2.0 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB3.0 OTG Device or Host	TYPEC0_SBU1/DP0_AUXP	TYPEC0_SBU1	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN
	TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU2	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN	DP0_AUXP	DP0_AUXN
	TYPEC0_SSRX1/DP0_TX0	TYPEC0_SSRX1P	DP0_TX0P	DP0_TX0N	TYPEC0_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0N	DP0_TX0P	DP0_TX0N
USB2.0 OTG Device or Host	TYPEC0_SSTX1/DP0_TX1	TYPEC0_SSTX1P	DP0_TX1P	DP0_TX1N	TYPEC0_SSTX1P	DP0_TX1P	DP0_TX1P	DP0_TX1N	DP0_TX1P	DP0_TX1N
	TYPEC0_SSRX2/DP0_TX2	TYPEC0_SSRX2P	DP0_TX2P	DP0_TX2N	TYPEC0_SSRX2P	DP0_TX2P	DP0_TX2P	DP0_TX2N	DP0_TX2P	DP0_TX2N
	TYPEC0_SSTX2/DP0_TX3	TYPEC0_SSTX2P	DP0_TX3P	DP0_TX3N	TYPEC0_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3N	DP0_TX3P	DP0_TX3N
USB3.0 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP	TYPEC1_SBU1	DP1_AUXP	DP1_AUXN	TYPEC1_SBU1	DP1_AUXP	DP1_AUXP	DP1_AUXN	TYPEC1_SBU1	DP1_AUXP
	TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU2	DP1_AUXP	DP1_AUXN	TYPEC1_SBU2	DP1_AUXP	DP1_AUXP	DP1_AUXN	TYPEC1_SBU2	DP1_AUXP
	TYPEC1_SSRX1/DP1_TX0	TYPEC1_SSRX1P	DP1_TX0P	DP1_TX0N	TYPEC1_SSRX1P	DP1_TX0P	DP1_TX0P	DP1_TX0N	TYPEC1_SSRX1	DP1_TX0P
USB2.0 OTG1 Device or Host	TYPEC1_SSTX1/DP1_TX1	TYPEC1_SSTX1P	DP1_TX1P	DP1_TX1N	TYPEC1_SSTX1P	DP1_TX1P	DP1_TX1P	DP1_TX1N	TYPEC1_SSTX1	DP1_TX1P
	TYPEC1_SSRX2/DP1_TX2	TYPEC1_SSRX2P	DP1_TX2P	DP1_TX2N	TYPEC1_SSRX2P	DP1_TX2P	DP1_TX2P	DP1_TX2N	TYPEC1_SSRX2	DP1_TX2P
	TYPEC1_SSTX2/DP1_TX3	TYPEC1_SSTX2P	DP1_TX3P	DP1_TX3N	TYPEC1_SSTX2P	DP1_TX3P	TYPEC1_SSTX2P	DP1_TX3N	TYPEC1_SSTX2	DP1_TX3P
USB3.0 HOST2	PCIE2_2_TXP/SATA3_2_TXP/USB3_2_SSRXP		OPTION1 USB3.0 HOST	OPTION2 USB3.0 HOST	OPTION3 USB3.0 HOST					
	PCIE2_2_RXN/SATA3_2_RXN/USB3_2_SSTXP		OPTION1 USB3.0 HOST	OPTION2 USB3.0 HOST	OPTION3 USB3.0 HOST					
USB2.0 HOST0	USB2.0_HOST0_DP/USB2.0_HOST0_DM		OPTION1 USB2.0 HOST0_DP/USB2.0_HOST0_DM							
USB2.0 HOST1	USB2.0_HOST1_DP/USB2.0_HOST1_DM			OPTION2 USB2.0 HOST1_DP/USB2.0_HOST1_DM						

Note:
 0: Lane swap enable
 1: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
 1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1-TXDP/N

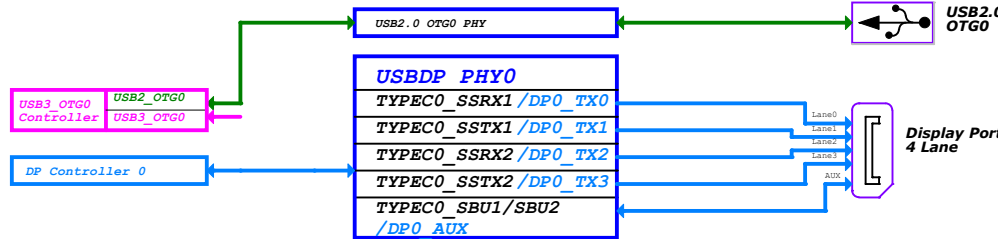
Config0:
TypeC0 (With DP function)



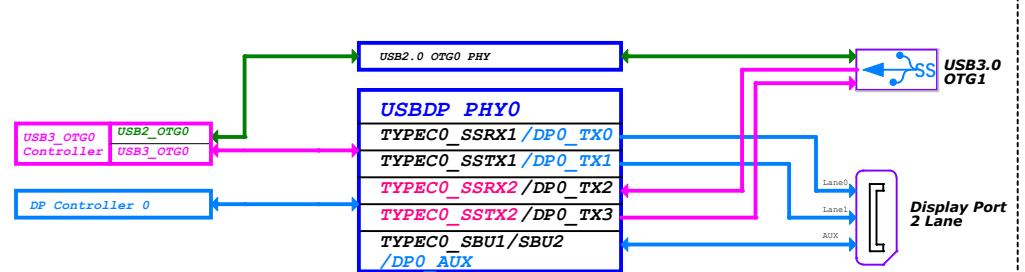
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



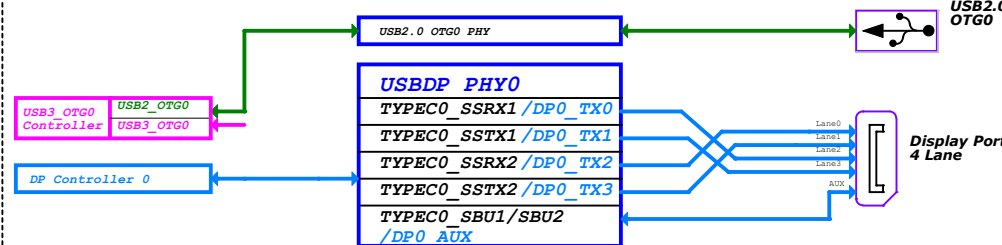
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



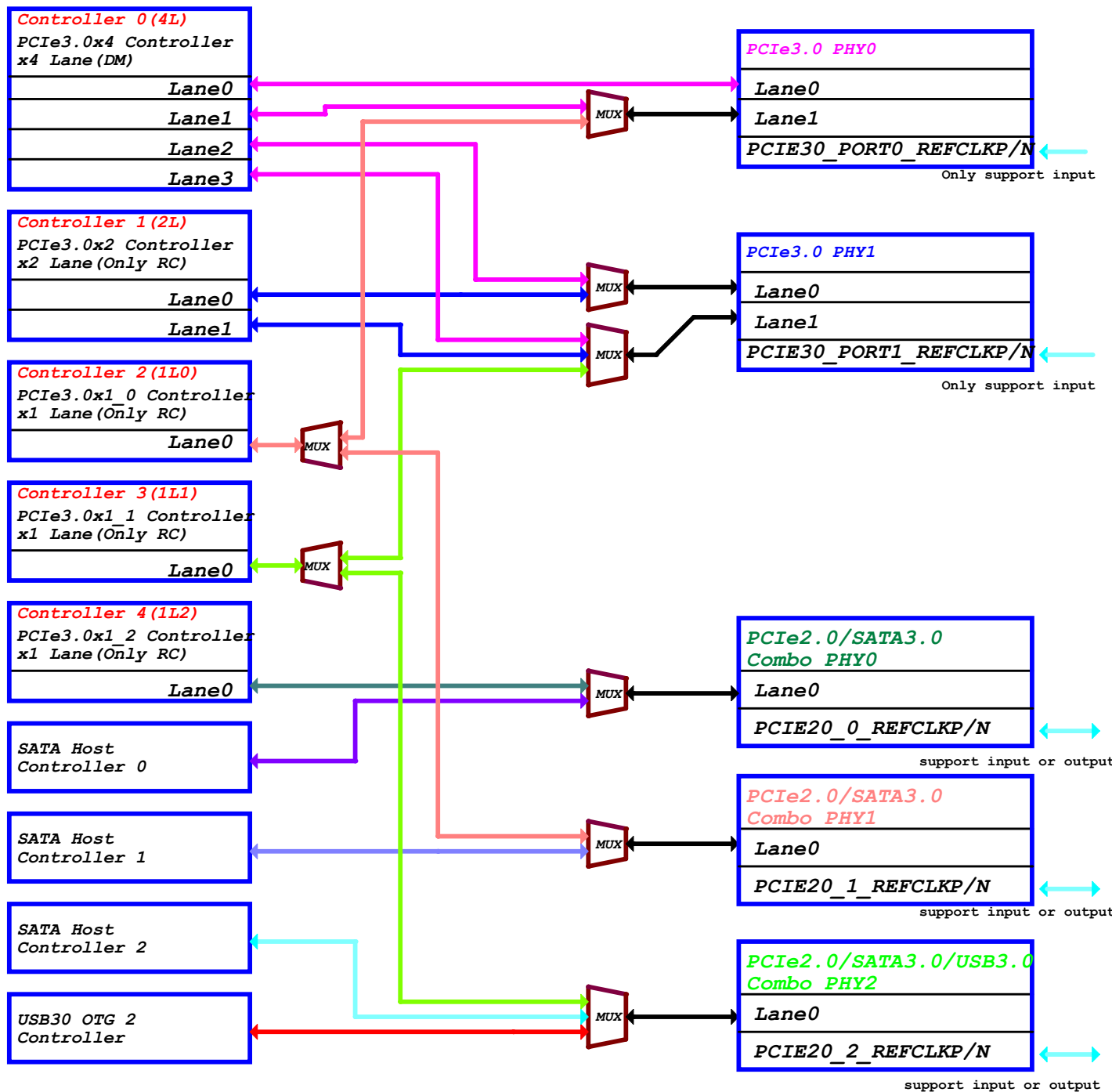
Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



PCIe/SATA Connector Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIe30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIe30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIe30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_TXN PCIE20_1_RXP PCIE20_1_RXN		
PCIe30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_TXN PCIE20_2_RXP PCIE20_2_RXN	
PCIe20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_TXN PCIE20_0_RXP PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note: PCIE30_PORT*_REF_CLKP/N is input gpio
PCIE20_*_REFCLKP/N is output or input gpio

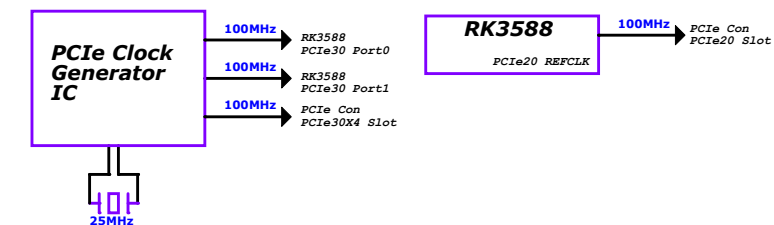
Note: M*=Mean to M0 or M1, It's the same source, Just multiplex to M0 or M1. So, Only use one at the same time.

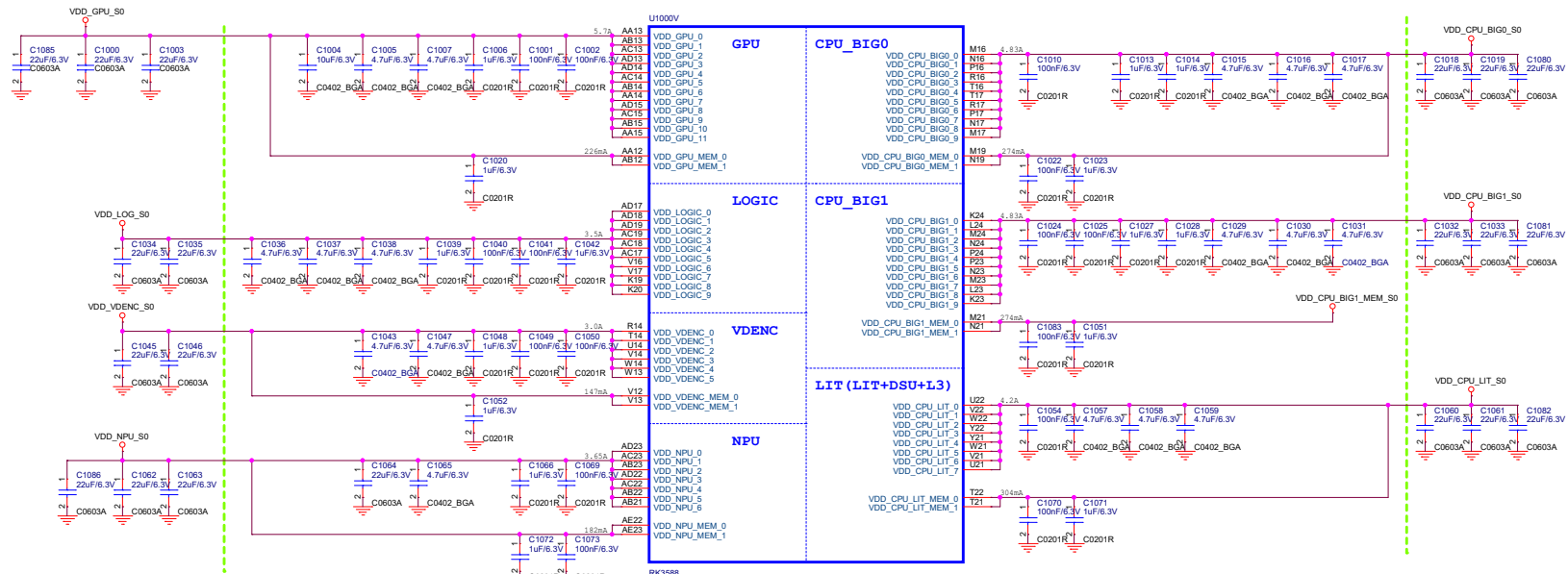
PCIe/SATA Function Combination

Function Combination				
Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK

PCIe2.0 REFCLK





Note:
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

U1000Z		
H28	AVSS_1	AVSS_52
H31	AVSS_2	AVSS_53
H32	AVSS_3	AVSS_54
H33	AVSS_4	AVSS_55
H34	AVSS_5	AVSS_56
H35	AVSS_6	AVSS_57
H36	AVSS_7	AVSS_58
H37	AVSS_8	AVSS_59
H38	AVSS_9	AVSS_60
H39	AVSS_10	AVSS_61
H40	AVSS_11	AVSS_62
H41	AVSS_12	AVSS_63
H42	AVSS_13	AVSS_64
H43	AVSS_14	AVSS_65
H44	AVSS_15	AVSS_66
H45	AVSS_16	AVSS_67
H46	AVSS_17	AVSS_68
H47	AVSS_18	AVSS_69
H48	AVSS_19	AVSS_70
H49	AVSS_20	AVSS_71
H50	AVSS_21	AVSS_72
H51	AVSS_22	AVSS_73
H52	AVSS_23	AVSS_74
H53	AVSS_24	AVSS_75
H54	AVSS_25	AVSS_76
H55	AVSS_26	AVSS_77
H56	AVSS_27	AVSS_78
H57	AVSS_28	AVSS_79
H58	AVSS_29	AVSS_80
H59	AVSS_30	AVSS_81
H60	AVSS_31	AVSS_82
H61	AVSS_32	AVSS_83
H62	AVSS_33	AVSS_84
H63	AVSS_34	AVSS_85
H64	AVSS_35	AVSS_86
H65	AVSS_36	AVSS_87
H66	AVSS_37	AVSS_88
H67	AVSS_38	AVSS_89
H68	AVSS_39	AVSS_90
H69	AVSS_40	AVSS_91
H70	AVSS_41	AVSS_92
H71	AVSS_42	AVSS_93
H72	AVSS_43	AVSS_94
H73	AVSS_44	AVSS_95
H74	AVSS_45	AVSS_96
H75	AVSS_46	AVSS_97
H76	AVSS_47	AVSS_98
H77	AVSS_48	AVSS_99
H78	AVSS_49	AVSS_100
H79	AVSS_50	AVSS_101

U1000X		
L3	VSS_107	VSS_108
L4	VSS_109	VSS_110
L5	VSS_111	VSS_112
L6	VSS_113	VSS_114
L7	VSS_115	VSS_116
L8	VSS_117	VSS_118
L9	VSS_119	VSS_120
L10	VSS_121	VSS_122
L11	VSS_123	VSS_124
L12	VSS_125	VSS_126
L13	VSS_127	VSS_128
L14	VSS_129	VSS_130
L15	VSS_131	VSS_132
L16	VSS_133	VSS_134
L17	VSS_135	VSS_136
L18	VSS_137	VSS_138
L19	VSS_139	VSS_140
L20	VSS_141	VSS_142
L21	VSS_143	VSS_144
L22	VSS_145	VSS_146
L23	VSS_147	VSS_148
L24	VSS_149	VSS_150
L25	VSS_151	VSS_152
L26	VSS_153	VSS_154
L27	VSS_155	VSS_156
L28	VSS_157	VSS_158
L29	VSS_159	VSS_160
L30	VSS_161	VSS_162
L31	VSS_163	VSS_164
L32	VSS_165	VSS_166
L33	VSS_167	VSS_168
L34	VSS_169	VSS_170
L35	VSS_171	VSS_172
L36	VSS_173	VSS_174
L37	VSS_175	VSS_176
L38	VSS_177	VSS_178
L39	VSS_179	VSS_180
L40	VSS_181	VSS_182
L41	VSS_183	VSS_184
L42	VSS_185	VSS_186
L43	VSS_187	VSS_188
L44	VSS_189	VSS_190
L45	VSS_191	VSS_192
L46	VSS_193	VSS_194
L47	VSS_195	VSS_196
L48	VSS_197	VSS_198
L49	VSS_199	VSS_200
L50	VSS_201	VSS_202
L51	VSS_203	VSS_204
L52	VSS_205	VSS_206
L53	VSS_207	VSS_208
L54	VSS_209	VSS_210
L55	VSS_211	VSS_212

U1000W		
A1	VSS_1	VSS_54
A2	VSS_2	VSS_55
A3	VSS_3	VSS_56
A4	VSS_4	VSS_57
A5	VSS_5	VSS_58
A6	VSS_6	VSS_59
A7	VSS_7	VSS_60
A8	VSS_8	VSS_61
A9	VSS_9	VSS_62
A10	VSS_10	VSS_63
A11	VSS_11	VSS_64
A12	VSS_12	VSS_65
A13	VSS_13	VSS_66
A14	VSS_14	VSS_67
A15	VSS_15	VSS_68
A16	VSS_16	VSS_69
A17	VSS_17	VSS_70
A18	VSS_18	VSS_71
A19	VSS_19	VSS_72
A20	VSS_20	VSS_73
A21	VSS_21	VSS_74
A22	VSS_22	VSS_75
A23	VSS_23	VSS_76
A24	VSS_24	VSS_77
A25	VSS_25	VSS_78
A26	VSS_26	VSS_79
A27	VSS_27	VSS_80
A28	VSS_28	VSS_81
A29	VSS_29	VSS_82
A30	VSS_30	VSS_83
A31	VSS_31	VSS_84
A32	VSS_32	VSS_85
A33	VSS_33	VSS_86
A34	VSS_34	VSS_87
A35	VSS_35	VSS_88
A36	VSS_36	VSS_89
A37	VSS_37	VSS_90
A38	VSS_38	VSS_91
A39	VSS_39	VSS_92
A40	VSS_40	VSS_93
A41	VSS_41	VSS_94
A42	VSS_42	VSS_95
A43	VSS_43	VSS_96
A44	VSS_44	VSS_97
A45	VSS_45	VSS_98
A46	VSS_46	VSS_99
A47	VSS_47	VSS_100
A48	VSS_48	VSS_101
A49	VSS_49	VSS_102
A50	VSS_50	VSS_103
A51	VSS_51	VSS_104
A52	VSS_52	VSS_105
A53	VSS_53	VSS_106

U1000Y		
W3	VSS_213	VSS_266
W4	VSS_214	VSS_267
W5	VSS_215	VSS_268
W6	VSS_216	VSS_269
W7	VSS_217	VSS_270
W8	VSS_218	VSS_271
W9	VSS_219	VSS_272
W10	VSS_220	VSS_273
W11	VSS_221	VSS_274
W12	VSS_222	VSS_275
W13	VSS_223	VSS_276
W14	VSS_224	VSS_277
W15	VSS_225	VSS_278
W16	VSS_226	VSS_279
W17	VSS_227	VSS_280
W18	VSS_228	VSS_281
W19	VSS_229	VSS_282
W20	VSS_230	VSS_283
W21	VSS_231	VSS_284
W22	VSS_232	VSS_285
W23	VSS_233	VSS_286
W24	VSS_234	VSS_287
W25	VSS_235	VSS_288
W26	VSS_236	VSS_289
W27	VSS_237	VSS_290
W28	VSS_238	VSS_291
W29	VSS_239	VSS_292
W30	VSS_240	VSS_293
W31	VSS_241	VSS_294
W32	VSS_242	VSS_295
W33	VSS_243	VSS_296
W34	VSS_244	VSS_297
W35	VSS_245	VSS_298
W36	VSS_246	VSS_299
W37	VSS_247	VSS_300
W38	VSS_248	VSS_301
W39	VSS_249	VSS_302
W40	VSS_250	VSS_303
W41	VSS_251	VSS_304
W42	VSS_252	VSS_305
W43	VSS_253	VSS_306
W44	VSS_254	VSS_307
W45	VSS_255	VSS_308
W46	VSS_256	VSS_309
W47	VSS_257	VSS_310
W48	VSS_258	VSS_311
W49	VSS_259	VSS_312
W50	VSS_260	VSS_313
W51	VSS_261	VSS_314
W52	VSS_262	VSS_315
W53	VSS_263	VSS_316
W54	VSS_264	VSS_317
W55	VSS_265	VSS_318

RK3588_E (OSC/PLL/PMUIO1/2)

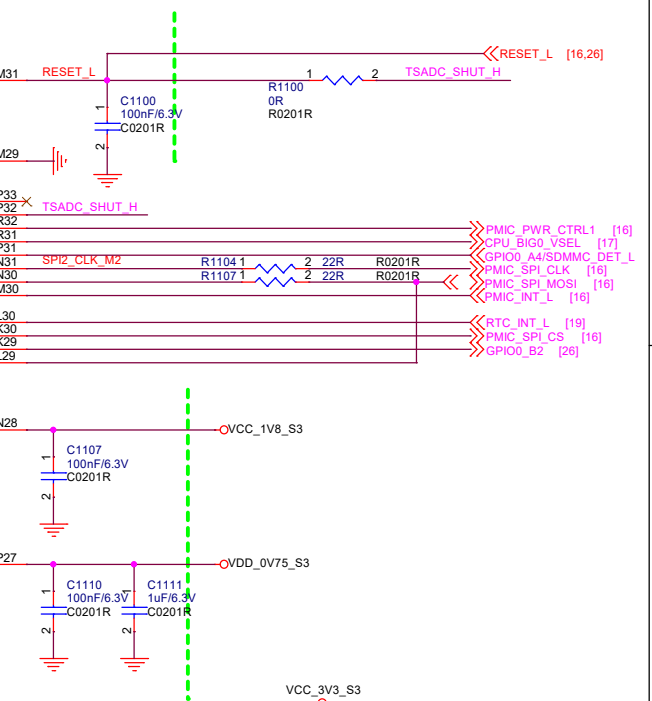
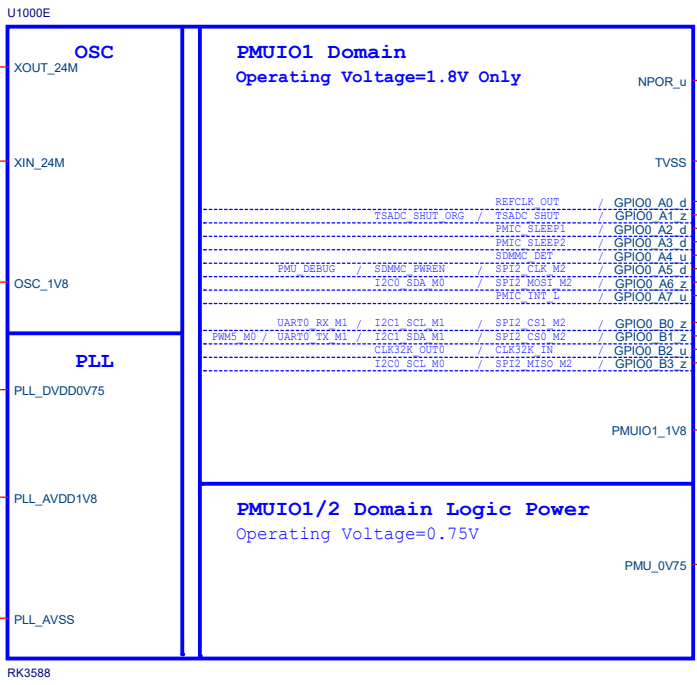
Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

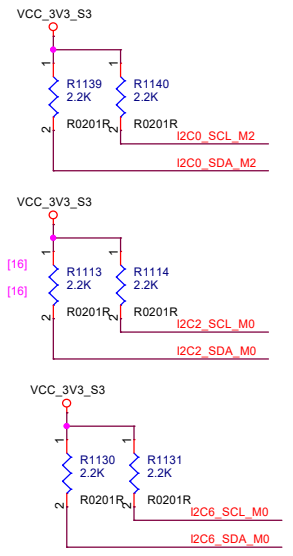
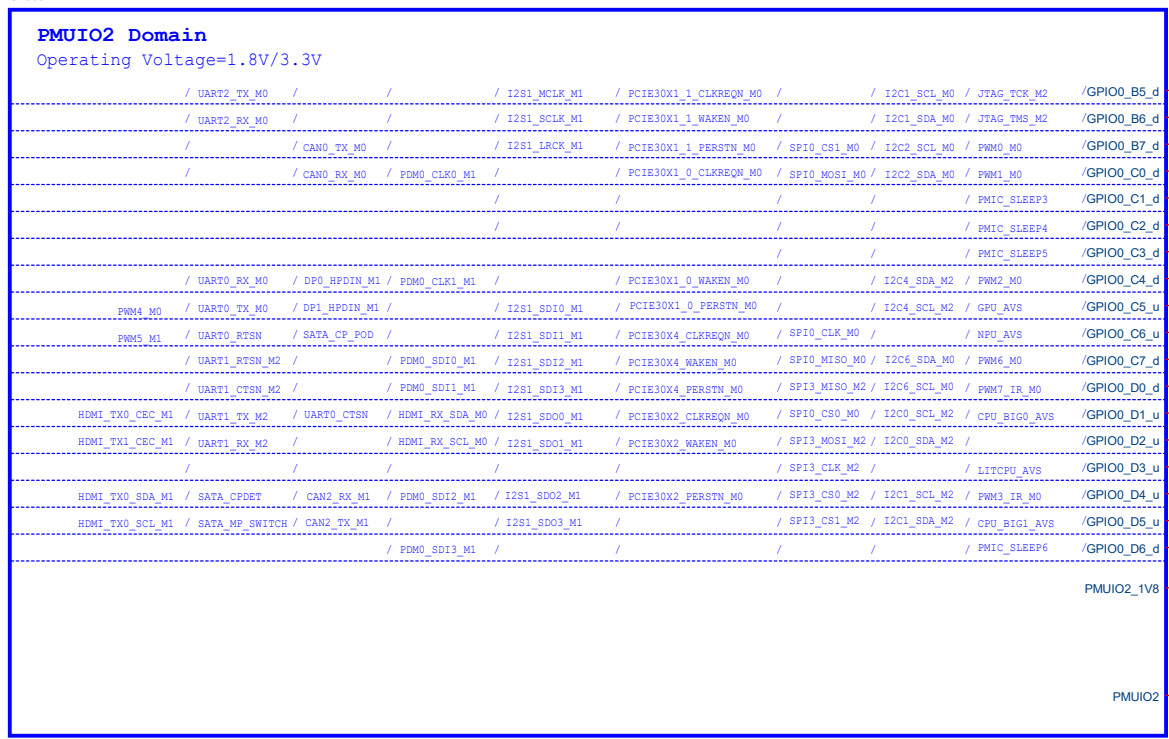
$$CL = \left(\frac{CL1 * CL2}{CL1 + CL2} \right) + PCB \text{ strays}$$

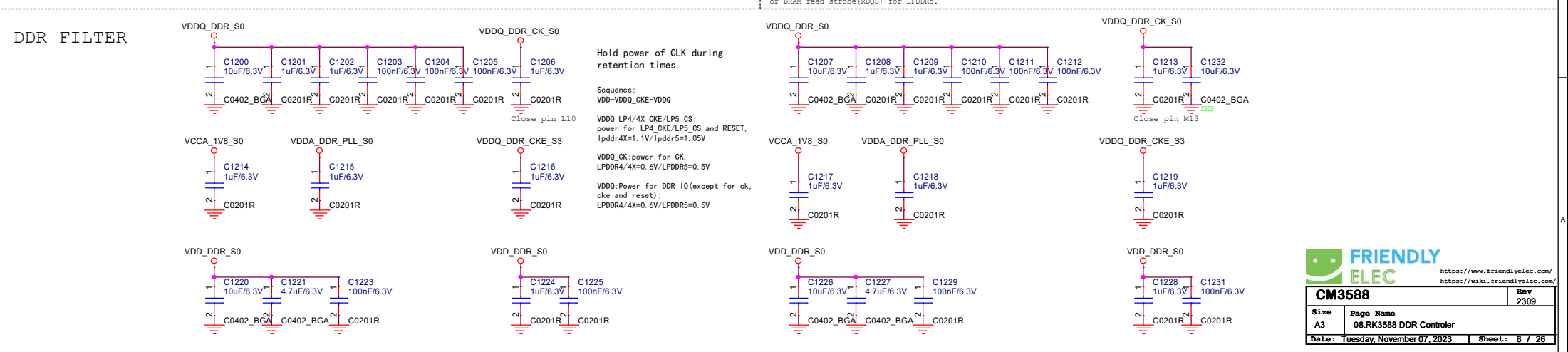
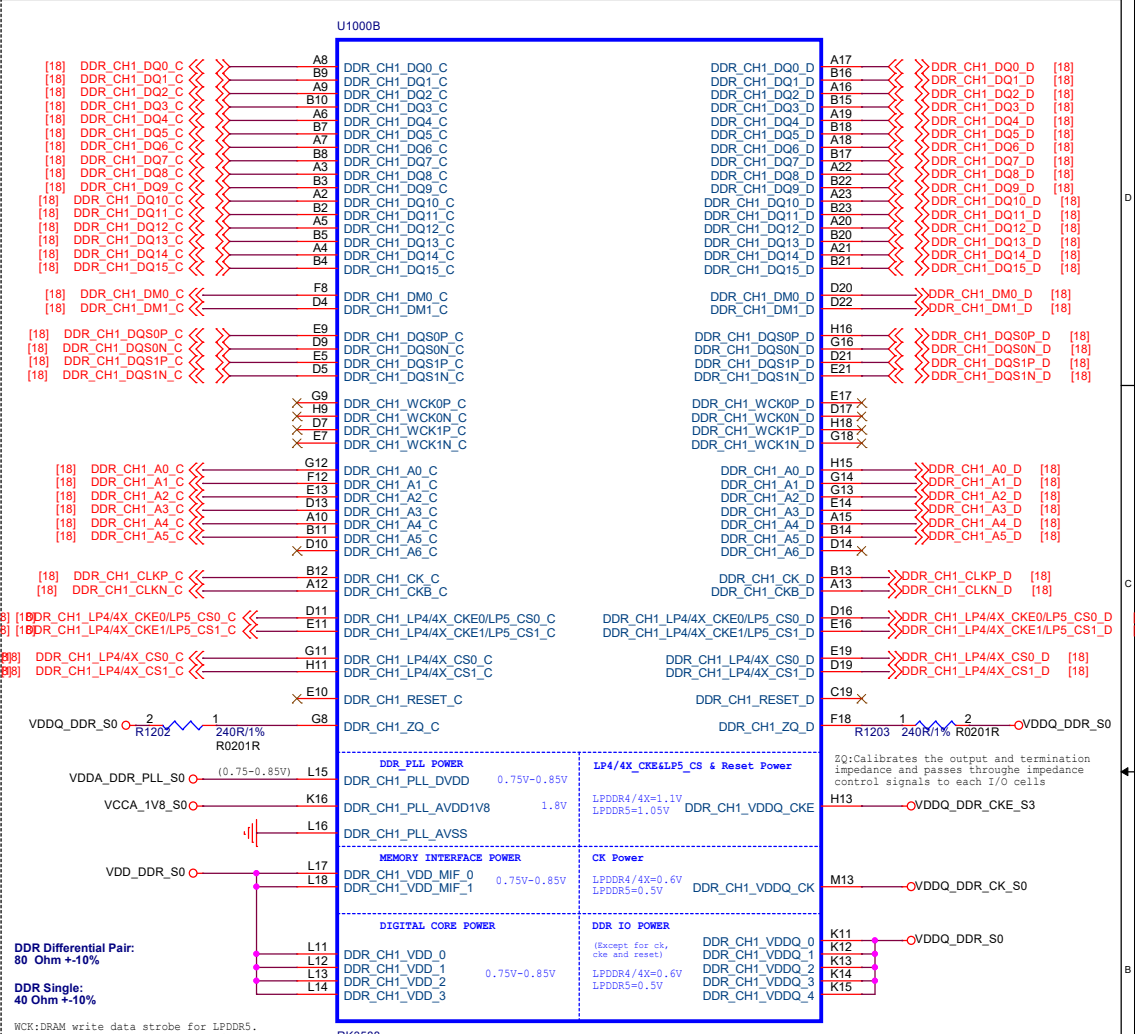
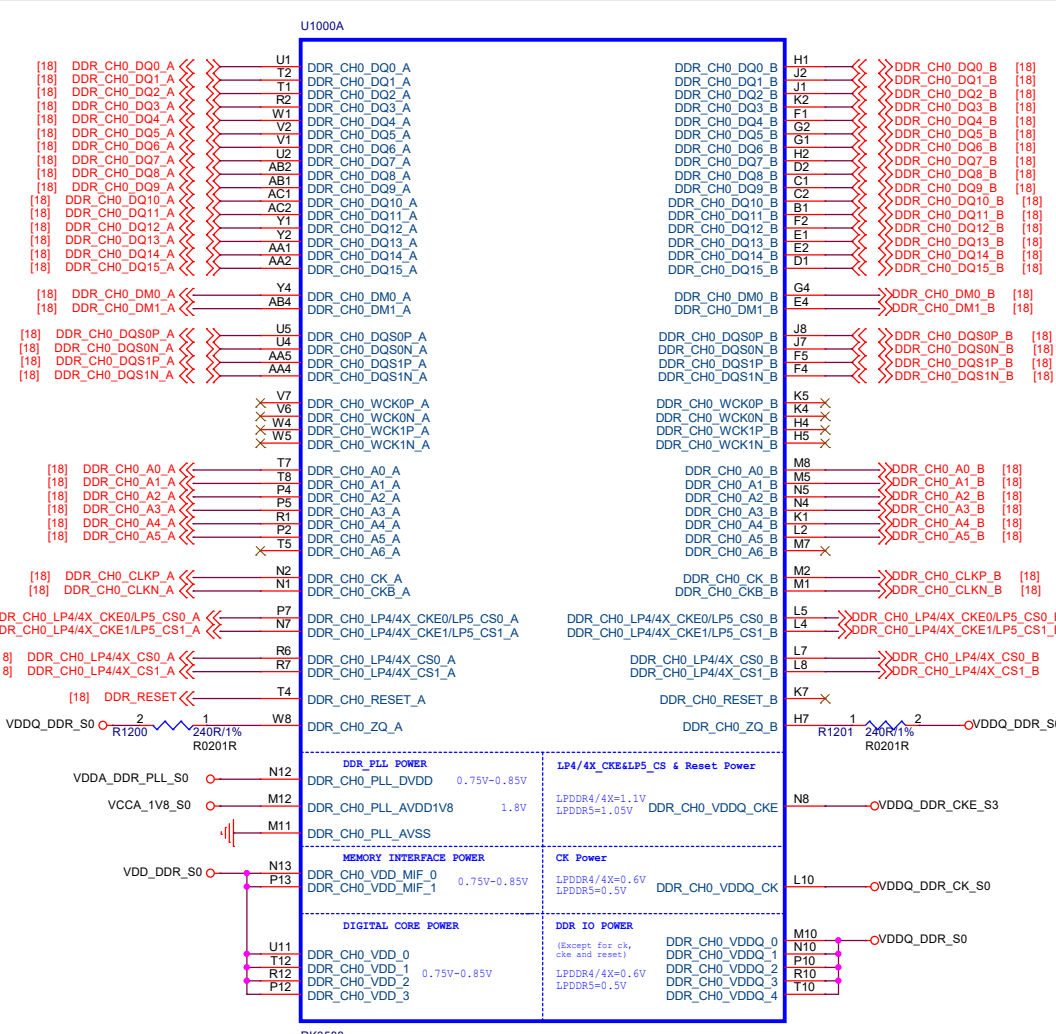
Total CL <= 12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



RK3588_F (PMUIO2)





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<https://wiki.friendlyelec.com/>

CM3588		Rev
Size	Page Name	2309
A3	08.RK3588 DDR Controller	
Date:	Tuesday, November 07, 2023	Sheet: 8 / 26

RK3588_C (EMMCIO Domain)

U1000C

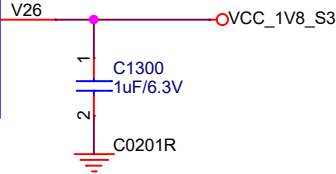
EMMCIO Domain

Operating Voltage=1.8V

FSPi D0 M0	/ EMMC D0	/ GPIO2 D0 u
FSPi D1 M0	/ EMMC D1	/ GPIO2 D1 u
FSPi D2 M0	/ EMMC D2	/ GPIO2 D2 u
FSPi D3 M0	/ EMMC D3	/ GPIO2 D3 u
UART5 RX M2	/ I2C1 SCL M3 / EMMC D4	/ GPIO2 D4 u
UART5 TX M2	/ I2C1 SDA M3 / EMMC D5	/ GPIO2 D5 u
FSPi CS0N M0	/ EMMC D6	/ GPIO2 D6 u
FSPi CS1N M0	/ EMMC D7	/ GPIO2 D7 u
FSPi CLK M0	/ EMMC CMD	/ GPIO2 A0 u
	/ EMMC CLKOUT	/ GPIO2 A1 d
UART5 CTSN M1	/ I2C2 SDA M2 / EMMC DATA STROBE	/ GPIO2 A2 d
UART5 RTSN M1	/ I2C2 SCL M2 / EMMC RSTn	/ GPIO2 A3 d



EMMCIO_1V8



RK3588

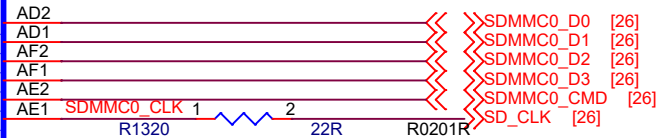
RK3588_D (VCCIO2 Domain)

U1000D

VCCIO2 Domain

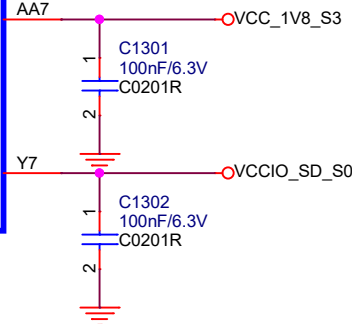
Operating Voltage=1.8V/3.3V

PWM8 M1	/ I2C3 SCL M4 / PDM1 SDI3 M0 / JTAG TCK M1	/ UART2 TX M1	/ SDMMC D0	/ GPIO4 D0 u
PWM9 M1	/ I2C3 SDA M4 / PDM1 SDI2 M0 / JTAG TMS M1	/ UART2 RX M1	/ SDMMC D1	/ GPIO4 D1 u
	/ I2C8 SCL M0 / PDM1 SDI1 M0 / JTAG TCK M0	/ UART5 CTSN M0	/ SDMMC D2	/ GPIO4 D2 u
PWM10 M1	/ I2C8 SDA M0 / PDM1 SDIO M0 / JTAG TMS M0	/ UART5 RTSN M0	/ SDMMC D3	/ GPIO4 D3 u
PWM7 IR M1	/ CAN0 TX M1 / PDM1 CLK1 M0 / MCU JTAG TCK M0	/ UART5 RX M0	/ SDMMC CMD	/ GPIO4 D4 u
TEST_CLKOUT M0	/ CAN0 RX M1 / PDM1 CLK0 M0 / MCU JTAG TMS M0	/ UART5 TX M0	/ SDMMC CLK	/ GPIO4 D5 d



VCCIO2_1V8

VCCIO2



RK3588



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<https://wiki.friendlyelec.com/>

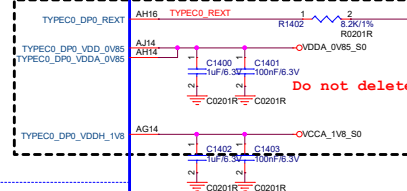
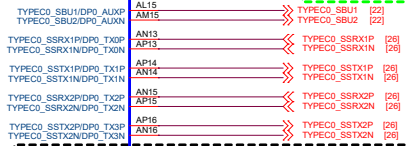
CM3588		Rev 2309
Size A4	Page Name 09.RK3588_Flash/SD Controller	
Date: Tuesday, November 07, 2023	Sheet: 9 / 26	

RK3588_M (TYPEC/DP)

U1000M

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

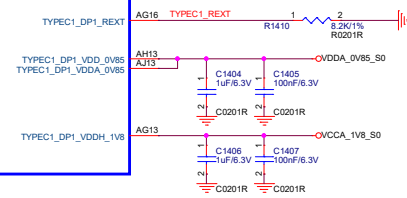
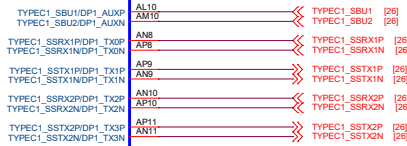


Do not delete!!!

USB30 Differential Pair: DATE:90 Ohm +/-10%
DP Differential Pair: DATE:100 Ohm +/-10%
For USB30 For DP

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3



Note:
If need full function of Typec1 (with DP function) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

Note:
If TYPEC0 is not used:
Signal: Leave floating
REXT: 20 ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC&DP MIX Differential Pair:
DATE:90 Ohm +/-10%
For Typec

RK3588

USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX Lane0-3
Option2	USB30 x4Lane	DP_TX Lane0-3
Option3	USB30x2Lane+DPx2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30x2Lane+DPx2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

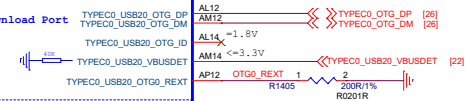
RK3588_L (USB2.0 HOST/OTG)

U1000L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)

HS/FS/LS

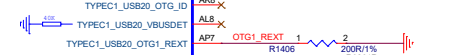
Download Port



USB20 Differential Pair:
DATE:90 Ohm +/-10%

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)

HS/FS/LS



USB2.0 HOST0

HS/FS/LS

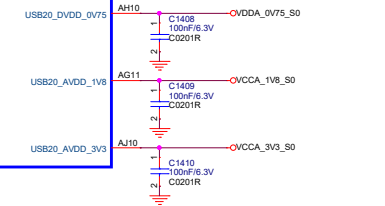


USB2.0 HOST1

HS/FS/LS



USB2.0 POWER



RK3588

Note:
TYPECO_USB20_OTG:
DP/DM: Must used for download
ID: According to demand, if not used, Leave floating
VBUSDET: Must provide
REXT: 200ohm 1% resistor must be connected externally
Power: Must supply power

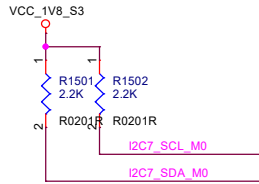
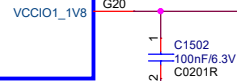
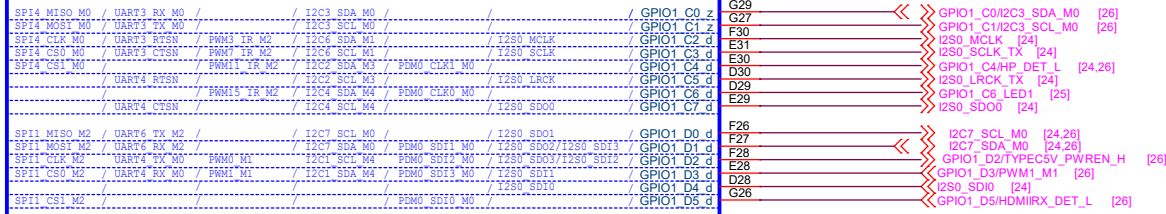
TYPEC1_USB20_OTG: USB20_HOST0/USB20_HOST1:
If not used: If not used:
DP/DM: Leave floating DP/DM: Leave floating
ID: Leave floating ID: Leave floating
VBUSDET: Leave floating VBUSDET: Leave floating
REXT: Leave floating REXT: Leave floating

Note:
The USB20 VBUSDET pin internal has a pull-down resistance(40K ohm) to ground, The resistance creates a voltage with the external series 30K ohm resistor. The VBUSDET pin voltage range <=3.3V.

RK3588_G (VCCIO1 Domain)

U1000G

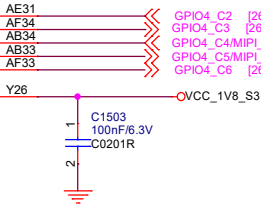
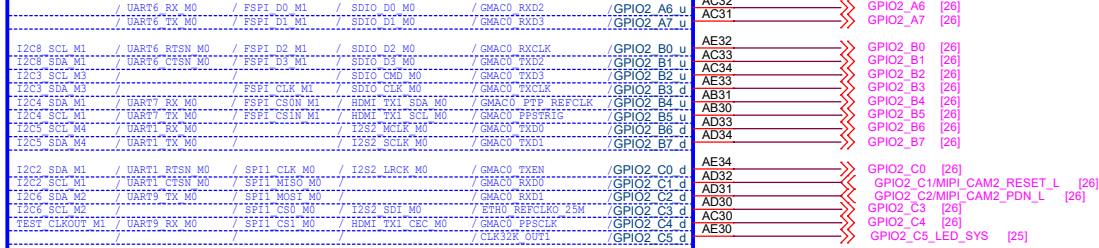
VCCIO1 Domain
Operating Voltage=1.8V



RK3588_H (VCCIO3 Domain)

U1000H

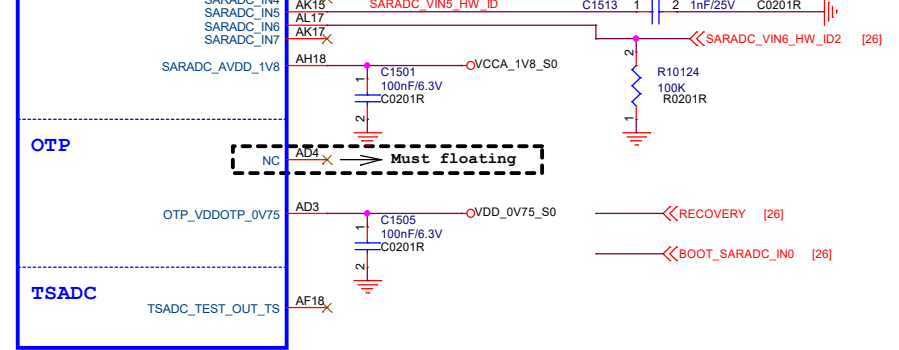
VCCIO3 Domain
Operating Voltage=1.8V



RK3588_U (SARADC/OTP)

U1000U

SARADC
12-bit 1MS/s

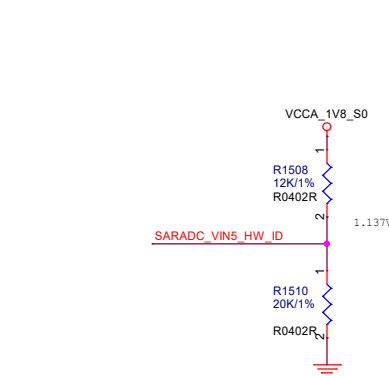


BOOT MODE CONFIG

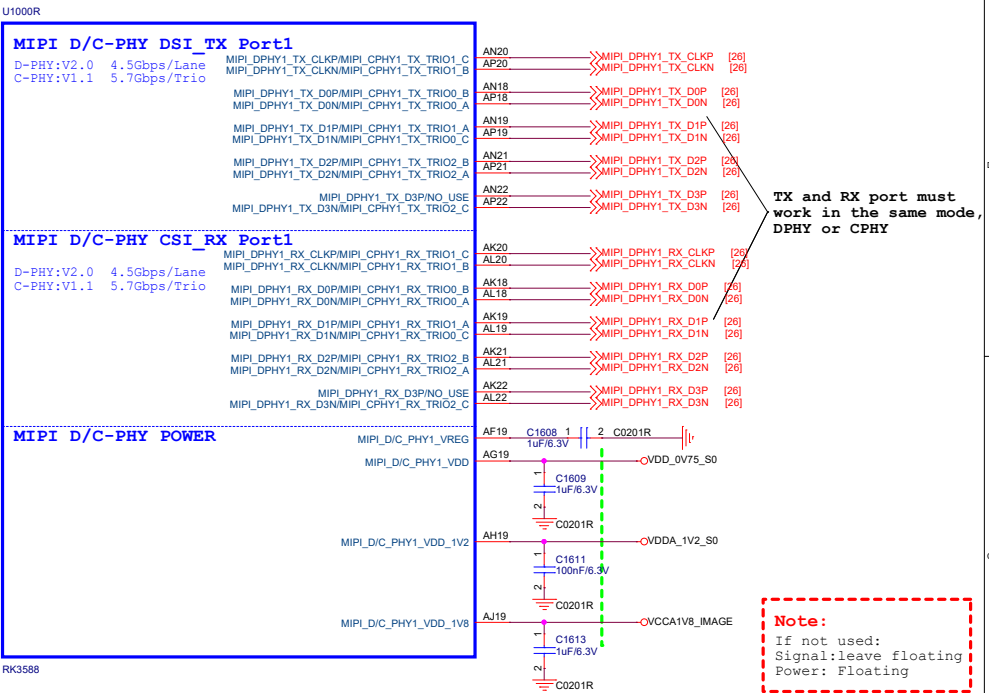
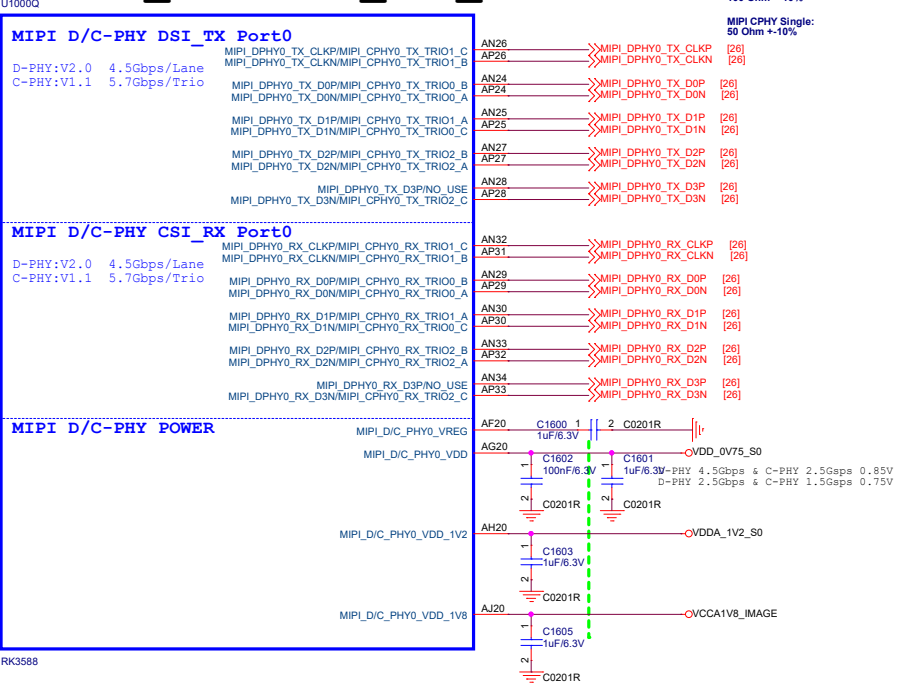
TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0-EMMC-SD Card-USB

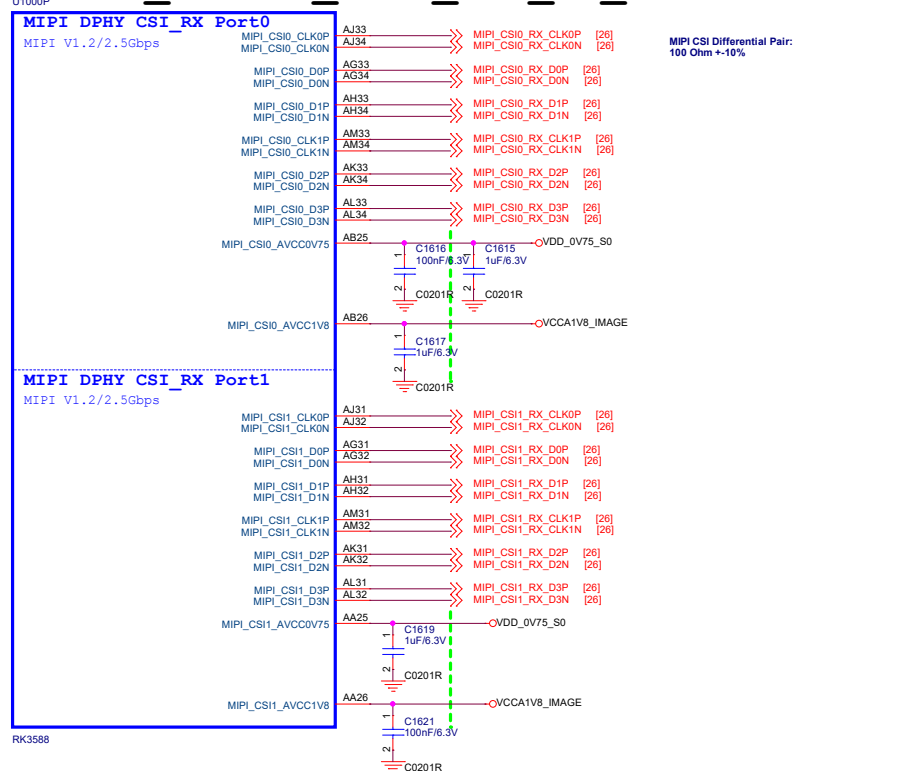
BOARD ID CONFIG



RK3588_Q/R (MIPI_D/C_PHY0/1)



RK3588_P (MIPI_DPHY_CSI_RX_PHY)



MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
 When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

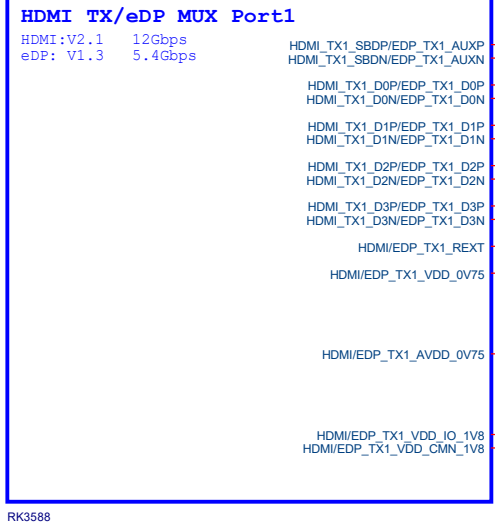
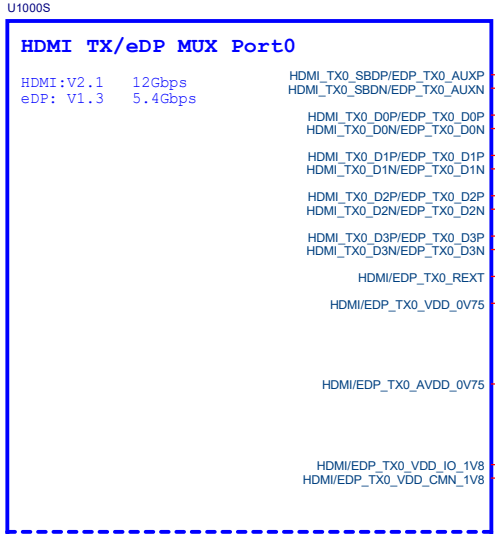
Note:
 The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

Note:
 If not used:
 Signal:leave floating
 Power: Floating

RK3588_S (HDMI2.1 TX)

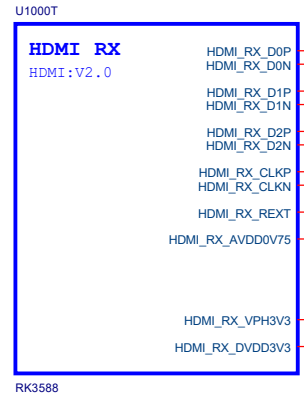
RK3588_T (HDMI20 RX)

Note:
 The HDMI2.1 trace length is less than 100mm.
 The HDMI2.1 differential trace impedance is 100 OHM.



Note:
 The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

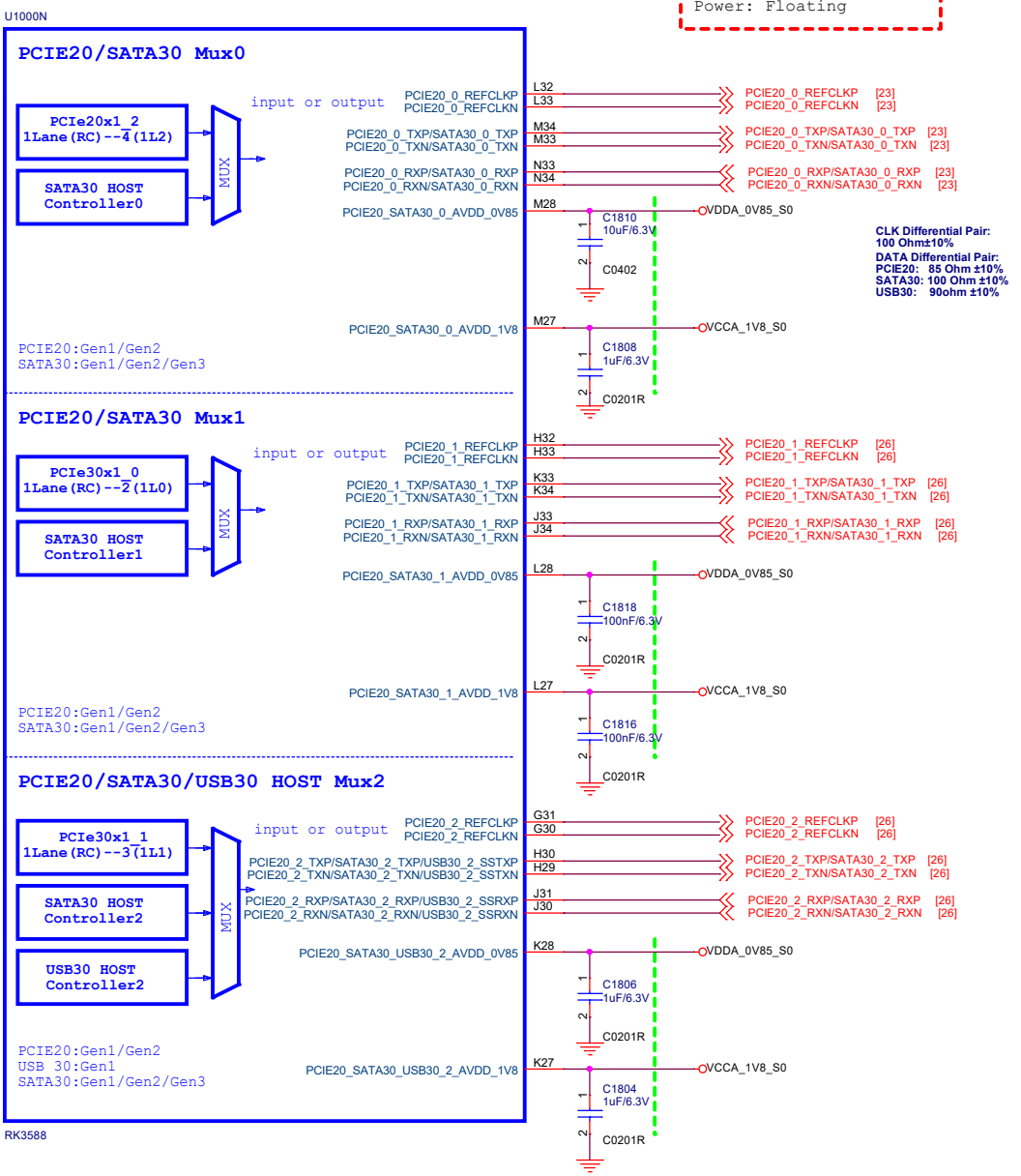
Note:
 If not used:
 Signal: leave floating
 Power: Floating or tie to VSS



Note:
 If not used:
 Signal: leave floating
 Power: Floating

RK3588_N (PCIE20)

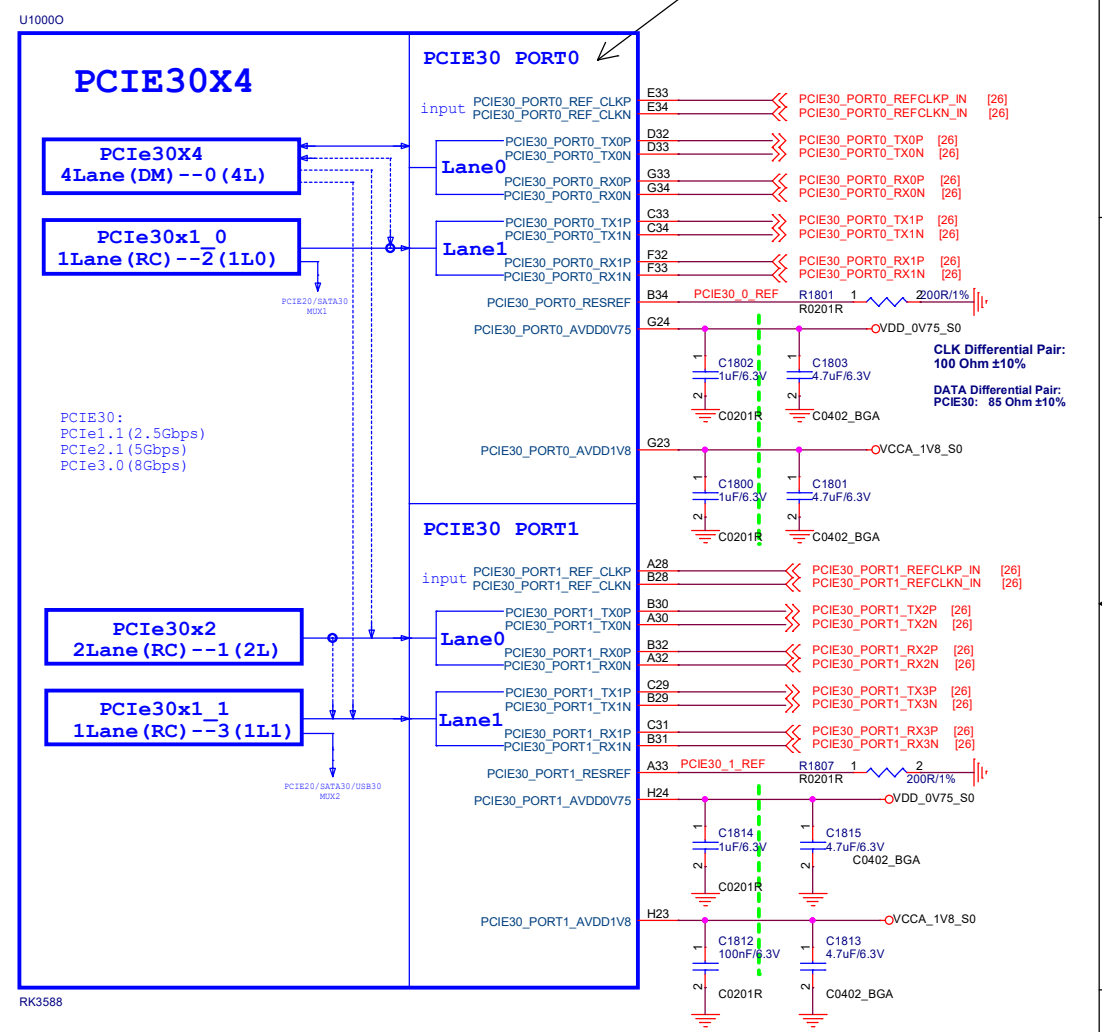
Note:
 If not used:
 Signal: leave floating
 Power: Floating



Note:
 The SATA differential trace impedance is 100 OHM
 The SATA trace length is less than 5 inch

RK3588_O (PCIE30)

Note:
 Only PCIe3.0 Controller 0
 support RC and EP, Other
 controller only support RC
 Mode.



Note:
 If Port0 and Port1 are not used,
 Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
 Port0 and Port1 Other Signal: Leave floating
 Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used, Port1 is not used,
 Port1 REF_CLKP/N: Leave floating or tie to VSS
 Port1 Other Signal: Leave floating
 Port1 Power: Must supply power

If Port1 is used, Port0 is not used,
 Port0 REF_CLKP/N: Leave floating or tie to VSS
 Port0 Other Signal: Leave floating
 Port0 Power: Must supply power

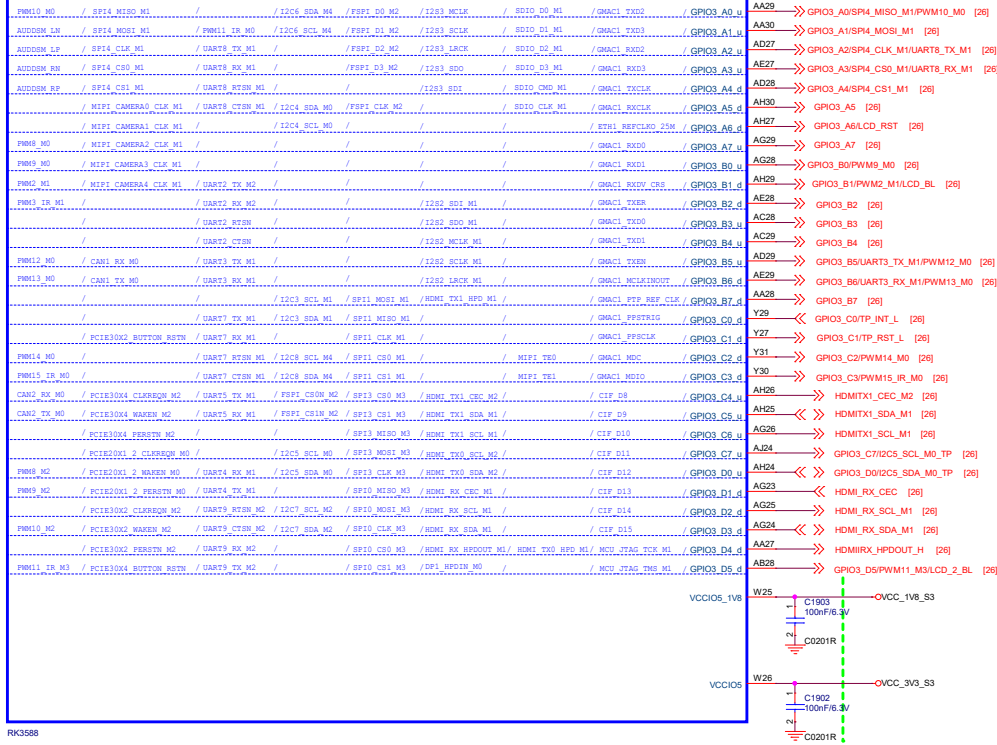
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<https://wiki.friendlyelec.com/>

CM3588		Rev	2309
Size	Page Name		
A3	14.RK3588_PCIE30/PCIE20/SATA30		
Date:	Tuesday, November 07, 2023	Sheet:	14/ 26

RK3588_J (VCCIO5 Domain)

U1000J

VCCIO5 Domain
Operating Voltage=1.8V/3.3V

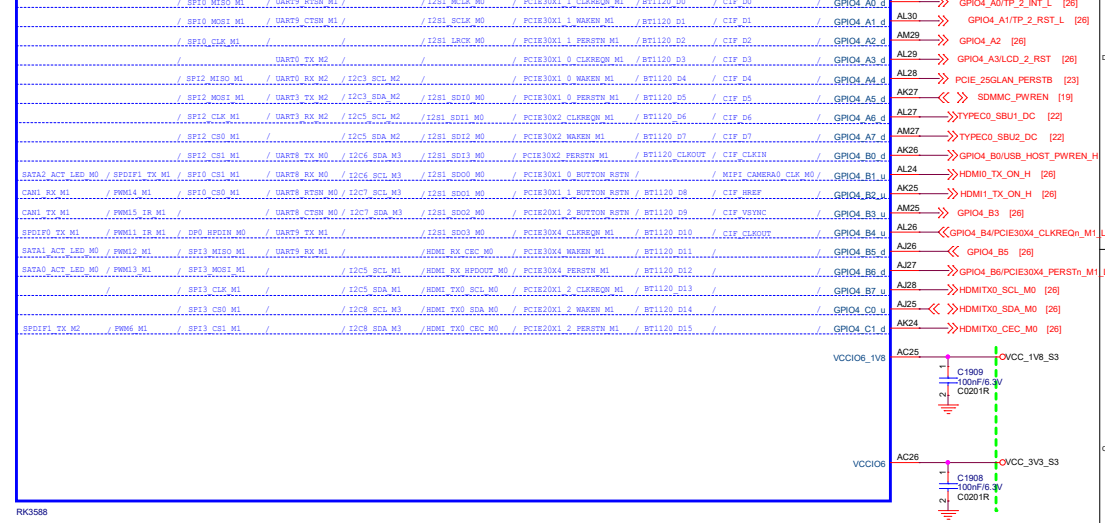


RK3588

RK3588_K (VCCIO6 Domain)

U1000K

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

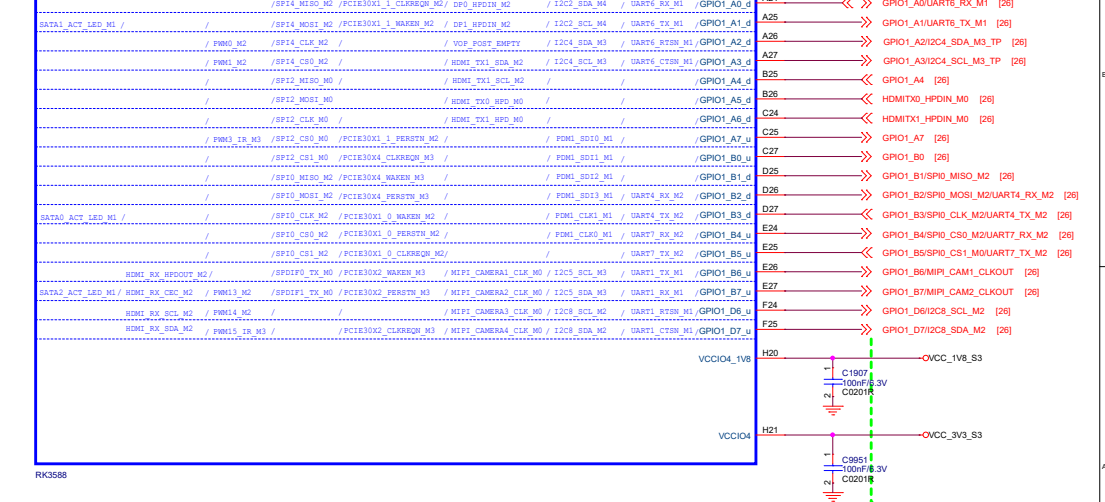


RK3588

RK3588_I (VCCIO4 Domain)

U1000I

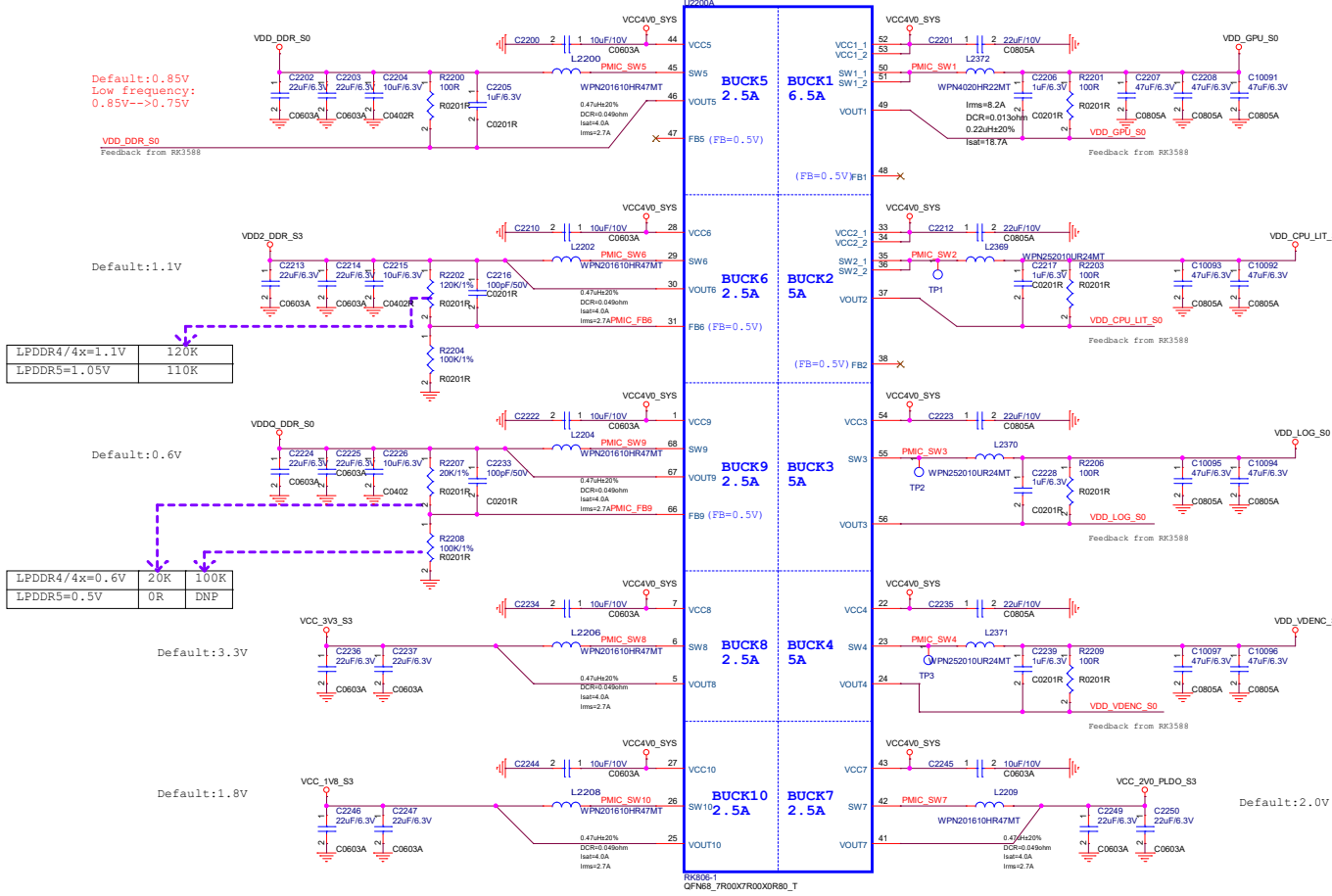
VCCIO4 Domain
Operating Voltage=1.8V/3.3V



RK3588

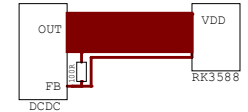
PMIC RK806-1 BUCK

- PMIC_SPI_CS [7]
- PMIC_SPI_MOSI [7]
- PMIC_SPI_CLK [7]
- PMIC_PWR_CTRL1 [7]
- PMIC_PWR_CTRL2 [7]
- PMIC_PWR_CTRL3 [7]
- PMIC_INT_L [7]
- RESET_L [7,26]
- PWRON_EXT_EN_OUT [17,26]
- PWRON_L [26]



LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

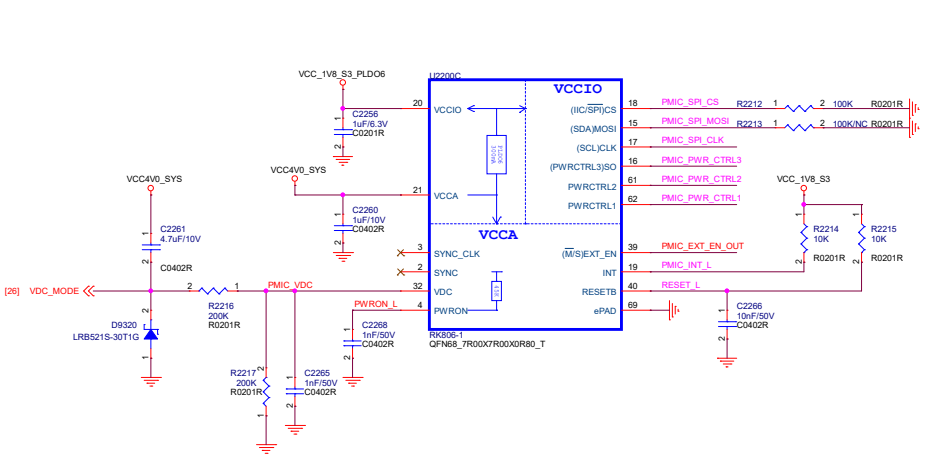


IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

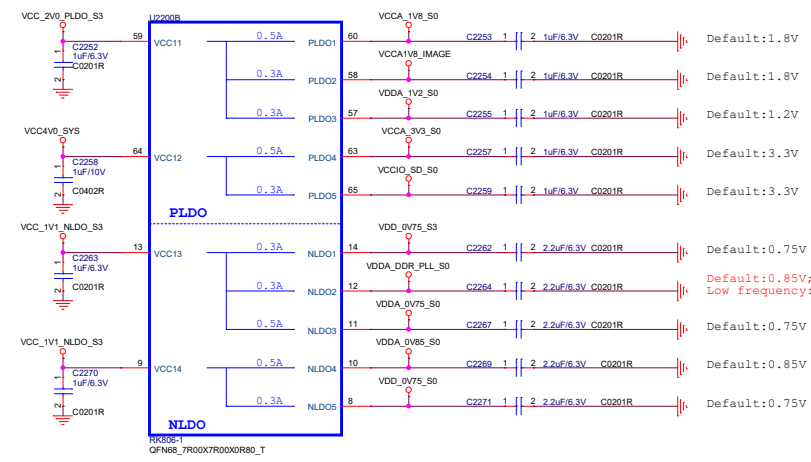
This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications
 Operating Supply Voltage > 5.5V(5.25-6V)
 Peak Pulse Current > 10A (tPulse/20us)
 Surge Clamping Voltage < 6.5V

DO NOT DELETE IT!

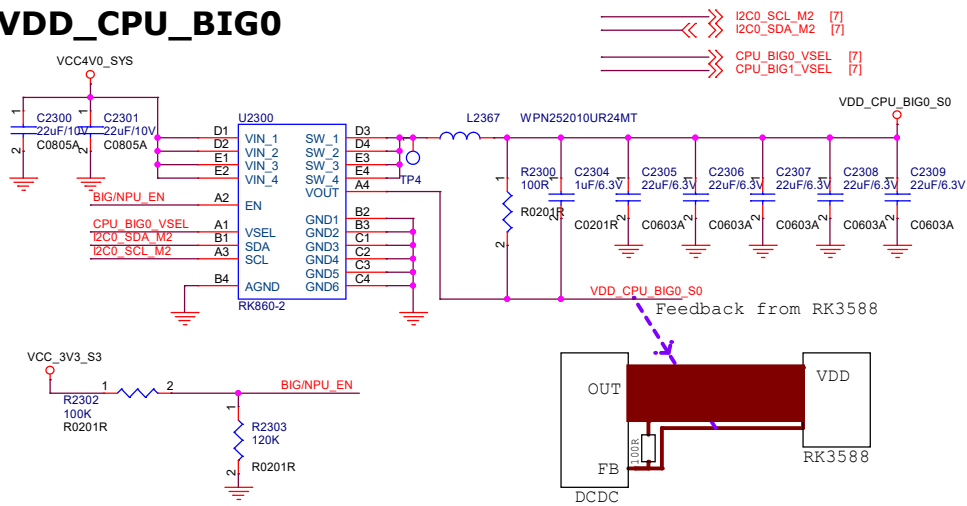
PMIC RK806-1 Management



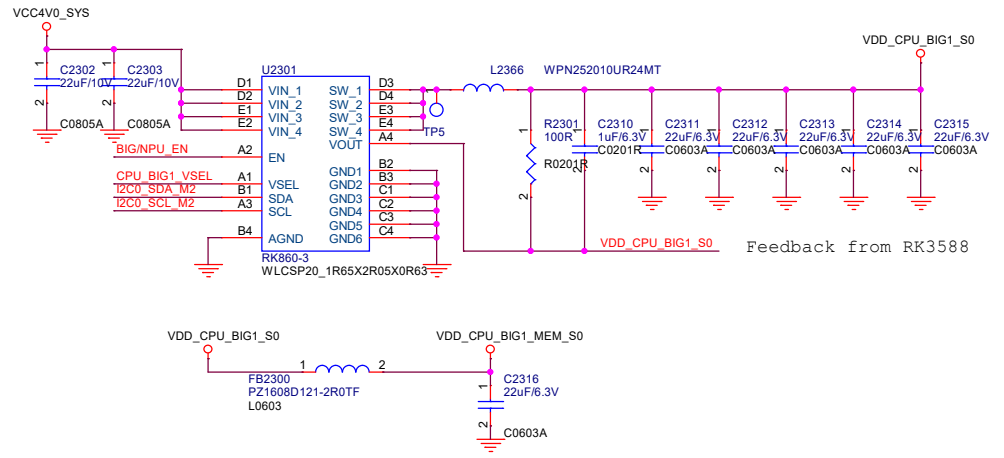
PMIC RK806-1 LDO



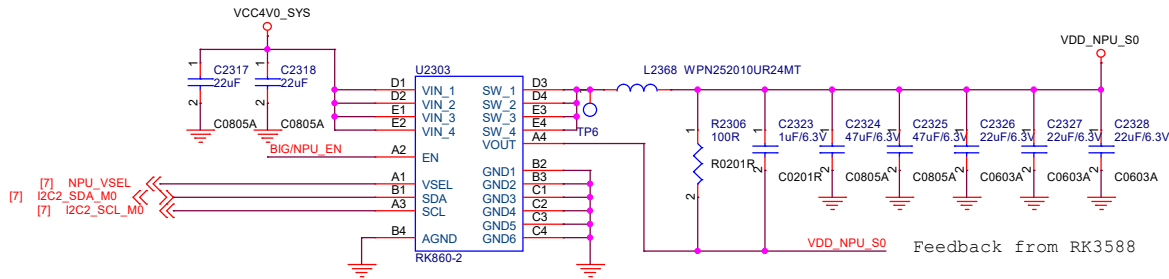
VDD_CPU_BIG0



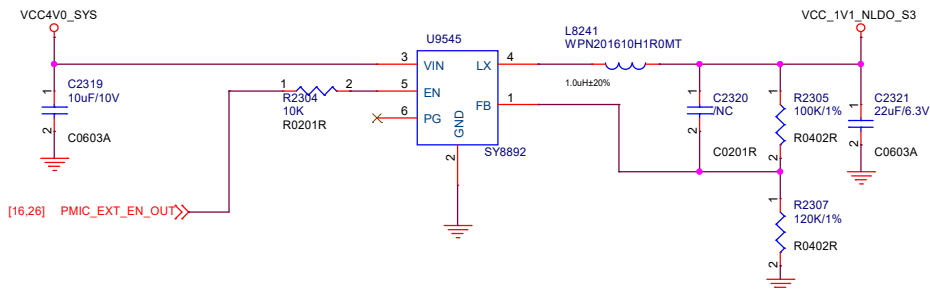
VDD_CPU_BIG1



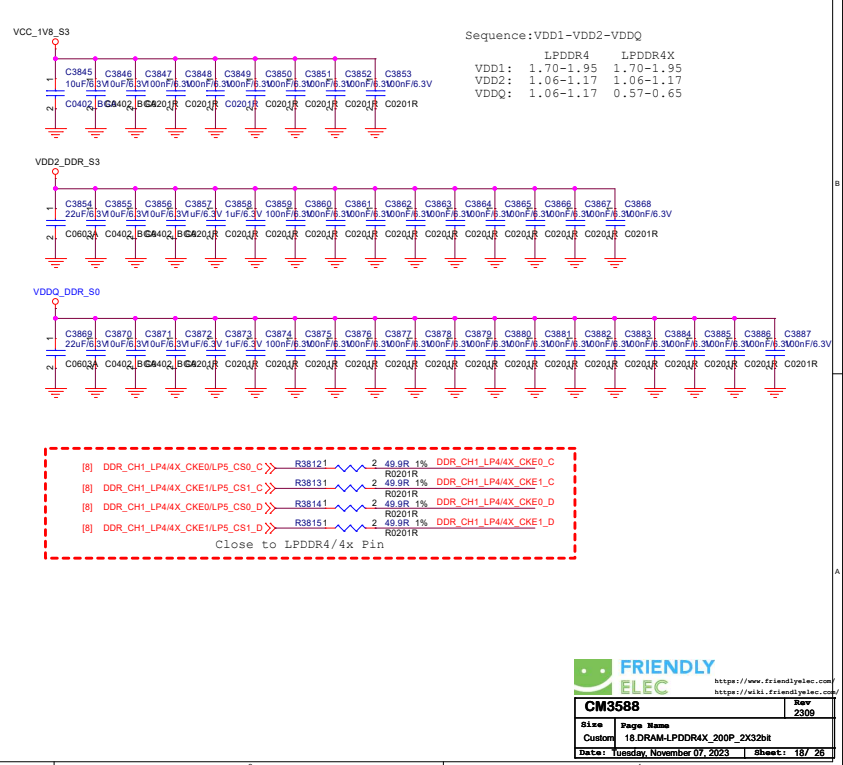
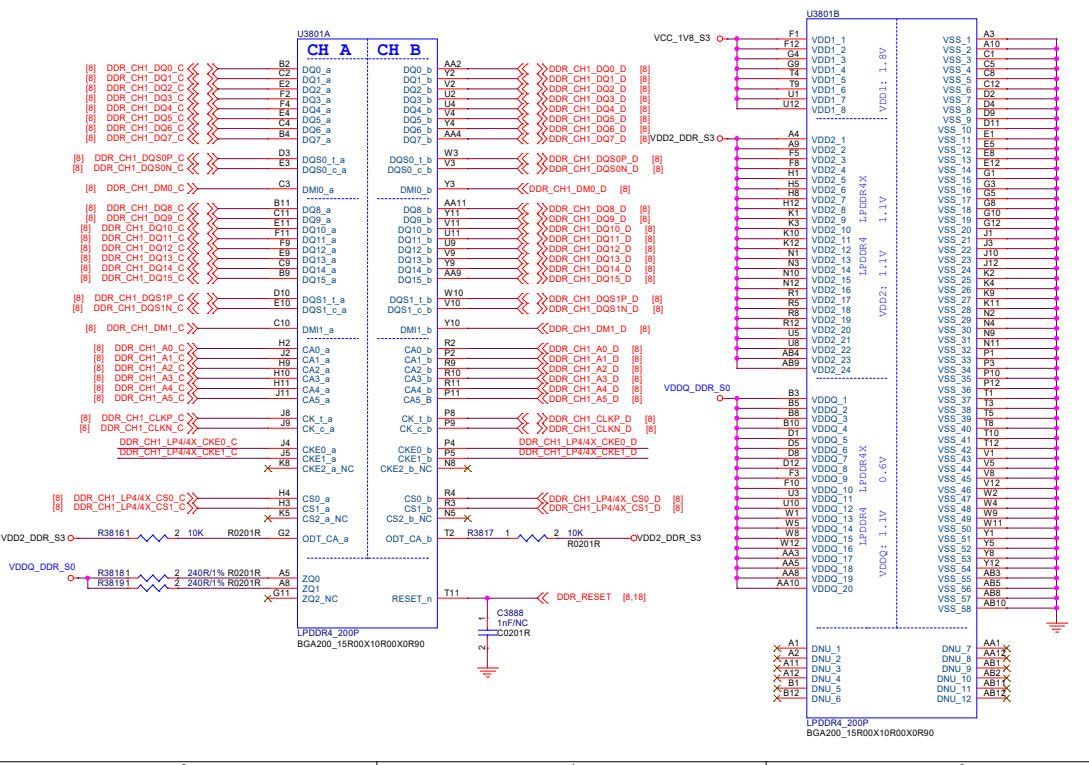
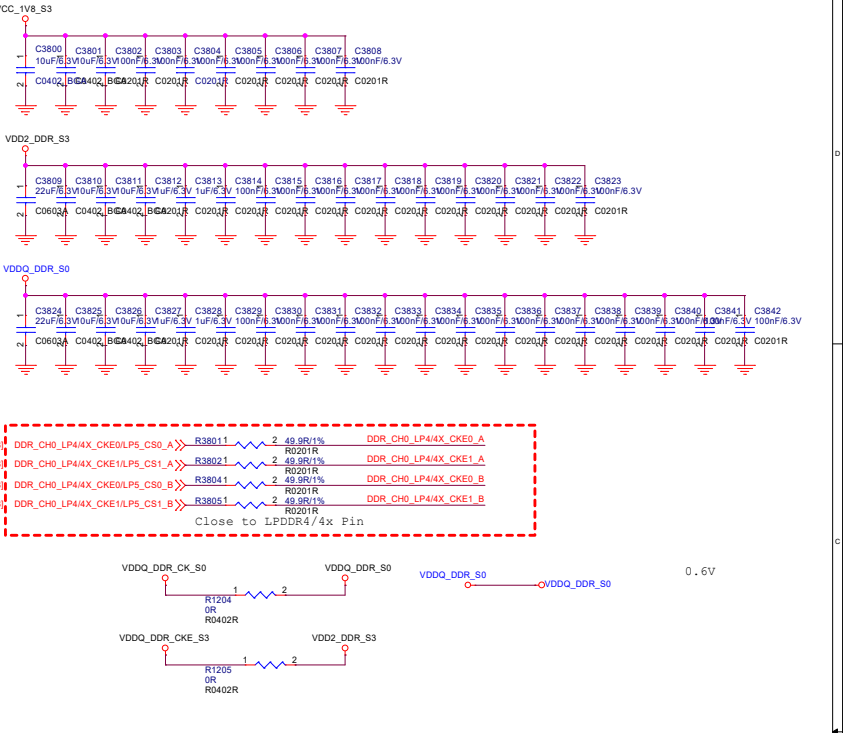
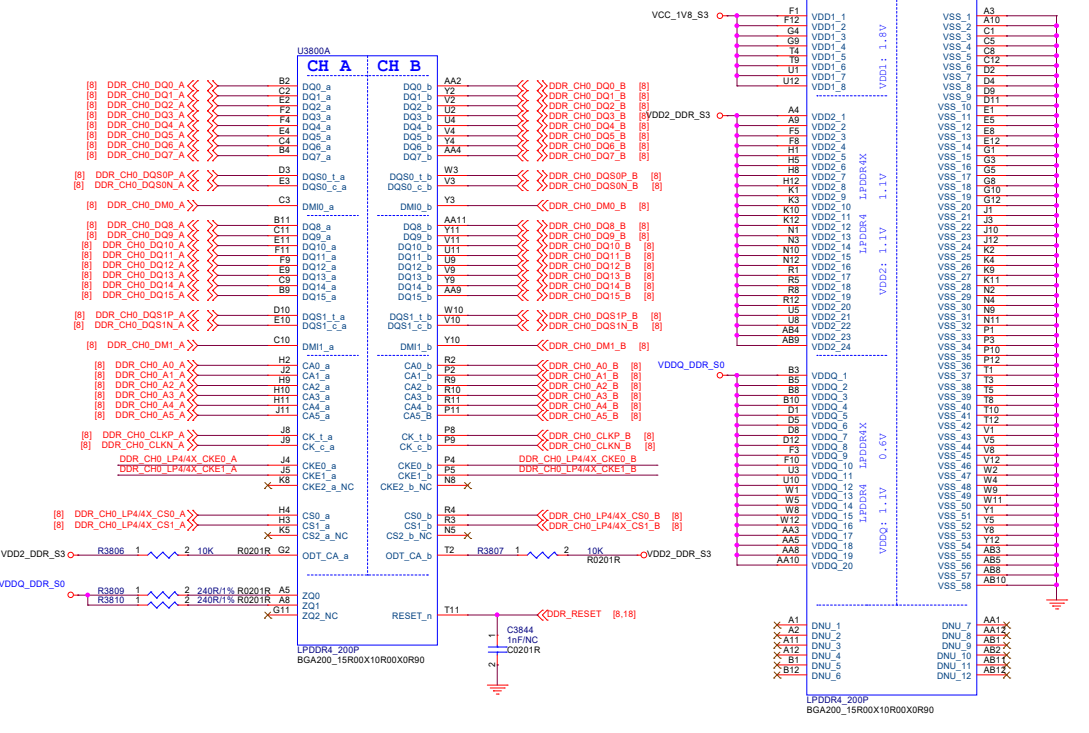
VDD_NPU



VCC_1V1_NLDO_S3



LPDDR4X



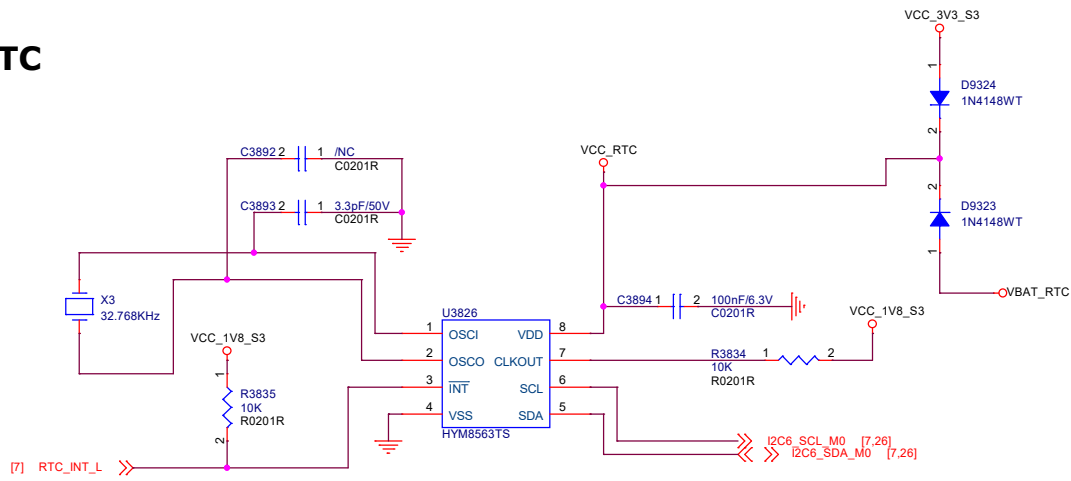
FRIENDLY ELEC

CM3588 Rev 2309

18 DRAM LPDDR4X_200P_2X32bH

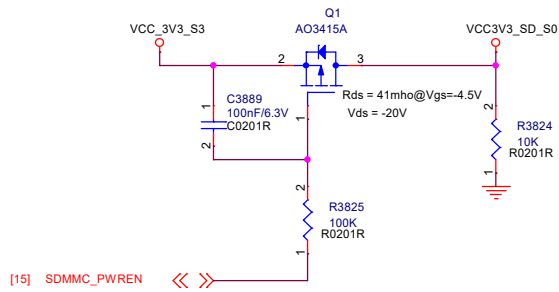
Date: 18/11/2023 Sheet: 18/26

RTC

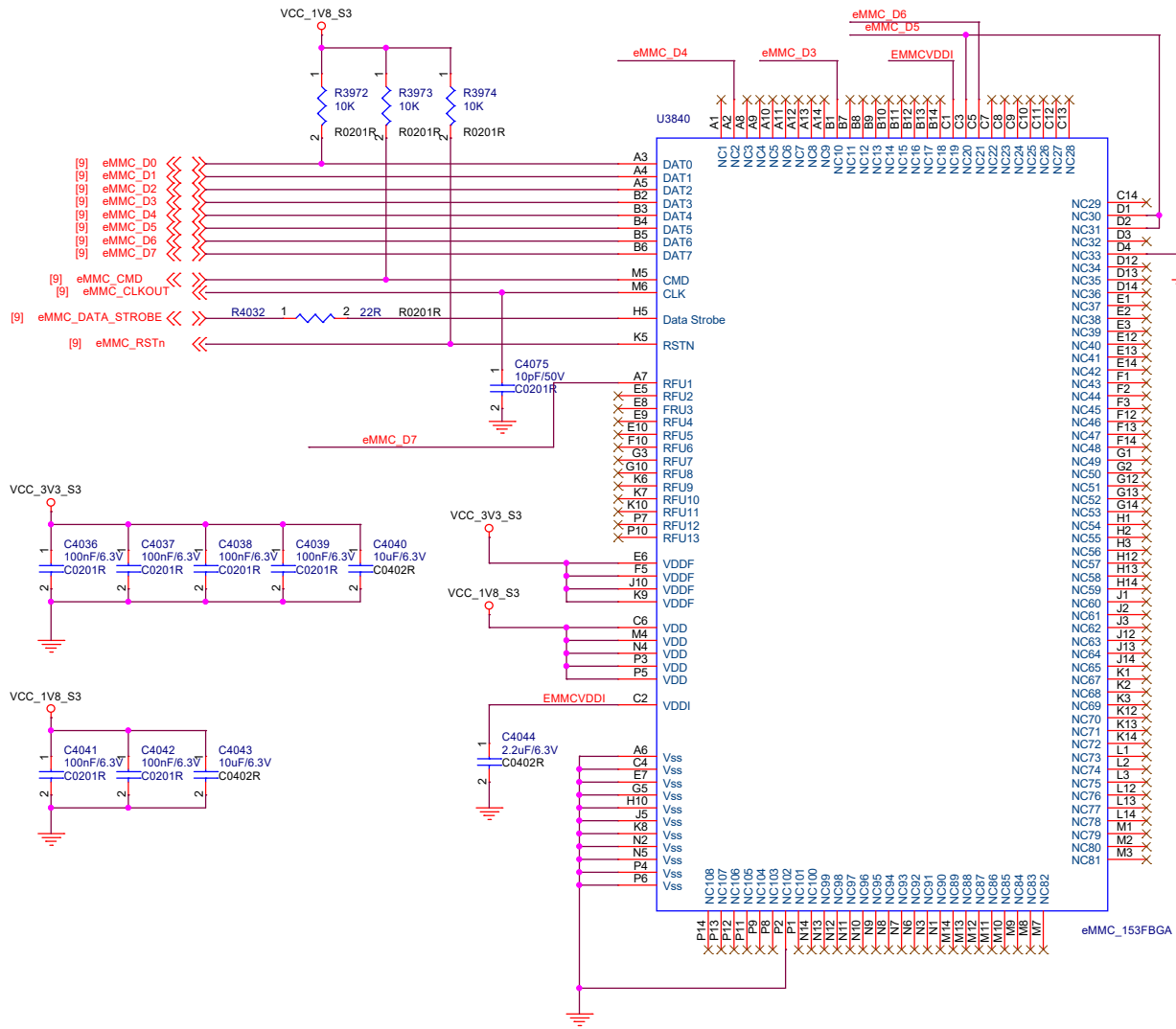


Address: Read A3H, Write A2H
7bit address: 0x51

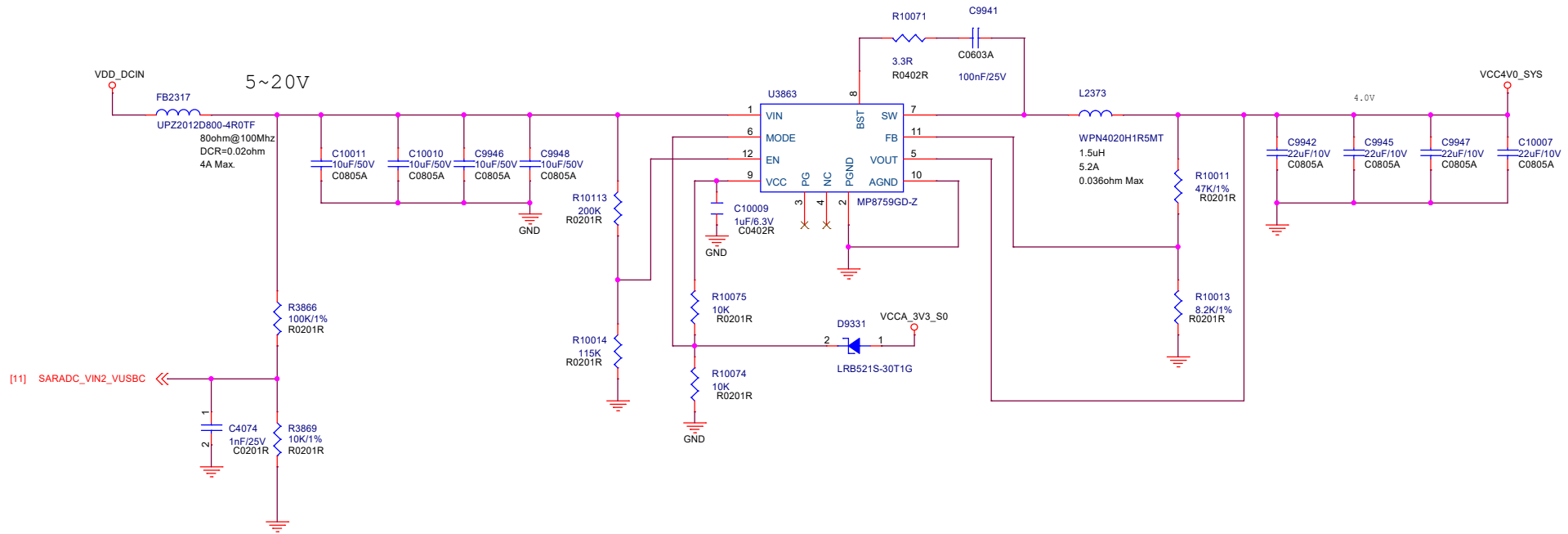
microSD Power



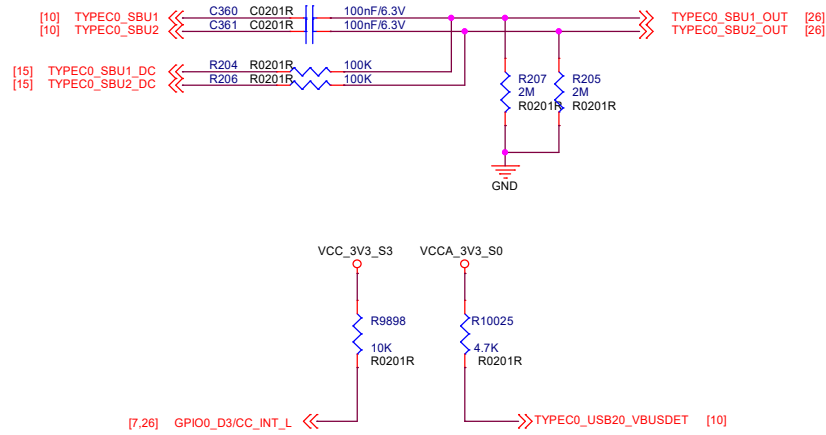
eMMC



Power IN



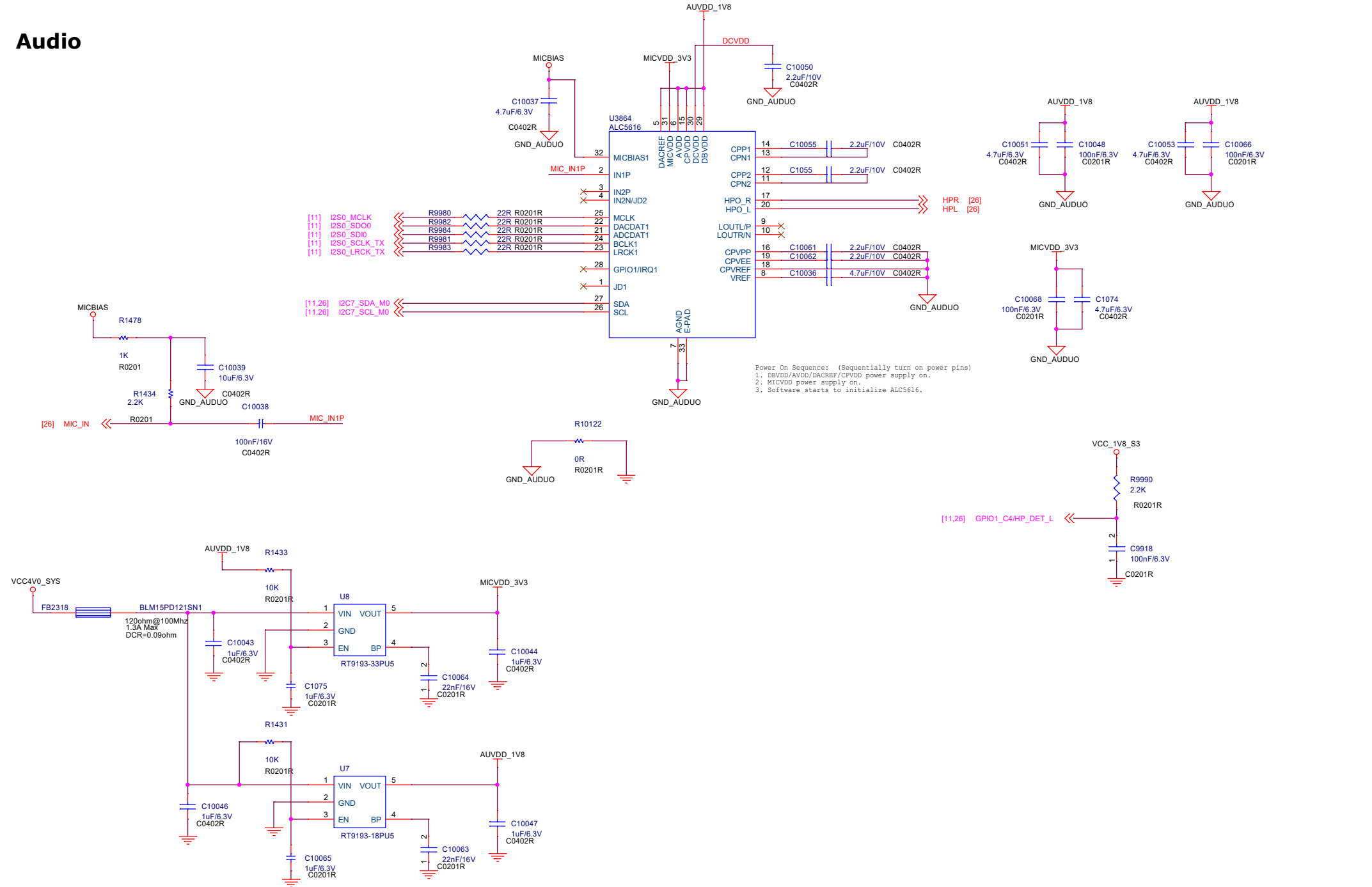
USB3.0 Type-C



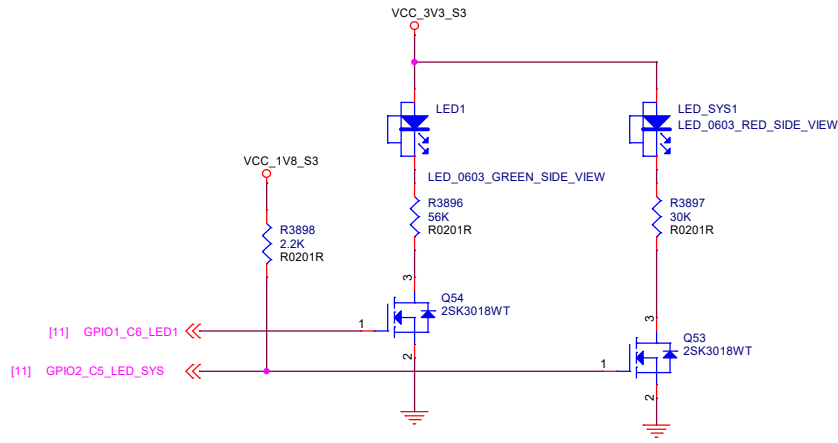
HDMI



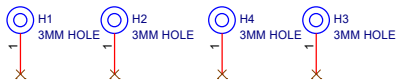
Audio



LEDs



Holes



UART0	3.3V	M0	UART9	3.3V	M1
UART1	3.3V / 1.8V	M0/M1			
UART2	3.3V	Debug Console			
UART3	3.3V / 1.8V	M0/M1			
UART4	3.3V	M2			
UART5	/	NC			
UART6	3.3V / 1.8V	M0/M1			
UART7	3.3V / 1.8V	M0/M1/M2			
UART8	3.3V	M1			

I2C0	3.3V	RK860-3 (CPU0), RK860-2 (CPU1)
I2C1	3.3V	M2
I2C2	3.3V	RK860-2 (NPU)
I2C3	3.3V / 1.8V	M0/M1/M3
I2C4	3.3V / 1.8V	M0/M1/M2/M3
I2C5	3.3V / 1.8V	M0/M3/M4
I2C6	3.3V	24AA025E48T-I/OT, HYM8563TS, FUSB302MPX
I2C7	1.8V	Codec, M0
I2C8	3.3V / 1.8V	M1/M2/M4

PWM0	3.3V / 1.8V	M1/M2	PWM9	3.3V	M0
PWM1	3.3V / 1.8V	M1/M2	PWM10	3.3V	M0
PWM2	3.3V / 1.8V	M0/M1/M2	PWM11	3.3V	M0/M1/M3
PWM3	3.3V	M0/M1/M3	PWM12	3.3V	M0/M1
PWM4	3.3V / 1.8V	M1/M0	PWM13	3.3V	M0/M1/M2
PWM5	3.3V / 1.8V	M1/M2	PWM14	3.3V	M0/M2
PWM6	1.8V	M2	PWM15	3.3V	M0/M1/M3
PWM7	1.8V	M3			
PWM8	3.3V	M0/M2			

SPI0	3.3V	M2
SPI1	3.3V / 1.8V	M0/M1
SPI2	/	NC
SPI3	/	NC
SPI4	3.3V	M1/M2

I2S0	1.8V	ALC5616 Codec
I2S1	3.3V	M0
I2S2	3.3V / 1.8V	M0/M1
I2S3	3.3V	YES

CAN0	/	NC
CAN1	3.3V	M0
CAN2	3.3V	M1

SPDIF0	3.3V	M0/M1
SPDIF1	3.3V	M0

SDIO	3.3V / 1.8V	M0/M1
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Pinout

VDD_DCIN	5-20VDC Power input, 15W max
BOOT_SARADC_IN0	Pull low to enter USB Maskrom Mode
SARADC_VIN6_HW_ID2	for Carrier Board ID
PWRON_L	Connect to PowerKey
RESET_L	RESET input to RK3588 and PMIC
PMIC_EXT_EN_OUT	Control the power of carrier board
VDC_MODE	Keep float: power up immediately after VDD_DCIN is powered Short to GND: power up after PowerKey is pressed

