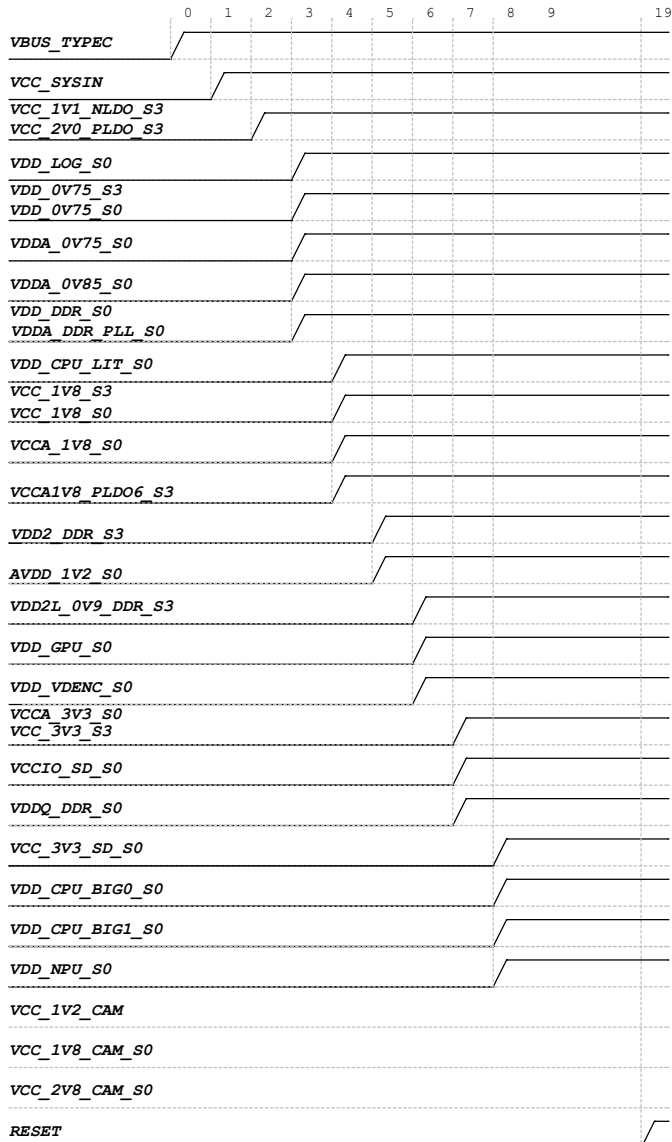


# NanoPi R6C



<b>NanoPi R6C</b>		<b>Rev</b> 2302
<b>Size</b> A3	<b>Page Name</b> 01.Title	
<b>Date:</b> Wednesday, March 08, 2023	<b>Sheet:</b> 1 / 27	

# Power Sequence

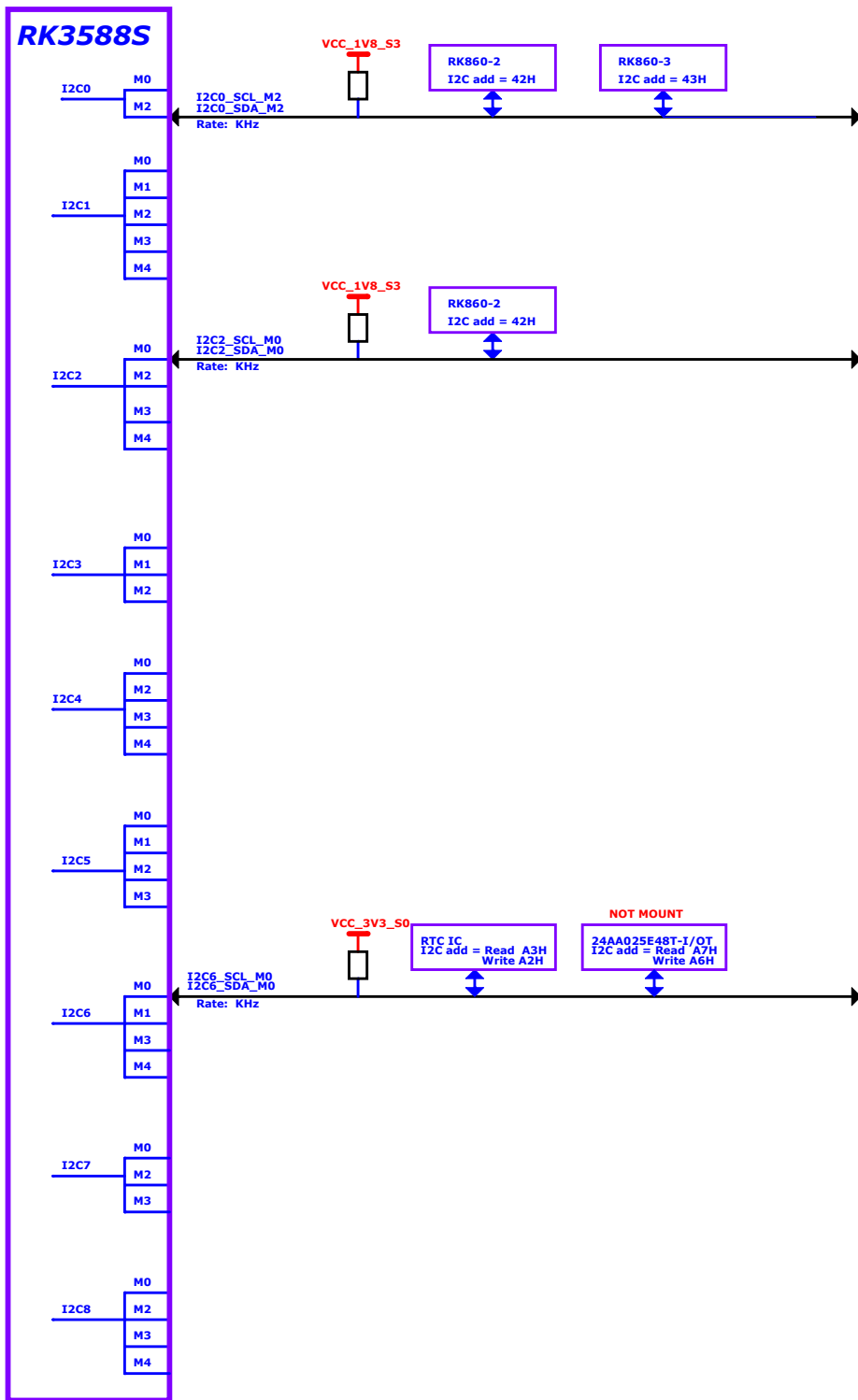


Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

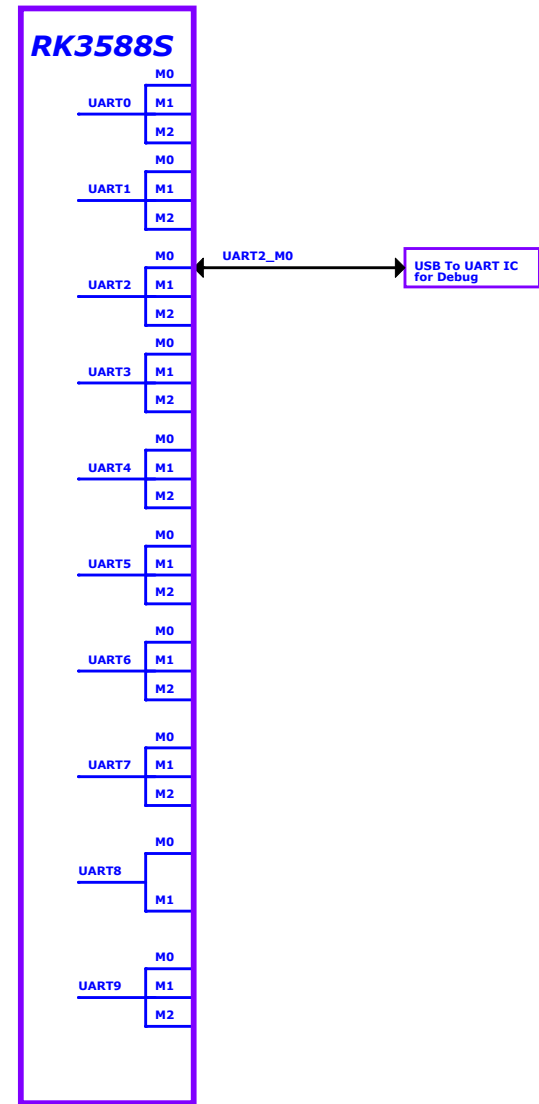
## IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
	Pin V35 V36		PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin AC35	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
	Pin AC36				
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_IO_SD	1.8V/3.3V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_3V3_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin A334	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin AL33 AM33		VCCIO6	VCC_3V3_S0	3.3V

# I2C MAP



# UART MAP

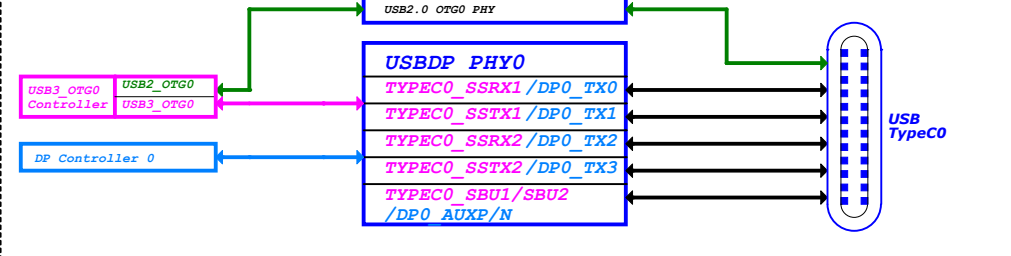


**USB Controller Configure Table**

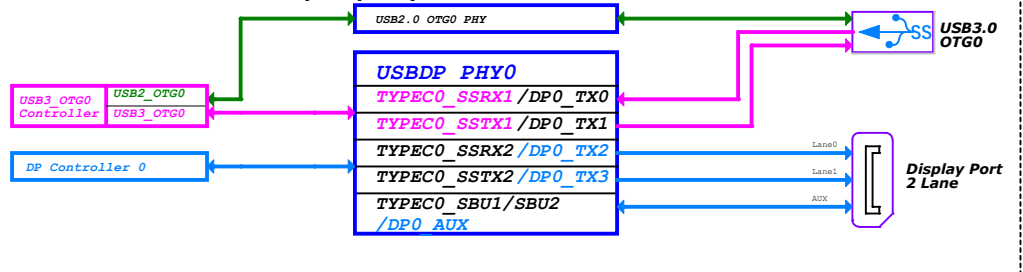
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEPC_SSR1/DP0_AUX0	TYPEPC_SSR1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEPC_SSR2/DP0_AUX1	TYPEPC_SSR2	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1
	TYPEPC_SSRX1/DP0_TX0	TYPEPC_SSRX1P	DP0_TX0P	DP0_TX0P	TYPEPC_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P
	TYPEPC_SSRX2/DP0_TX1	TYPEPC_SSRX2P	DP0_TX1P	DP0_TX1P	TYPEPC_SSRX2P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P
USB20 OTG0 Device or Host	TYPEPC_SSTX1/DP0_TX2	TYPEPC_SSTX1P	DP0_TX2P	DP0_TX2P	TYPEPC_SSTX1P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC_SSTX2/DP0_TX3	TYPEPC_SSTX2P	DP0_TX3P	DP0_TX3P	TYPEPC_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC_SBU1/SBU2	TYPEPC_SBU1P	DP0_TX4P	DP0_TX4P	TYPEPC_SBU1P	DP0_TX4P	DP0_TX4P	DP0_TX4P	DP0_TX4P	DP0_TX4P
	TYPEPC_SBU2/SBU2	TYPEPC_SBU2P	DP0_TX5P	DP0_TX5P	TYPEPC_SBU2P	DP0_TX5P	DP0_TX5P	DP0_TX5P	DP0_TX5P	DP0_TX5P
USB30 OTG2 Device or Host	PCIE20_2_RXP/SATA10_2_RXP/USB30_2_SSTXP		OPTION1 USB30 HOST	OPTION2 USB30 HOST						
	PCIE20_2_TXN/SATA10_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP	USB30_2_SSTXP	USB30_2_SSTXP	USB30_2_SSTXP				
USB20 HOST0	USB20_HOST0_DP		USB30_2_SSRXP	USB30_2_SSRXP	USB30_2_SSRXP	USB30_2_SSRXP				
	USB20_HOST0_DM		USB30_2_SSRXN	USB30_2_SSRXN	USB30_2_SSRXN	USB30_2_SSRXN				
USB20 HOST1	USB20_HOST1_DP				USB20_HOST1_DP					
	USB20_HOST1_DM				USB20_HOST1_DM					

Note:  
 DP Lane swap enable  
 0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N  
 1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

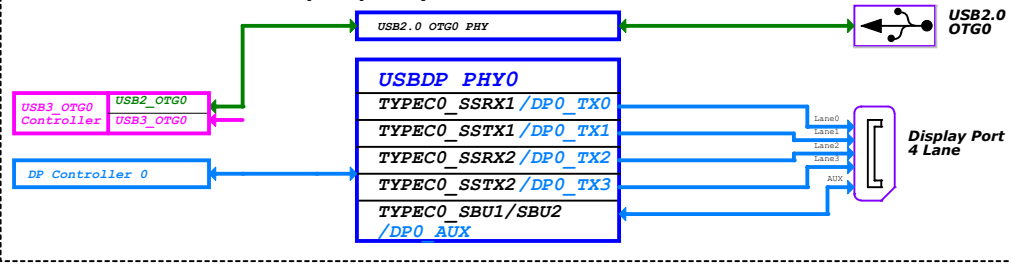
**Config0: TypeC0 (With DP function)**



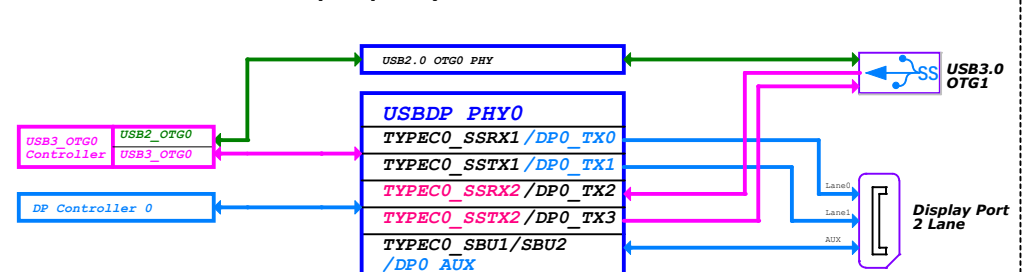
**Config3:(Default) USB3.0 OTG0 + DP0 2Lane(Swap ON)**



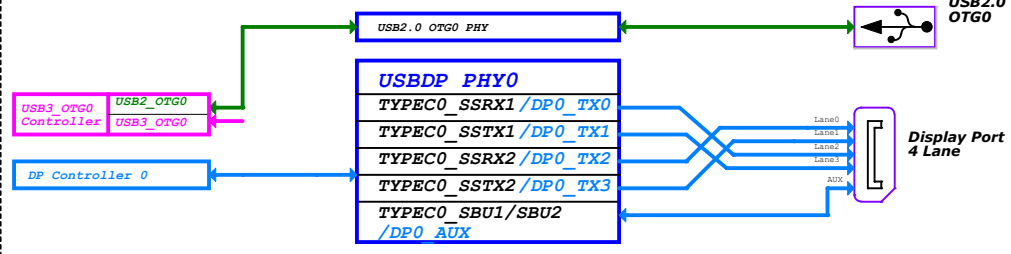
**Config1: USB2.0 OTG0 + DP0 4Lane(Swap OFF)**



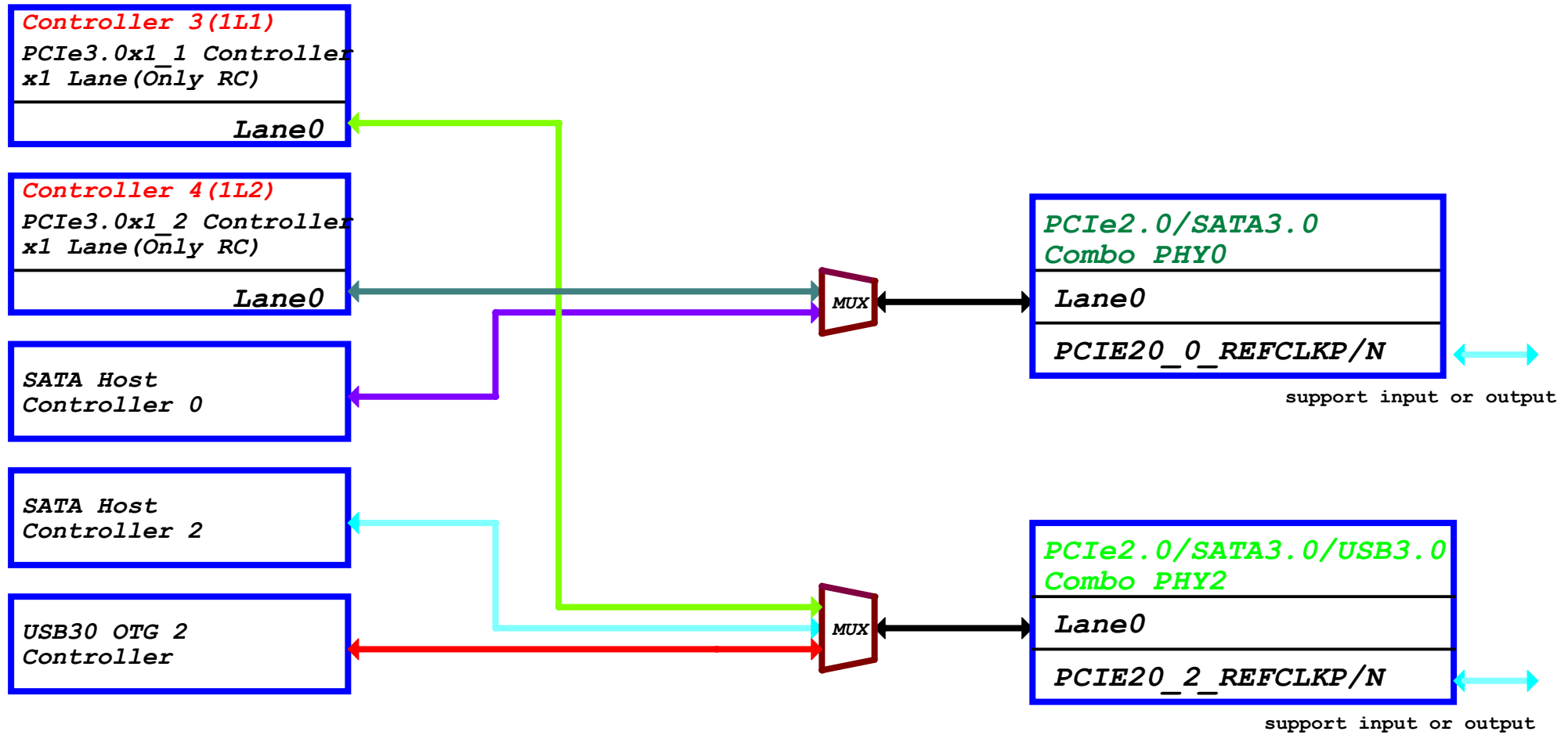
**Config4: USB3.0 OTG0 + DP0 2Lane(Swap OFF)**



**Config2: USB2.0 OTG0 + DP0 4Lane(Swap ON)**



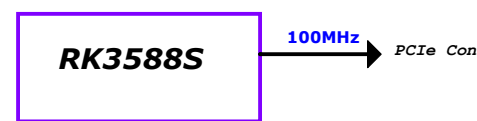
# PCIe/SATA Connecter Diagram



## PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

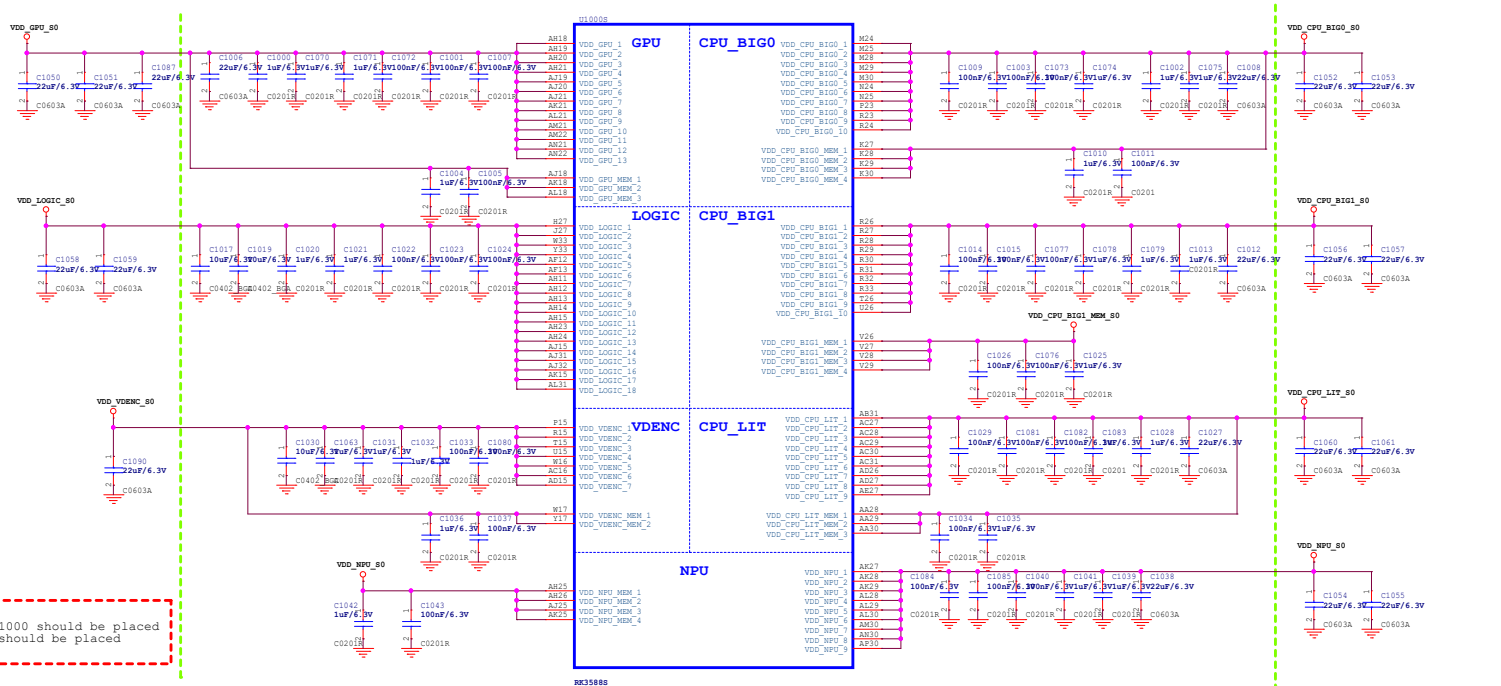
## PCIe2.0 REFCLK



### Note:

PCIE20\*\_REFCLKP/N is output or input gpio  
M\*=Mean to M0 or M1 or M2, It's the same source, Just multiplex to M0 or M1 or M2, Only use one at the same time.

# RK3588S (Power&Gnd)



**Note:**  
The Caps between green line and A1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

U1000		U900		U1000V		U1000W		U1000X		U1000Y		U1000Z	
A1 VBS 1	VBS 101	A22 VBS 101	VBS 151	B11 VBS 201	VBS 251	A10 VBS 301	VBS 351	A10 VBS 401	VBS 451	A10 VBS 501	VBS 551	A10 VBS 601	VBS 651
A2 VBS 2	VBS 102	A22 VBS 102	VBS 152	B11 VBS 202	VBS 252	A10 VBS 302	VBS 352	A10 VBS 402	VBS 452	A10 VBS 502	VBS 552	A10 VBS 602	VBS 652
B1 VBS 3	VBS 103	B21 VBS 103	VBS 153	B21 VBS 203	VBS 253	A10 VBS 303	VBS 353	A10 VBS 403	VBS 453	A10 VBS 503	VBS 553	A10 VBS 603	VBS 653
B2 VBS 4	VBS 104	B21 VBS 104	VBS 154	B21 VBS 204	VBS 254	A10 VBS 304	VBS 354	A10 VBS 404	VBS 454	A10 VBS 504	VBS 554	A10 VBS 604	VBS 654
B3 VBS 5	VBS 105	B21 VBS 105	VBS 155	B21 VBS 205	VBS 255	A10 VBS 305	VBS 355	A10 VBS 405	VBS 455	A10 VBS 505	VBS 555	A10 VBS 605	VBS 655
B4 VBS 6	VBS 106	B21 VBS 106	VBS 156	B21 VBS 206	VBS 256	A10 VBS 306	VBS 356	A10 VBS 406	VBS 456	A10 VBS 506	VBS 556	A10 VBS 606	VBS 656
B5 VBS 7	VBS 107	B21 VBS 107	VBS 157	B21 VBS 207	VBS 257	A10 VBS 307	VBS 357	A10 VBS 407	VBS 457	A10 VBS 507	VBS 557	A10 VBS 607	VBS 657
B6 VBS 8	VBS 108	B21 VBS 108	VBS 158	B21 VBS 208	VBS 258	A10 VBS 308	VBS 358	A10 VBS 408	VBS 458	A10 VBS 508	VBS 558	A10 VBS 608	VBS 658
B7 VBS 9	VBS 109	B21 VBS 109	VBS 159	B21 VBS 209	VBS 259	A10 VBS 309	VBS 359	A10 VBS 409	VBS 459	A10 VBS 509	VBS 559	A10 VBS 609	VBS 659
B8 VBS 10	VBS 110	B21 VBS 110	VBS 160	B21 VBS 210	VBS 260	A10 VBS 310	VBS 360	A10 VBS 410	VBS 460	A10 VBS 510	VBS 560	A10 VBS 610	VBS 660
B9 VBS 11	VBS 111	B21 VBS 111	VBS 161	B21 VBS 211	VBS 261	A10 VBS 311	VBS 361	A10 VBS 411	VBS 461	A10 VBS 511	VBS 561	A10 VBS 611	VBS 661
B10 VBS 12	VBS 112	B21 VBS 112	VBS 162	B21 VBS 212	VBS 262	A10 VBS 312	VBS 362	A10 VBS 412	VBS 462	A10 VBS 512	VBS 562	A10 VBS 612	VBS 662
B11 VBS 13	VBS 113	B21 VBS 113	VBS 163	B21 VBS 213	VBS 263	A10 VBS 313	VBS 363	A10 VBS 413	VBS 463	A10 VBS 513	VBS 563	A10 VBS 613	VBS 663
B12 VBS 14	VBS 114	B21 VBS 114	VBS 164	B21 VBS 214	VBS 264	A10 VBS 314	VBS 364	A10 VBS 414	VBS 464	A10 VBS 514	VBS 564	A10 VBS 614	VBS 664
B13 VBS 15	VBS 115	B21 VBS 115	VBS 165	B21 VBS 215	VBS 265	A10 VBS 315	VBS 365	A10 VBS 415	VBS 465	A10 VBS 515	VBS 565	A10 VBS 615	VBS 665
B14 VBS 16	VBS 116	B21 VBS 116	VBS 166	B21 VBS 216	VBS 266	A10 VBS 316	VBS 366	A10 VBS 416	VBS 466	A10 VBS 516	VBS 566	A10 VBS 616	VBS 666
B15 VBS 17	VBS 117	B21 VBS 117	VBS 167	B21 VBS 217	VBS 267	A10 VBS 317	VBS 367	A10 VBS 417	VBS 467	A10 VBS 517	VBS 567	A10 VBS 617	VBS 667
B16 VBS 18	VBS 118	B21 VBS 118	VBS 168	B21 VBS 218	VBS 268	A10 VBS 318	VBS 368	A10 VBS 418	VBS 468	A10 VBS 518	VBS 568	A10 VBS 618	VBS 668
B17 VBS 19	VBS 119	B21 VBS 119	VBS 169	B21 VBS 219	VBS 269	A10 VBS 319	VBS 369	A10 VBS 419	VBS 469	A10 VBS 519	VBS 569	A10 VBS 619	VBS 669
B18 VBS 20	VBS 120	B21 VBS 120	VBS 170	B21 VBS 220	VBS 270	A10 VBS 320	VBS 370	A10 VBS 420	VBS 470	A10 VBS 520	VBS 570	A10 VBS 620	VBS 670
B19 VBS 21	VBS 121	B21 VBS 121	VBS 171	B21 VBS 221	VBS 271	A10 VBS 321	VBS 371	A10 VBS 421	VBS 471	A10 VBS 521	VBS 571	A10 VBS 621	VBS 671
B20 VBS 22	VBS 122	B21 VBS 122	VBS 172	B21 VBS 222	VBS 272	A10 VBS 322	VBS 372	A10 VBS 422	VBS 472	A10 VBS 522	VBS 572	A10 VBS 622	VBS 672
B21 VBS 23	VBS 123	B21 VBS 123	VBS 173	B21 VBS 223	VBS 273	A10 VBS 323	VBS 373	A10 VBS 423	VBS 473	A10 VBS 523	VBS 573	A10 VBS 623	VBS 673
B22 VBS 24	VBS 124	B21 VBS 124	VBS 174	B21 VBS 224	VBS 274	A10 VBS 324	VBS 374	A10 VBS 424	VBS 474	A10 VBS 524	VBS 574	A10 VBS 624	VBS 674
B23 VBS 25	VBS 125	B21 VBS 125	VBS 175	B21 VBS 225	VBS 275	A10 VBS 325	VBS 375	A10 VBS 425	VBS 475	A10 VBS 525	VBS 575	A10 VBS 625	VBS 675
B24 VBS 26	VBS 126	B21 VBS 126	VBS 176	B21 VBS 226	VBS 276	A10 VBS 326	VBS 376	A10 VBS 426	VBS 476	A10 VBS 526	VBS 576	A10 VBS 626	VBS 676
B25 VBS 27	VBS 127	B21 VBS 127	VBS 177	B21 VBS 227	VBS 277	A10 VBS 327	VBS 377	A10 VBS 427	VBS 477	A10 VBS 527	VBS 577	A10 VBS 627	VBS 677
B26 VBS 28	VBS 128	B21 VBS 128	VBS 178	B21 VBS 228	VBS 278	A10 VBS 328	VBS 378	A10 VBS 428	VBS 478	A10 VBS 528	VBS 578	A10 VBS 628	VBS 678
B27 VBS 29	VBS 129	B21 VBS 129	VBS 179	B21 VBS 229	VBS 279	A10 VBS 329	VBS 379	A10 VBS 429	VBS 479	A10 VBS 529	VBS 579	A10 VBS 629	VBS 679
B28 VBS 30	VBS 130	B21 VBS 130	VBS 180	B21 VBS 230	VBS 280	A10 VBS 330	VBS 380	A10 VBS 430	VBS 480	A10 VBS 530	VBS 580	A10 VBS 630	VBS 680
B29 VBS 31	VBS 131	B21 VBS 131	VBS 181	B21 VBS 231	VBS 281	A10 VBS 331	VBS 381	A10 VBS 431	VBS 481	A10 VBS 531	VBS 581	A10 VBS 631	VBS 681
B30 VBS 32	VBS 132	B21 VBS 132	VBS 182	B21 VBS 232	VBS 282	A10 VBS 332	VBS 382	A10 VBS 432	VBS 482	A10 VBS 532	VBS 582	A10 VBS 632	VBS 682
B31 VBS 33	VBS 133	B21 VBS 133	VBS 183	B21 VBS 233	VBS 283	A10 VBS 333	VBS 383	A10 VBS 433	VBS 483	A10 VBS 533	VBS 583	A10 VBS 633	VBS 683
B32 VBS 34	VBS 134	B21 VBS 134	VBS 184	B21 VBS 234	VBS 284	A10 VBS 334	VBS 384	A10 VBS 434	VBS 484	A10 VBS 534	VBS 584	A10 VBS 634	VBS 684
B33 VBS 35	VBS 135	B21 VBS 135	VBS 185	B21 VBS 235	VBS 285	A10 VBS 335	VBS 385	A10 VBS 435	VBS 485	A10 VBS 535	VBS 585	A10 VBS 635	VBS 685
B34 VBS 36	VBS 136	B21 VBS 136	VBS 186	B21 VBS 236	VBS 286	A10 VBS 336	VBS 386	A10 VBS 436	VBS 486	A10 VBS 536	VBS 586	A10 VBS 636	VBS 686
B35 VBS 37	VBS 137	B21 VBS 137	VBS 187	B21 VBS 237	VBS 287	A10 VBS 337	VBS 387	A10 VBS 437	VBS 487	A10 VBS 537	VBS 587	A10 VBS 637	VBS 687
B36 VBS 38	VBS 138	B21 VBS 138	VBS 188	B21 VBS 238	VBS 288	A10 VBS 338	VBS 388	A10 VBS 438	VBS 488	A10 VBS 538	VBS 588	A10 VBS 638	VBS 688
B37 VBS 39	VBS 139	B21 VBS 139	VBS 189	B21 VBS 239	VBS 289	A10 VBS 339	VBS 389	A10 VBS 439	VBS 489	A10 VBS 539	VBS 589	A10 VBS 639	VBS 689
B38 VBS 40	VBS 140	B21 VBS 140	VBS 190	B21 VBS 240	VBS 290	A10 VBS 340	VBS 390	A10 VBS 440	VBS 490	A10 VBS 540	VBS 590	A10 VBS 640	VBS 690
B39 VBS 41	VBS 141	B21 VBS 141	VBS 191	B21 VBS 241	VBS 291	A10 VBS 341	VBS 391	A10 VBS 441	VBS 491	A10 VBS 541	VBS 591	A10 VBS 641	VBS 691
B40 VBS 42	VBS 142	B21 VBS 142	VBS 192	B21 VBS 242	VBS 292	A10 VBS 342	VBS 392	A10 VBS 442	VBS 492	A10 VBS 542	VBS 592	A10 VBS 642	VBS 692
B41 VBS 43	VBS 143	B21 VBS 143	VBS 193	B21 VBS 243	VBS 293	A10 VBS 343	VBS 393	A10 VBS 443	VBS 493	A10 VBS 543	VBS 593	A10 VBS 643	VBS 693
B42 VBS 44	VBS 144	B21 VBS 144	VBS 194	B21 VBS 244	VBS 294	A10 VBS 344	VBS 394	A10 VBS 444	VBS 494	A10 VBS 544	VBS 594	A10 VBS 644	VBS 694
B43 VBS 45	VBS 145	B21 VBS 145	VBS 195	B21 VBS 245	VBS 295	A10 VBS 345	VBS 395	A10 VBS 445	VBS 495	A10 VBS 545	VBS 595	A10 VBS 645	VBS 695
B44 VBS 46	VBS 146	B21 VBS 146	VBS 196	B21 VBS 246	VBS 296	A10 VBS 346	VBS 396	A10 VBS 446	VBS 496	A10 VBS 546	VBS 596	A10 VBS 646	VBS 696
B45 VBS 47	VBS 147	B21 VBS 147	VBS 197	B21 VBS 247	VBS 297	A10 VBS 347	VBS 397	A10 VBS 447	VBS 497	A10 VBS 547	VBS 597	A10 VBS 647	VBS 697
B46 VBS 48	VBS 148	B21 VBS 148	VBS 198	B21 VBS 248	VBS 298	A10 VBS 348	VBS 398	A10 VBS 448	VBS 498	A10 VBS 548	VBS 598	A10 VBS 648	VBS 698
B47 VBS 49	VBS 149	B21 VBS 149	VBS 199	B21 VBS 249	VBS 299	A10 VBS 349	VBS 399	A10 VBS 449	VBS 499	A10 VBS 549	VBS 599	A10 VBS 649	VBS 699
B48 VBS 50	VBS 150	B21 VBS 150	VBS 200	B21 VBS 250	VBS 300	A10 VBS 350	VBS 400	A10 VBS 450	VBS 500	A10 VBS 550	VBS 600	A10 VBS 650	VBS 700

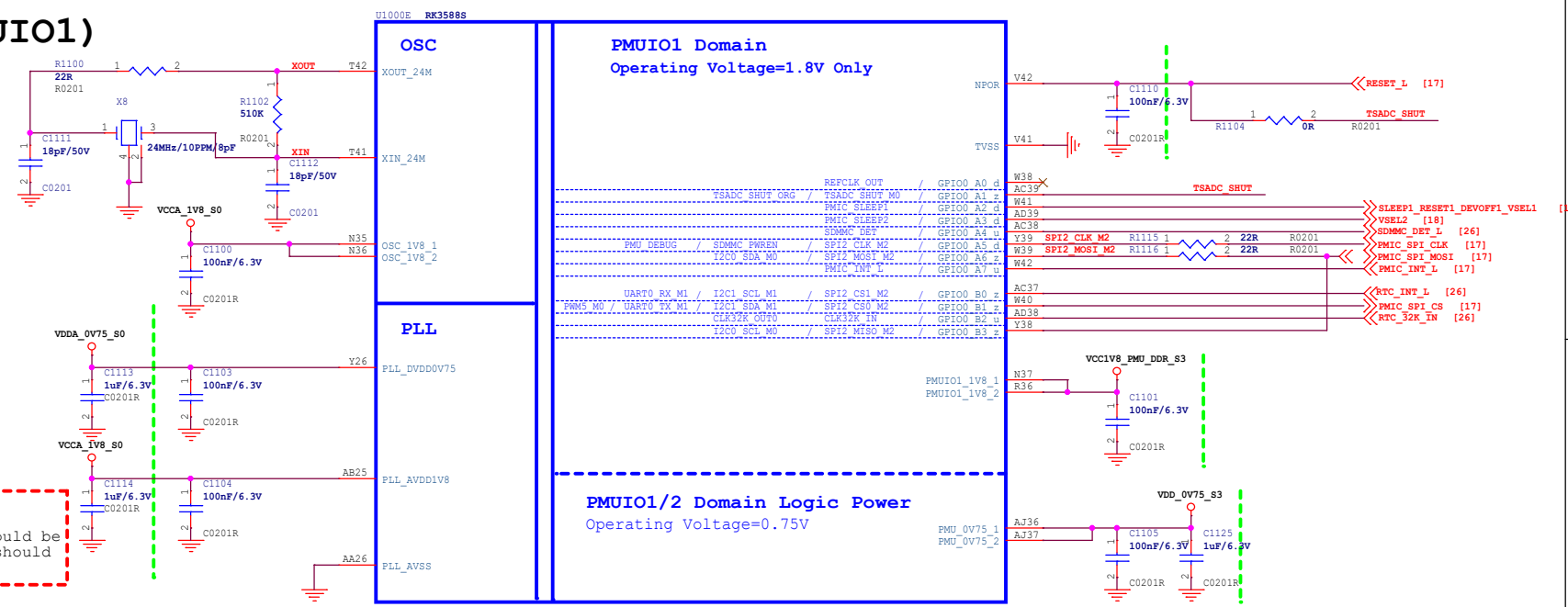
# RK3588S (OSC/PLL/PMUIO1)

**Note:**  
Adjusted the load capacitance according to the crystal specification

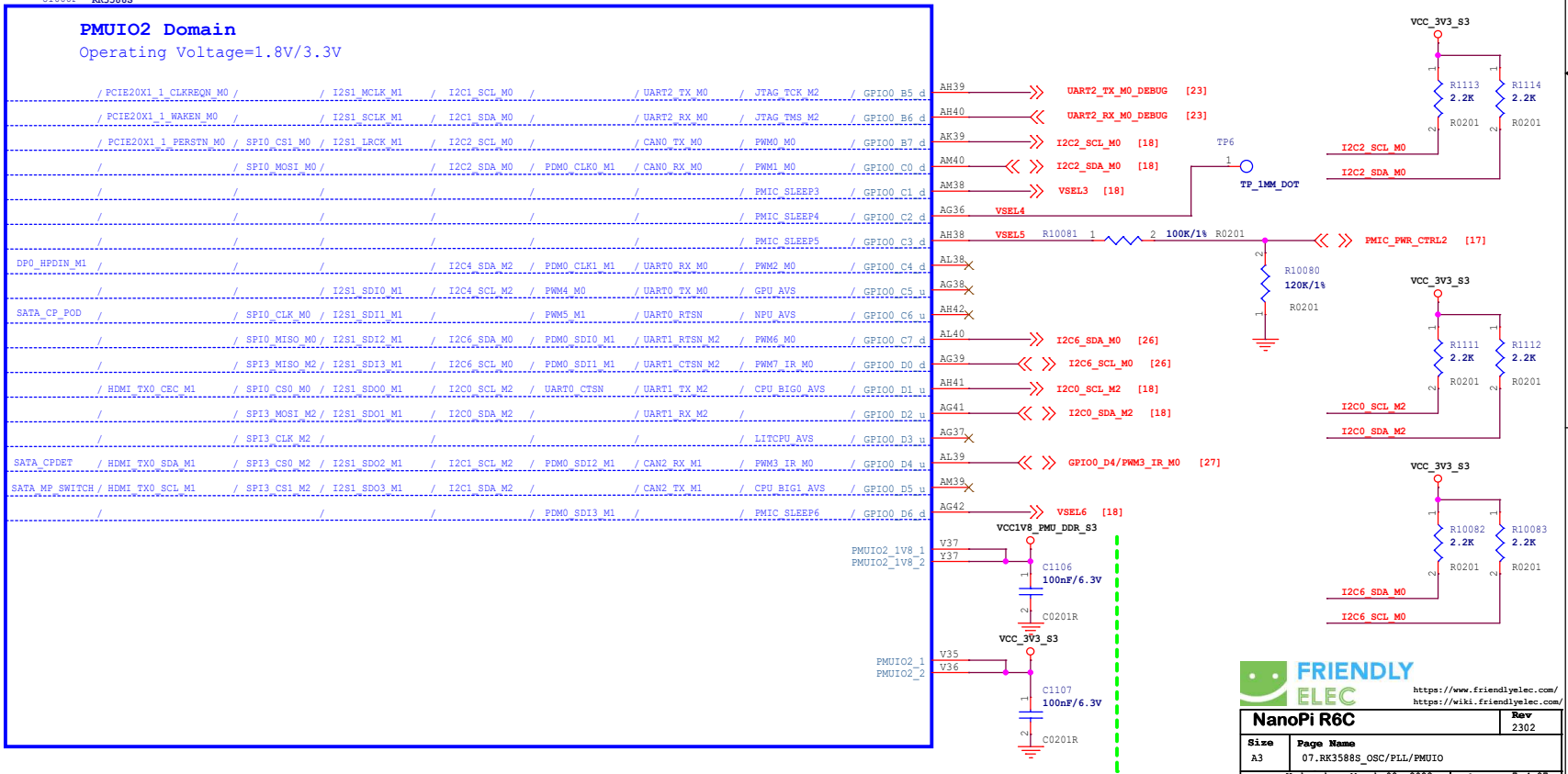
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$   
Total CL <= 12pF

**Note:**  
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

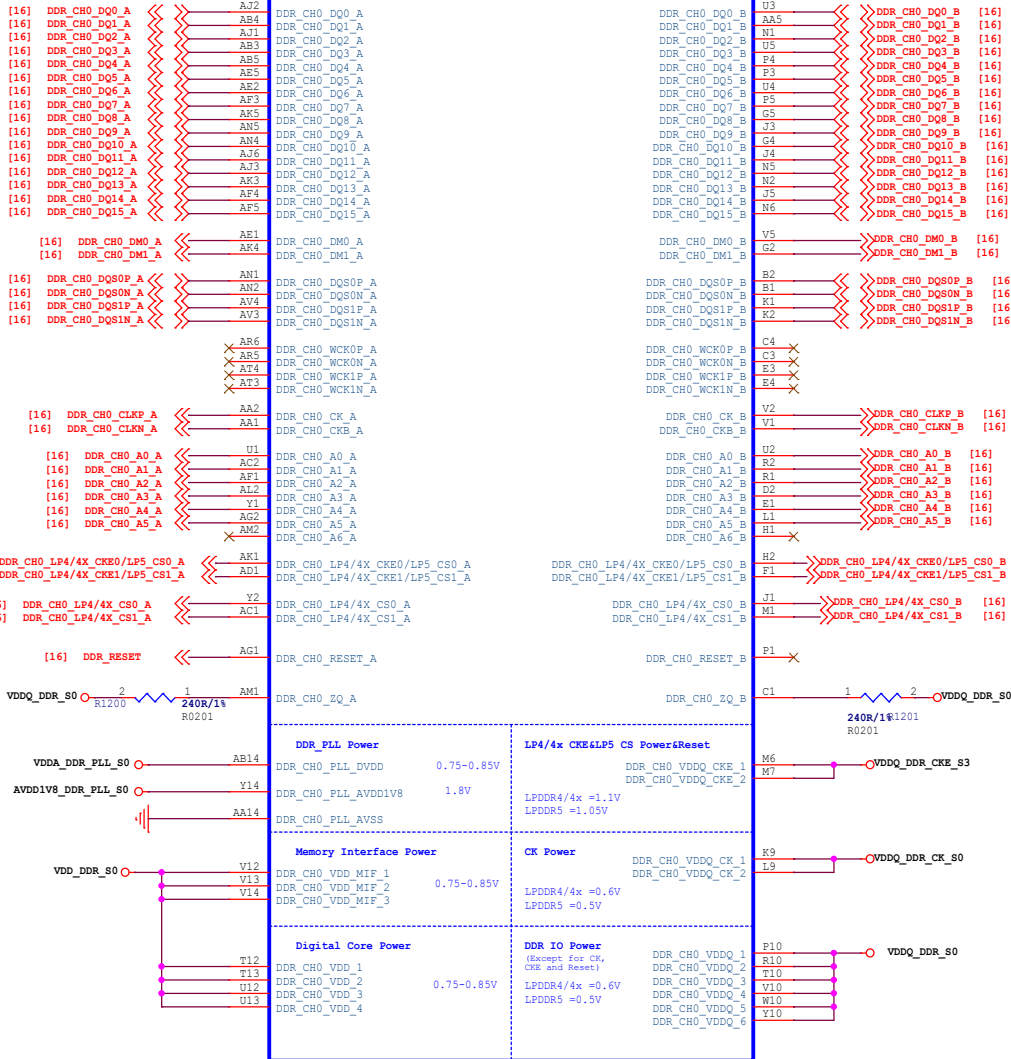


# RK3588S (PMUIO2)

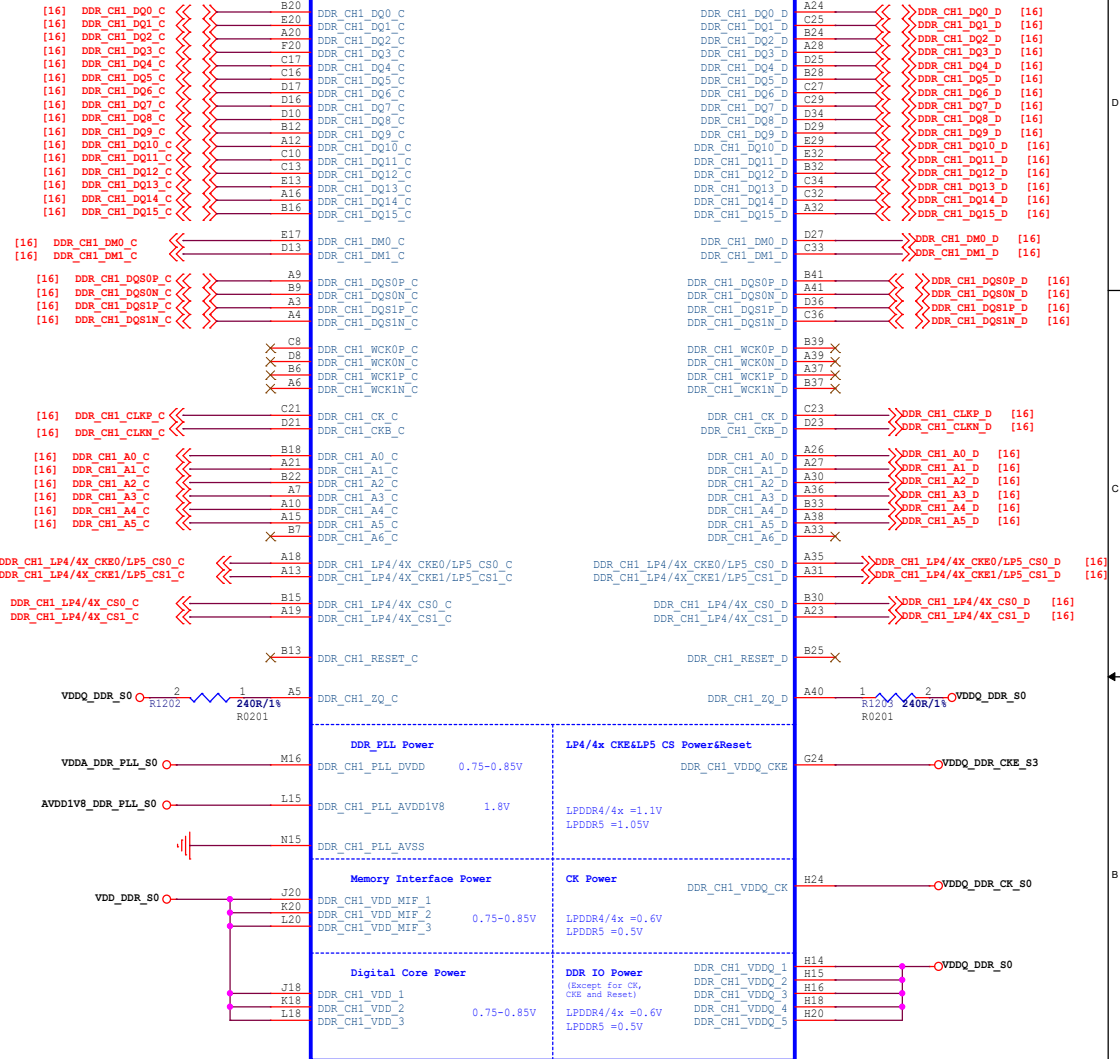


# RK3588S (DDR PHY)

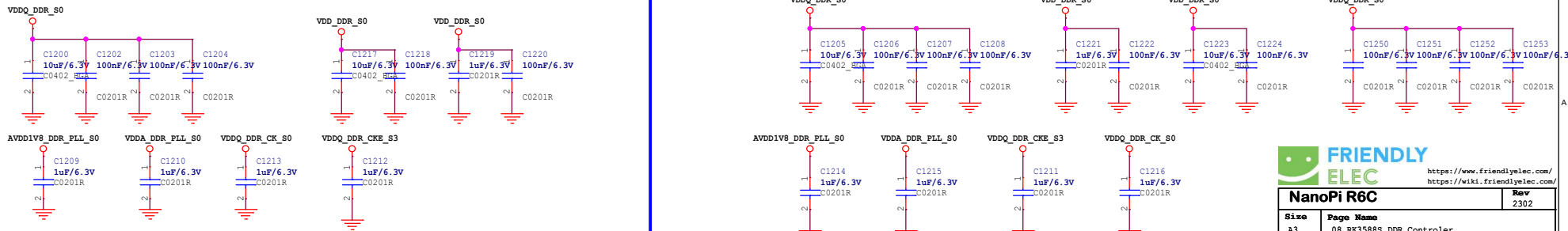
U1000A RK3588S



U1000B RK3588S

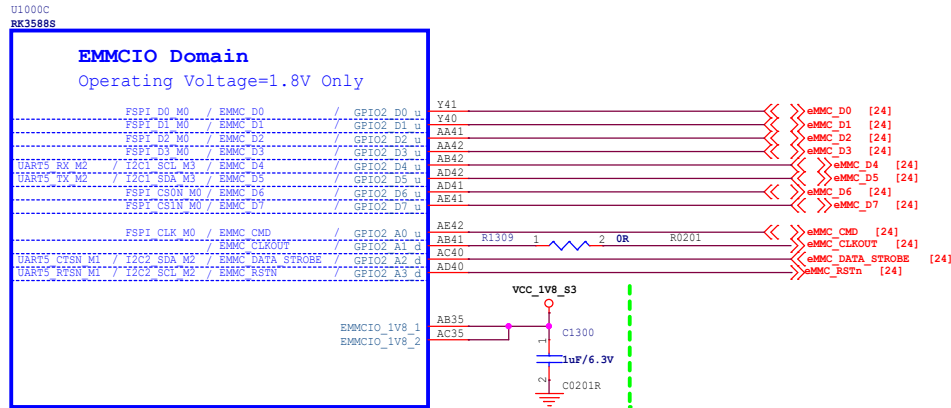


## DDR FILTER

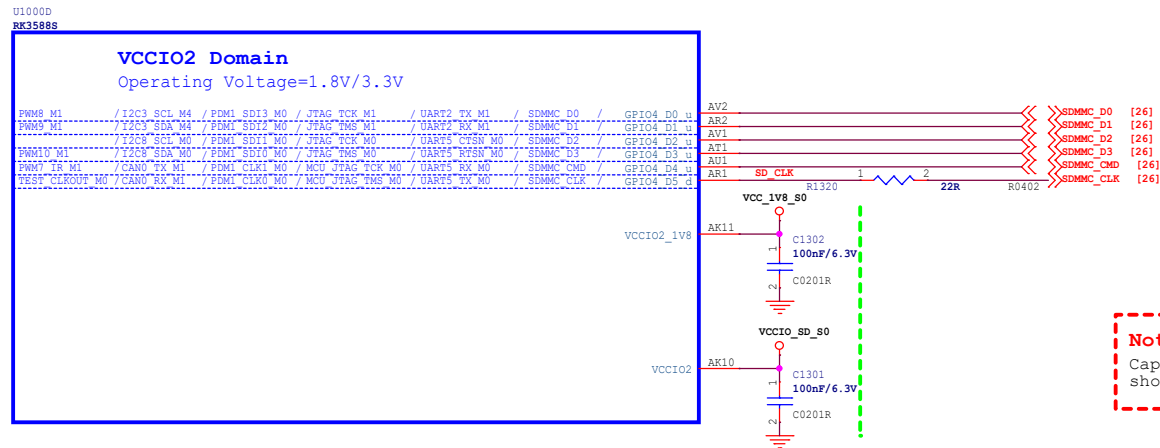




# RK3588S (EMMCIO Domain)



# RK3588S (VCCIO2 Domain)



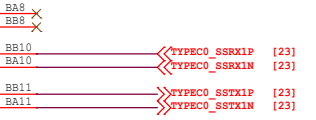
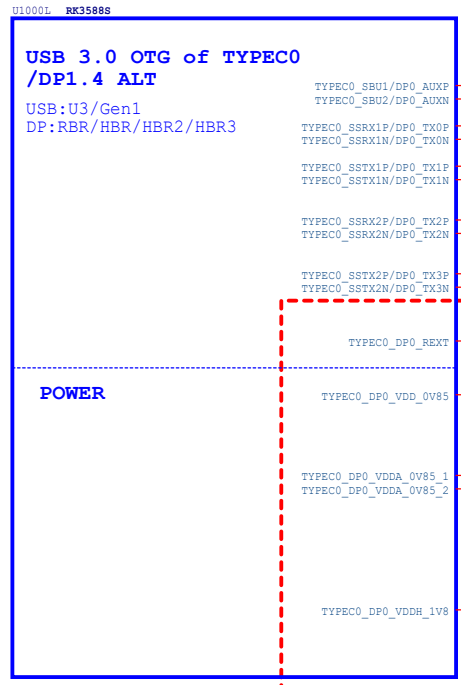
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

# RK3588S (USB3.0/DP1.4)

## USB30/DP1.4 Alt Mode Configuration

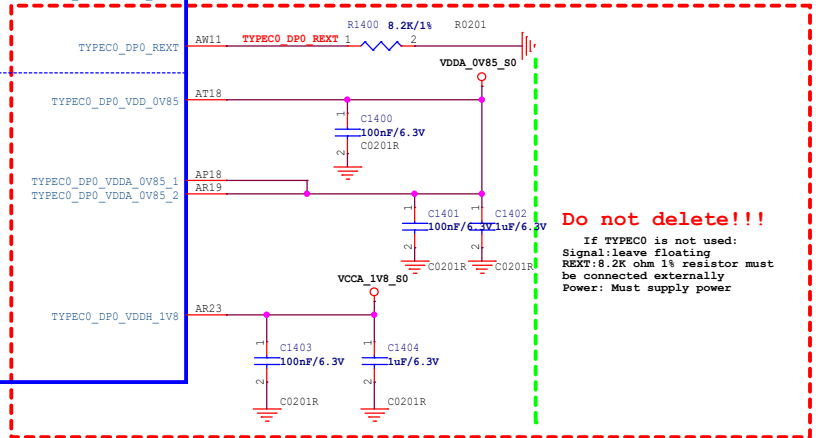
Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1

DP Lane  
Swap Off:  
Lane0/1/2/3\_TXdata mapping to Lane0/1/2/3\_TXDP/N  
Swap On:  
Lane0/1/2/3\_TXdata mapping to Lane2/3/0/1\_TXDP/N



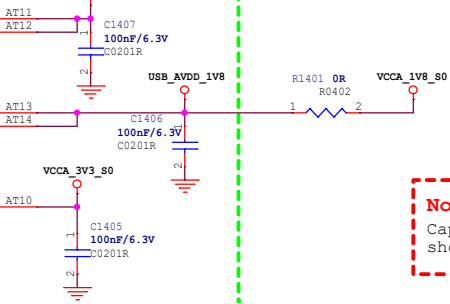
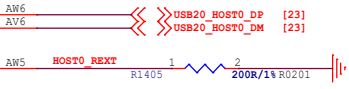
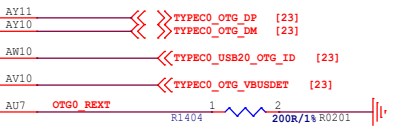
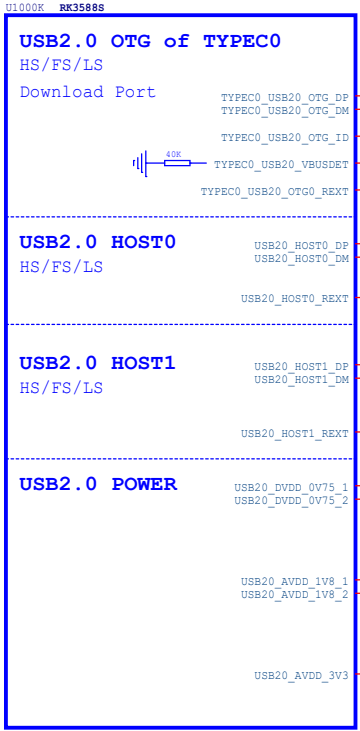
**TYPEC&DP MUX Differential Pair:**  
DATE:95 Ohm +/-10%  
For Typec

**USB30 Differential Pair:** DP Differential Pair:  
DATE:90 Ohm +/-10% DATE:100 Ohm +/-10%  
For USB30 For DP



**Do not delete!!!**  
If TYPECO is not used:  
Signal:leave floating  
REXT:8.2K ohm 1% resistor must be connected externally  
Power: Must supply power

# RK3588S (USB2.0)



**USB20 Differential Pair:**  
DATE:90 Ohm +/-10%

**Note:**  
The USB20\_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

**Note:**  
**TYPECO\_USB20\_OTG:**  
DP/DM:Must used for download  
ID:According to demand,if not used,Leave floating  
VBUSDET:Must provide  
REXT:200ohm 1% resistor must be connected externally  
Power: Must supply power

**USB20\_HOST0/USB20\_HOST1:**  
If not used:  
DP/DM:Leave floating  
REXT:Leave floating

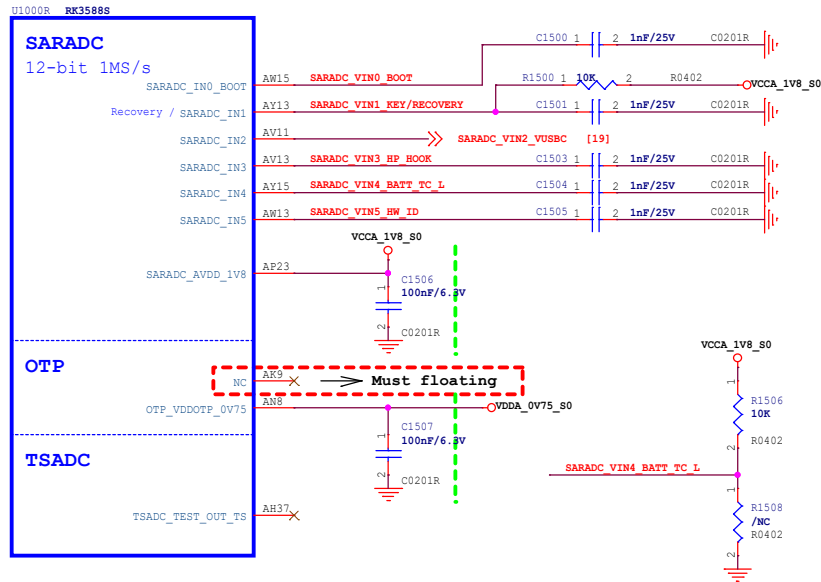
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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https://wiki.friendlyelec.com/

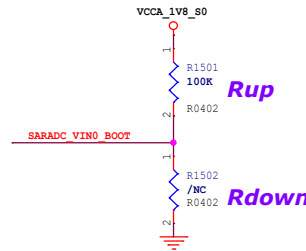
<b>NanoPi R6C</b>		Rev 2302
Size A3	Page Name 10_RK3588S_USB20/USB30/DP_PHY	
Date: Wednesday, March 08, 2023	Sheet: 10/ 27	

# RK3588S (SARADC/OTP/TSADC)

← SARADC\_VIN0\_BOOT [27]

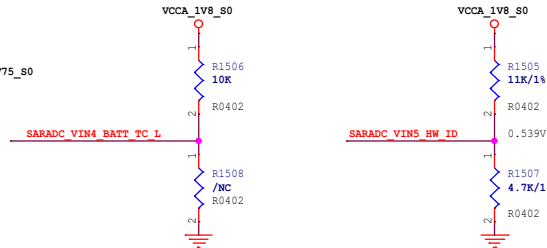


## BOOT MODE CONFIG



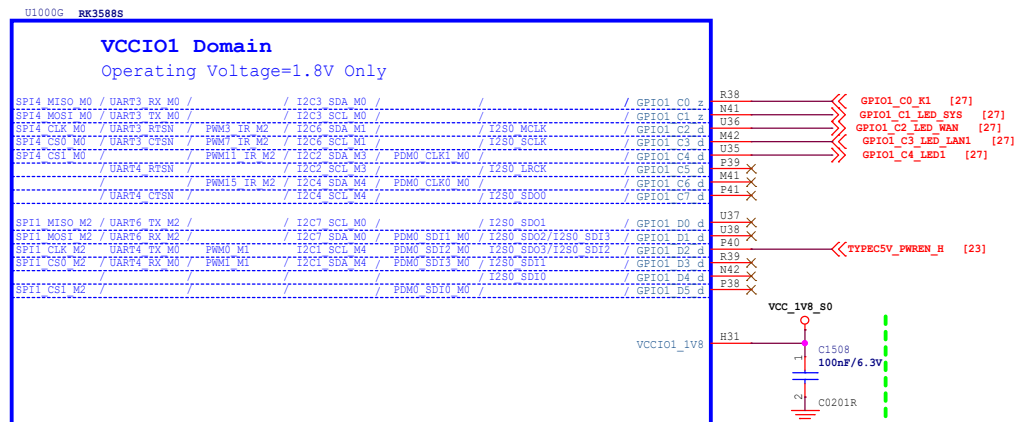
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

## BOARD ID CONFIG



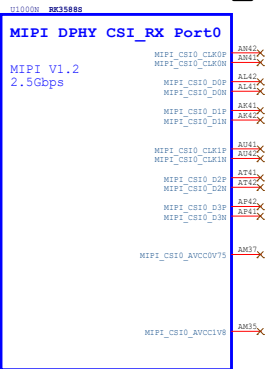
	0.539V (8GB)	0.887V (4GB)
R1505	11K/1%	11K/1%
R1507	4.7K/1%	6.8K/1%

# RK3588S (VCCIO1 Domain)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

# RK3588S (MIPI\_DPHY CSIO RX)



MIPI CSI Differential Pair:  
100 Ohm +/-10%

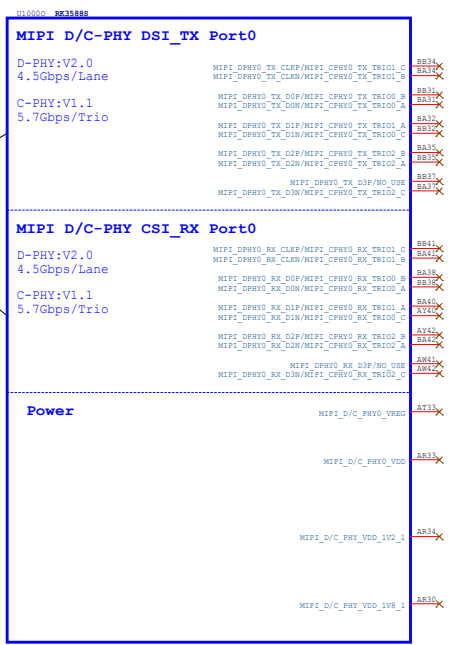
**Note:**  
If not used:  
Signal:leave floating  
Power: Floating

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0  MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

**Note:**  
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

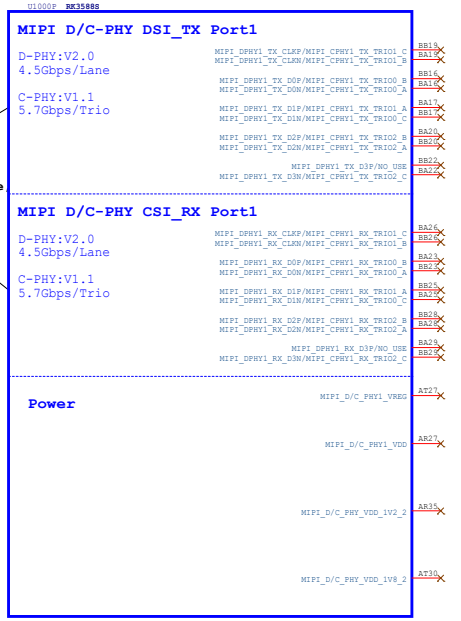
# RK3588S (MIPI\_D/C PHY0)



TX and RX port must work in the same mode, DPHY or CPHY

**Note:**  
If not used:  
Signal:leave floating  
Power: Floating

# RK3588S (MIPI\_D/C PHY1)



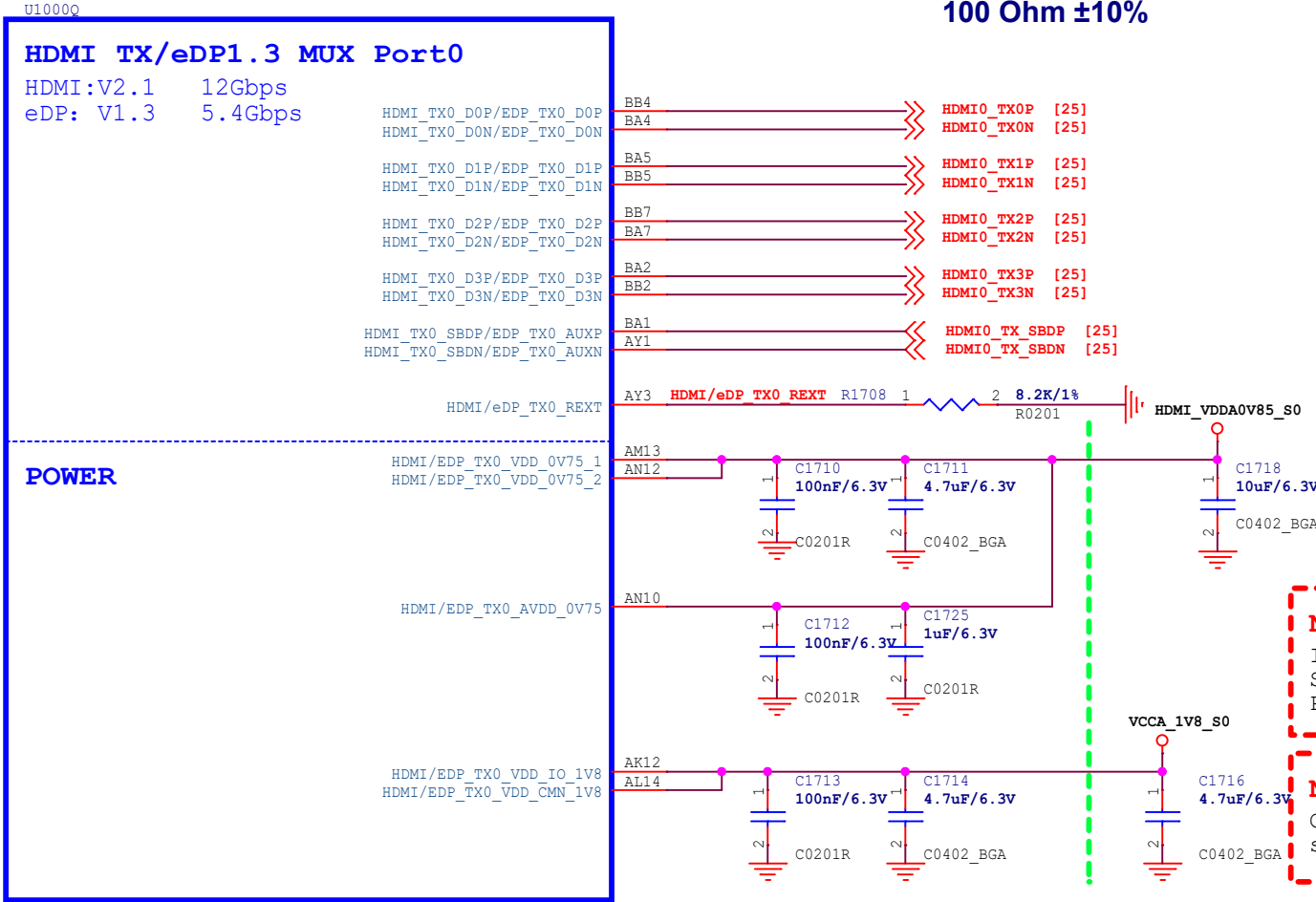
TX and RX port must work in the same mode DPHY or CPHY

**Note:**  
If not used:  
Signal:leave floating  
Power: Floating

# RK3588S (HDMI2.1 TX/eDP1.3 TX)

**Note:**  
 The HDMI2.1 trace length is less than 100mm.  
 The HDMI2.1 differential trace impedance is 100 OHM.

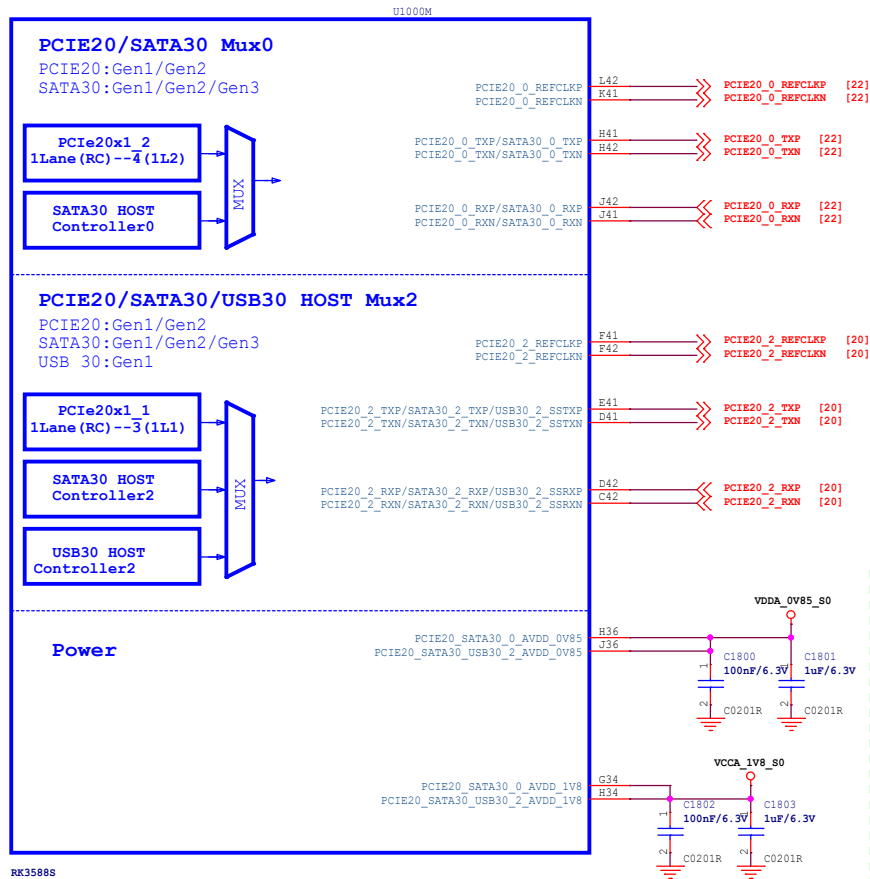
**HDMI TX**  
 100 Ohm ±10%



**Note:**  
 If not used:  
 Signal: leave floating  
 Power: Floating or tie to VSS

**Note:**  
 Caps of between dashed green lines and U1000 should be placed under the U1000 package

# RK3588S (PCIE20/SATA30/USB30)



**CLK Differential Pair:**  
 100 Ohm±10%  
**DATA Differential Pair:**  
 PCIe20: 85 Ohm±10%  
 SATA30: 100 Ohm±10%  
 USB30: 90ohm±10%

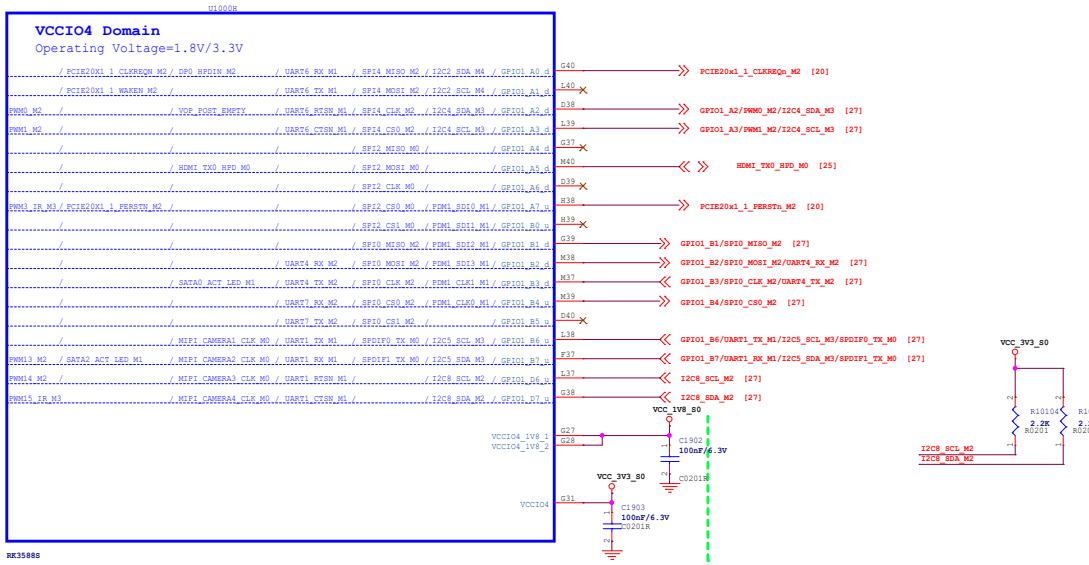
**Note:**  
 If not used:  
 Signal: leave floating  
 Power: Tie to VSS

**Note:**  
 Caps of between dashed green lines and U1000  
 should be placed under the U1000 package

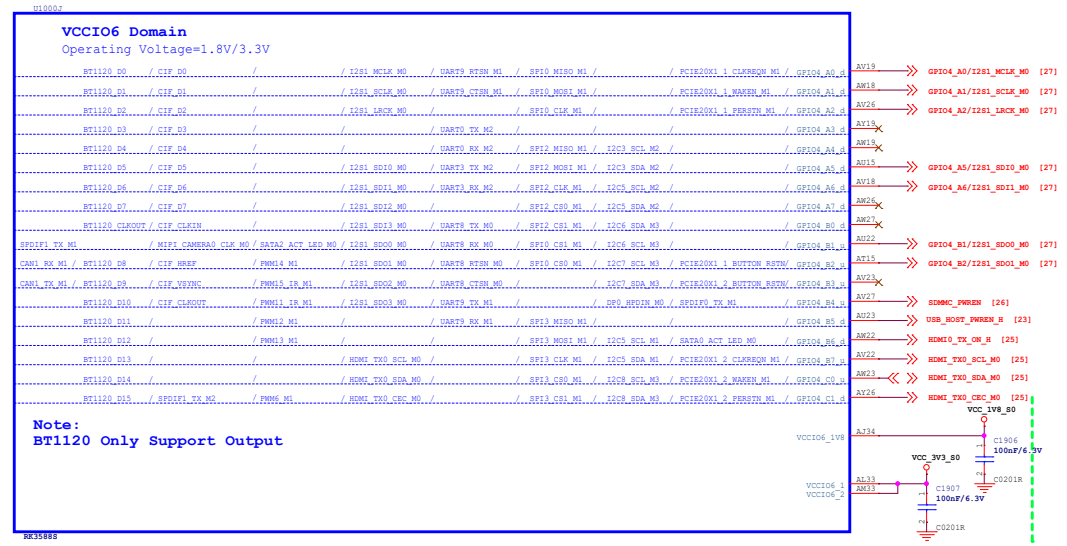
## PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

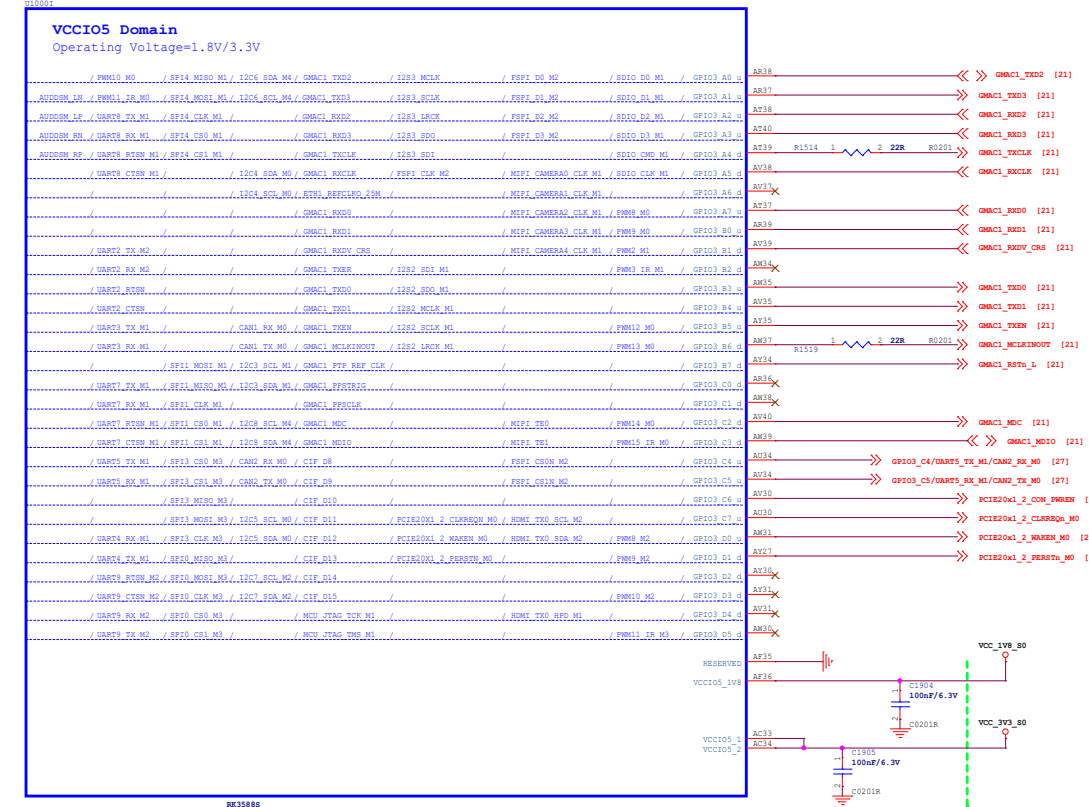
# RK3588S (VCCIO4 Domain)



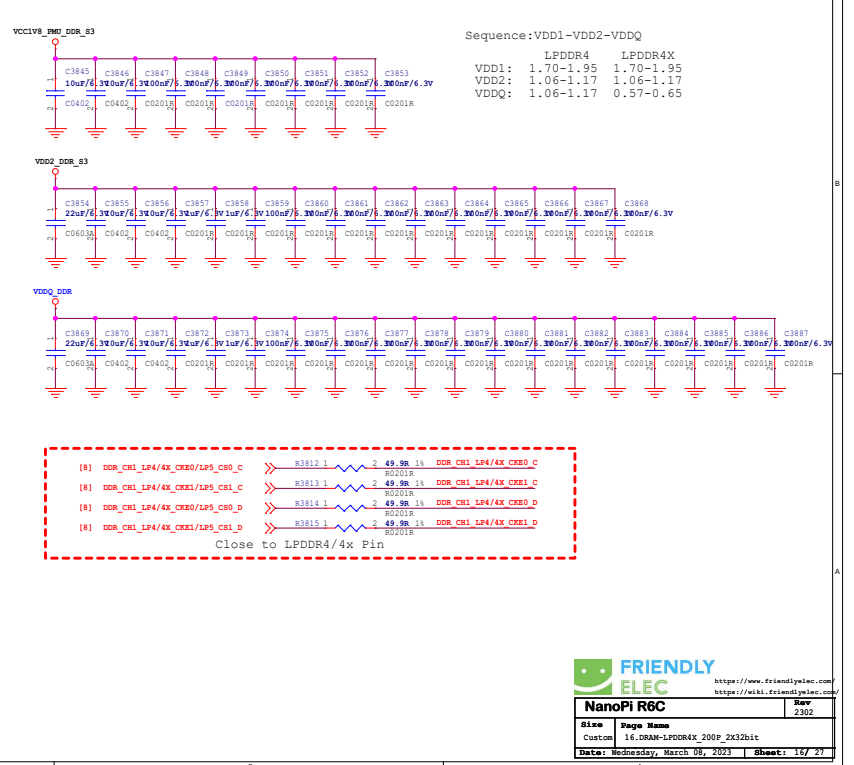
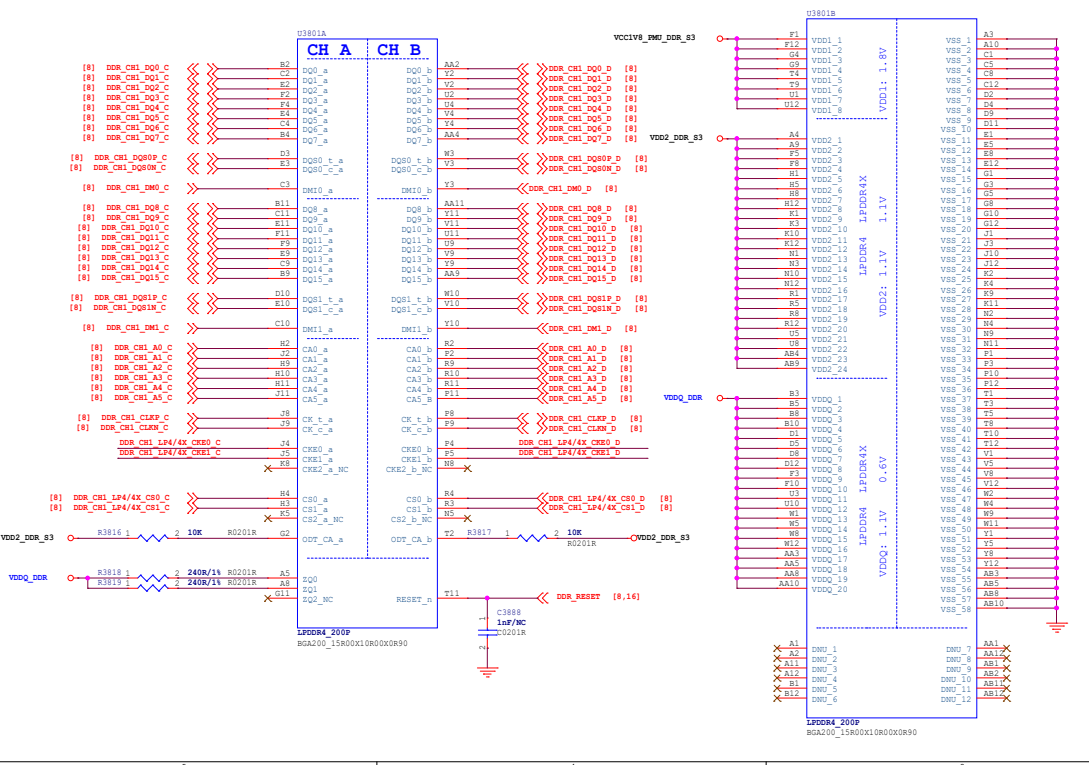
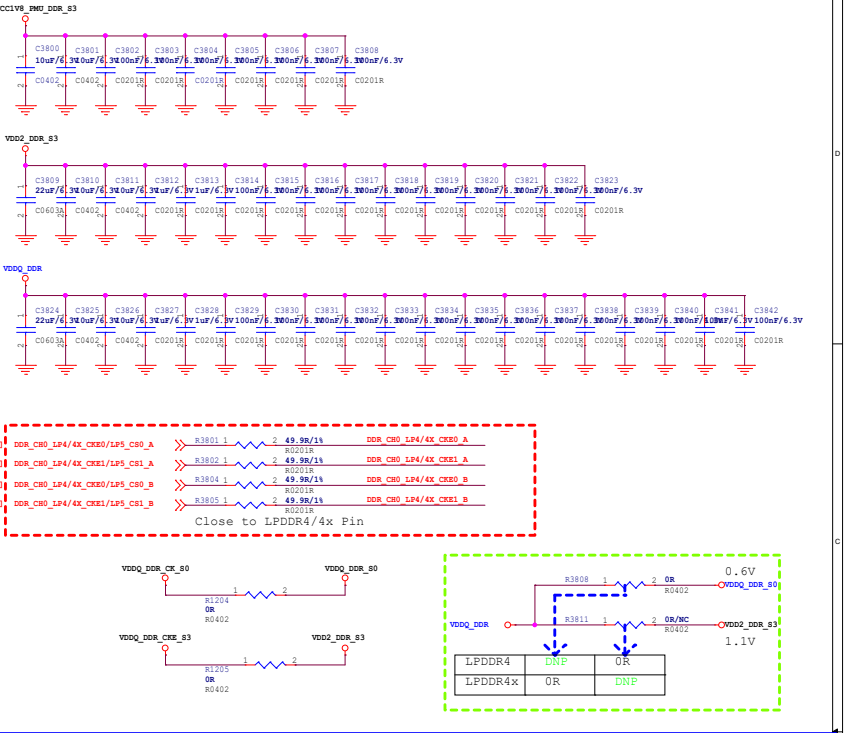
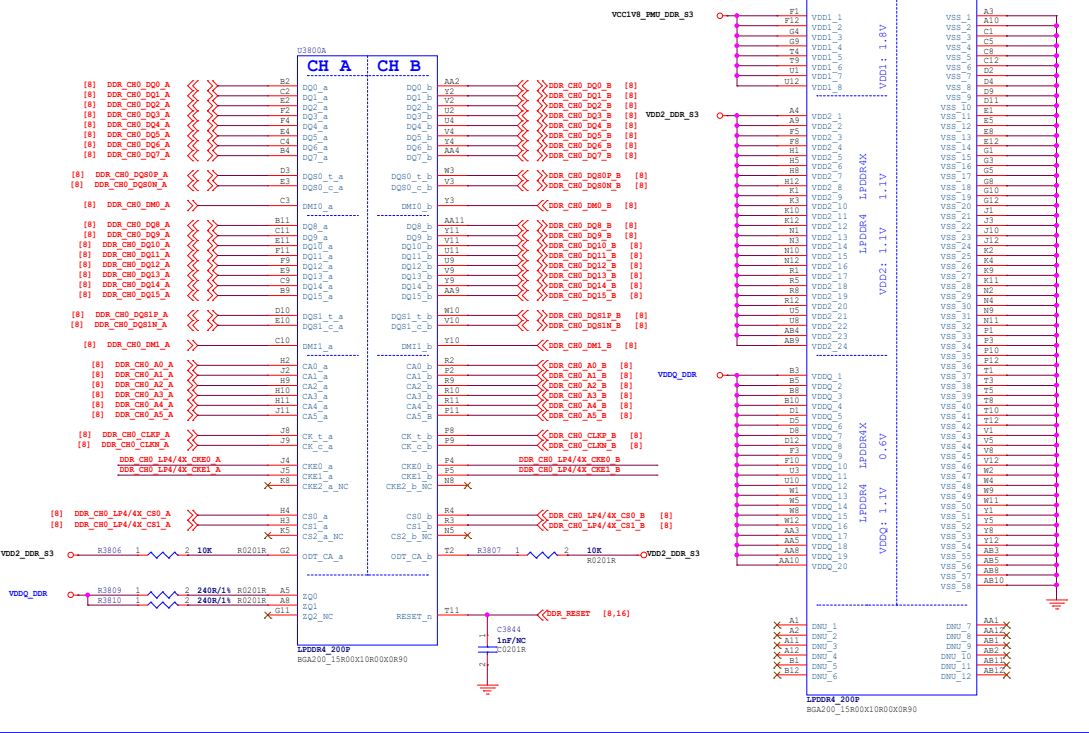
# RK3588S (VCCIO6 Domain)



# RK3588S (VCCIO5 Domain)



LPDDR4/4X



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**NanoPi R6C**  
Rev 2302

Blank Page Name  
Custom 16-GRAM-LPDDR4X\_200P\_2x32bit  
Date: Wednesday, March 08, 2023 8:56:21 AM



# PMIC RK806-1 BUCK

- PMIC\_SPI\_CS [7]
- PMIC\_SPI\_MOSI [7]
- PMIC\_SPI\_CLK [7]
- SLEEP1\_RESET1\_DEVOPFI\_VSEL1 [7]
- PMIC\_INT\_L [7]
- RESET\_L [7]
- PMIC\_EXT\_EN\_OUT [18]
- PMIC\_PWR\_CTRL2 [7]

Default: 0.85V  
Low frequency: 0.85V-->0.75V

Default: 1.1V

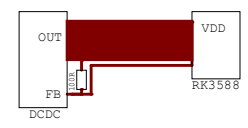
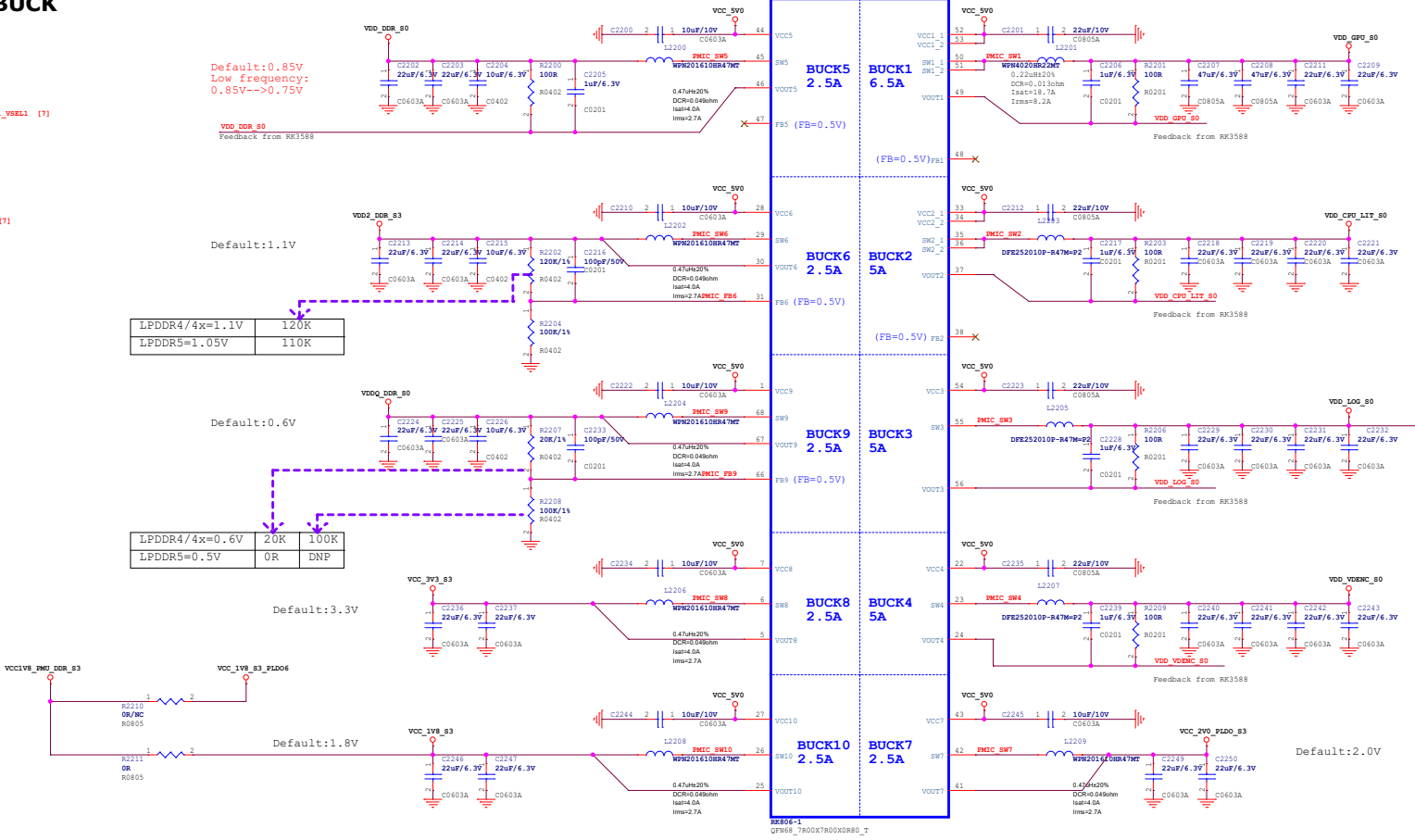
Default: 0.6V

Default: 3.3V

Default: 1.8V

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP



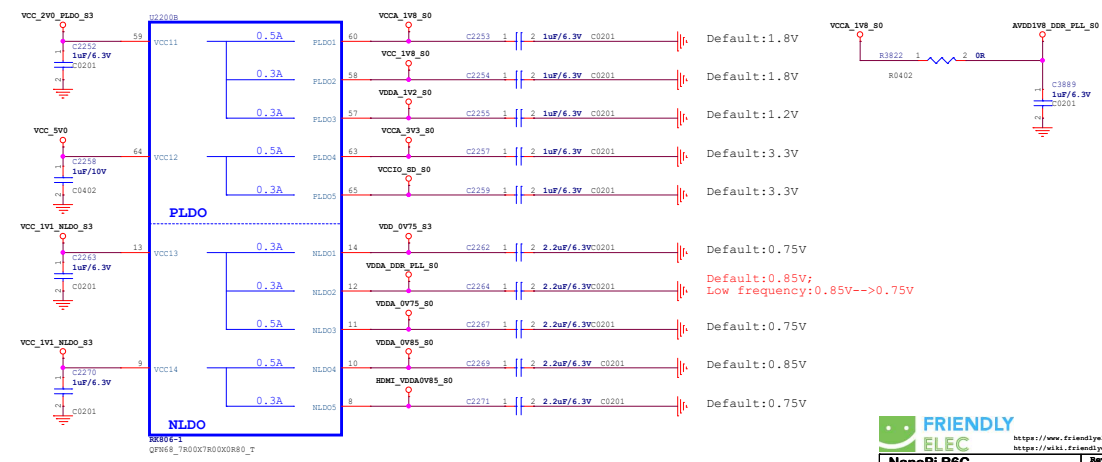
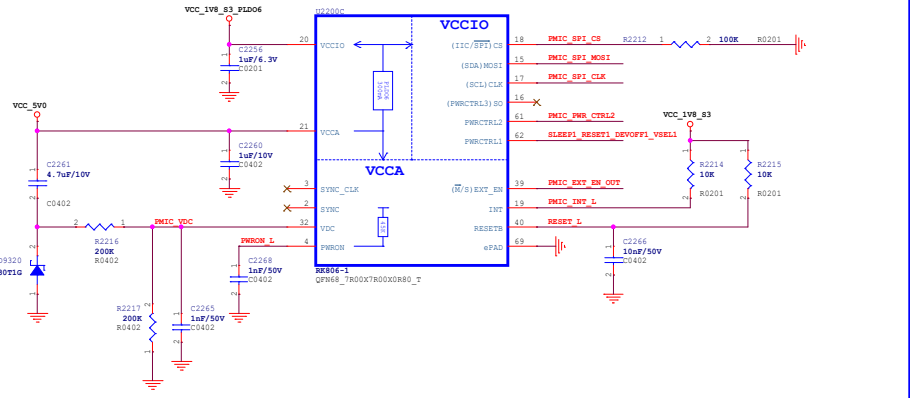
**IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!**

This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications  
Operating Supply Voltage: +5.5V(5.25-6V)  
Peak Pulse Current: >1A (tpe/20us)  
Surge Clamping Voltage: <6.5V

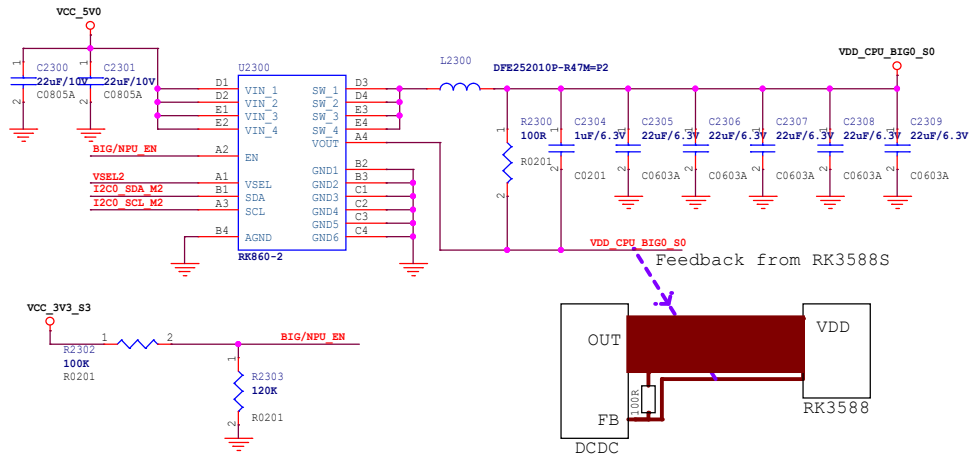
**DO NOT DELETE IT!**

# PMIC RK806-1 Management

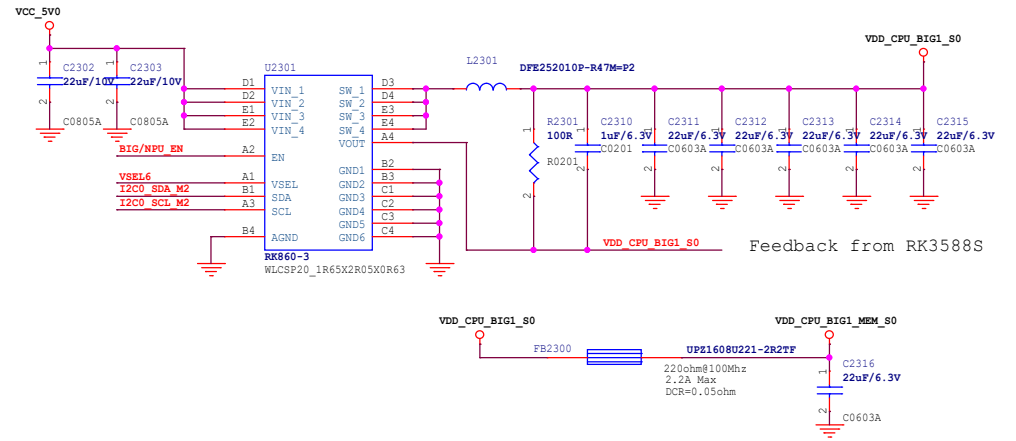
# PMIC RK806-1 LDO



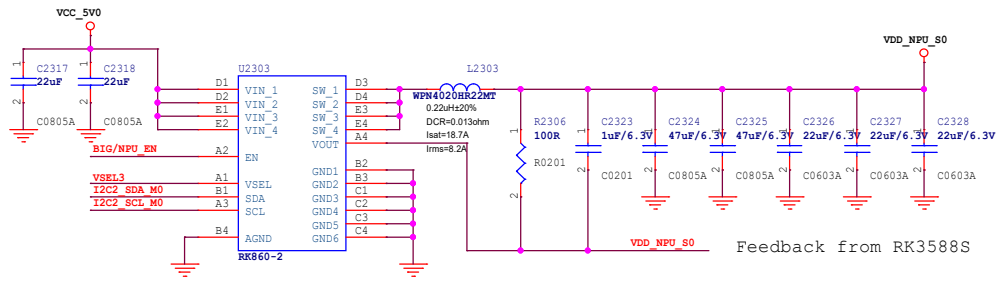
## VDD\_CPU\_BIG0



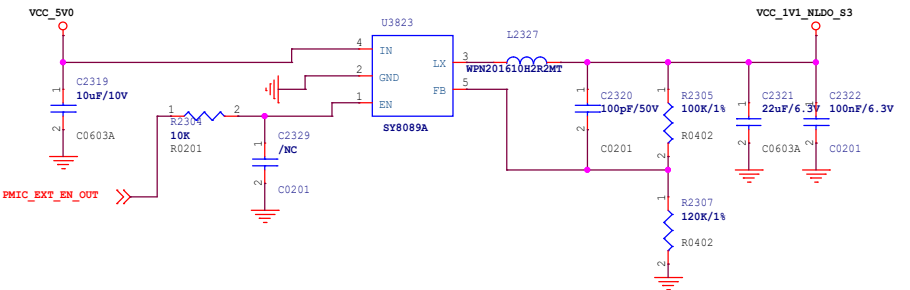
## VDD\_CPU\_BIG1



## VDD\_NPU

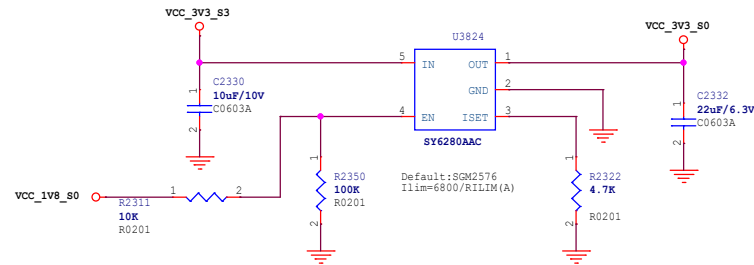


## VCC\_1V1\_NLDO\_S3



I2C0\_SCL\_M2 (7)  
 I2C0\_SDA\_M2 (7)  
 I2C2\_SCL\_M0 (7)  
 I2C2\_SDA\_M0 (7)

VSEL2 (7)  
 VSEL3 (7)  
 VSEL6 (7)



USB PD

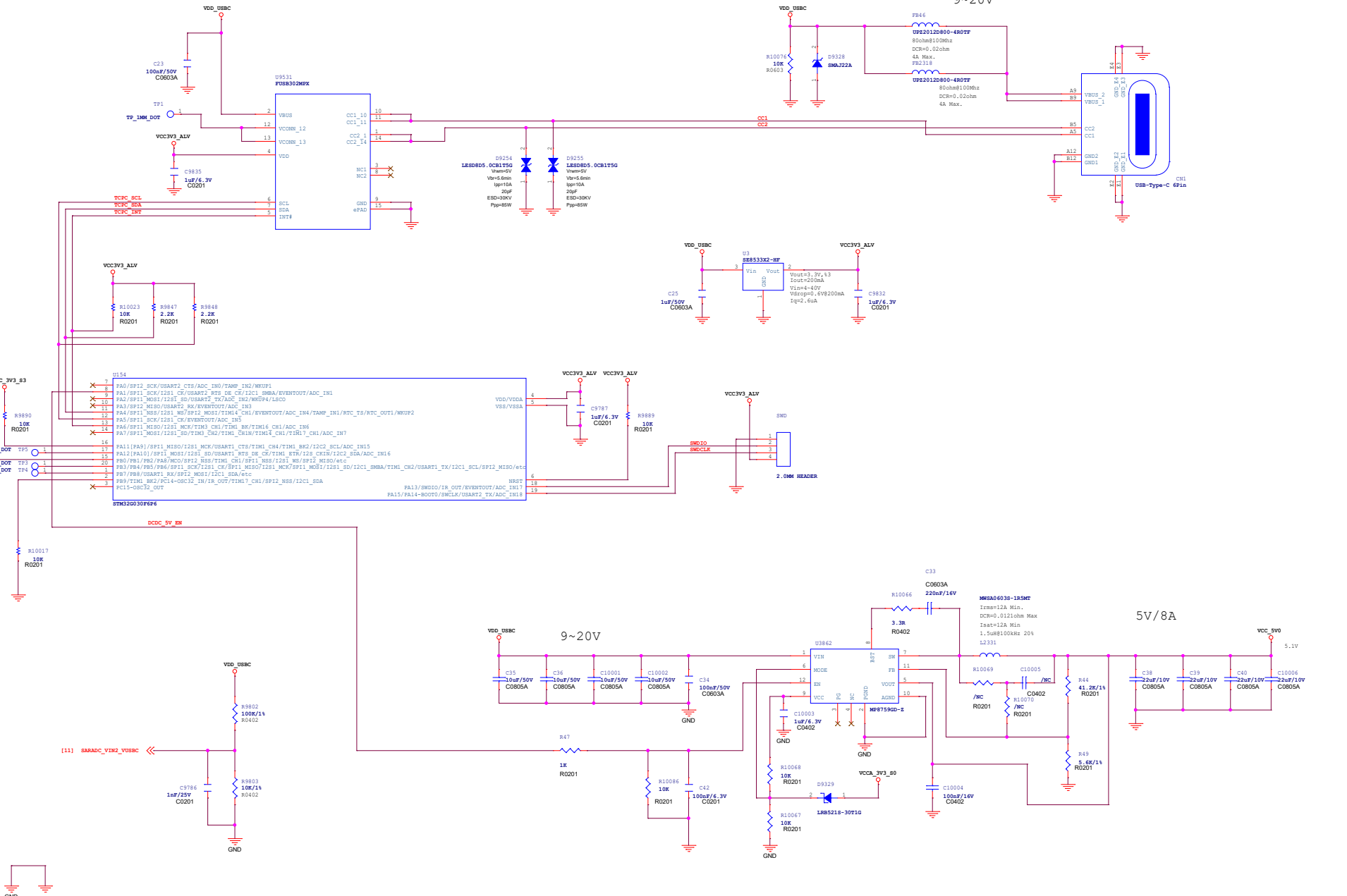
5

4

3

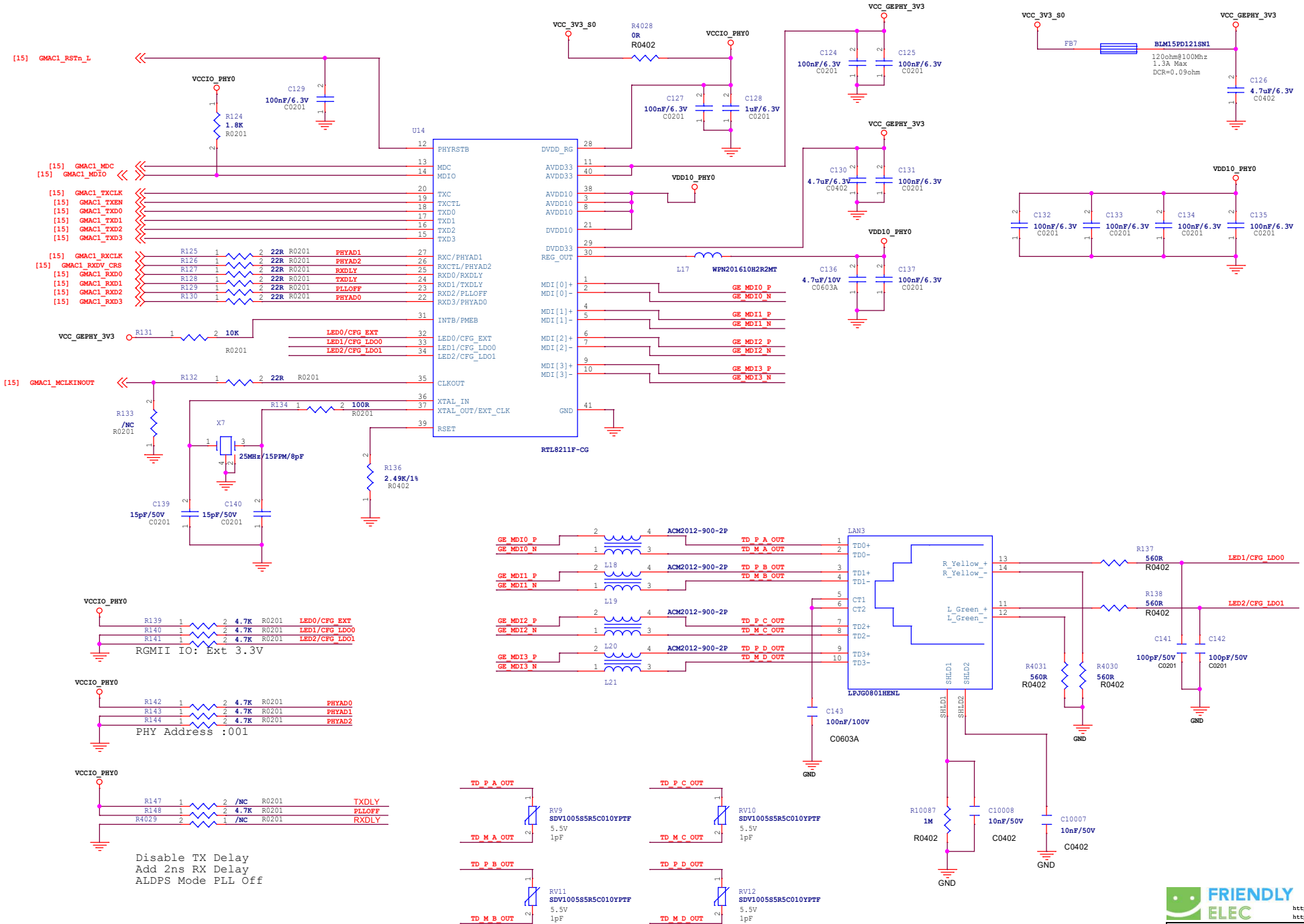
2

1

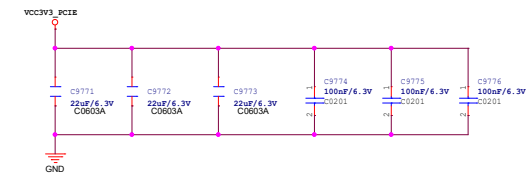
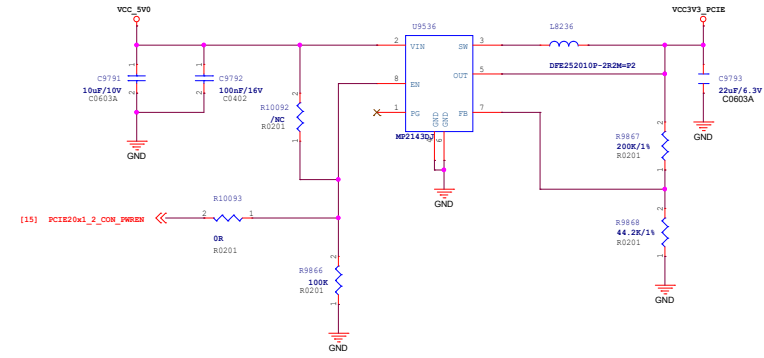
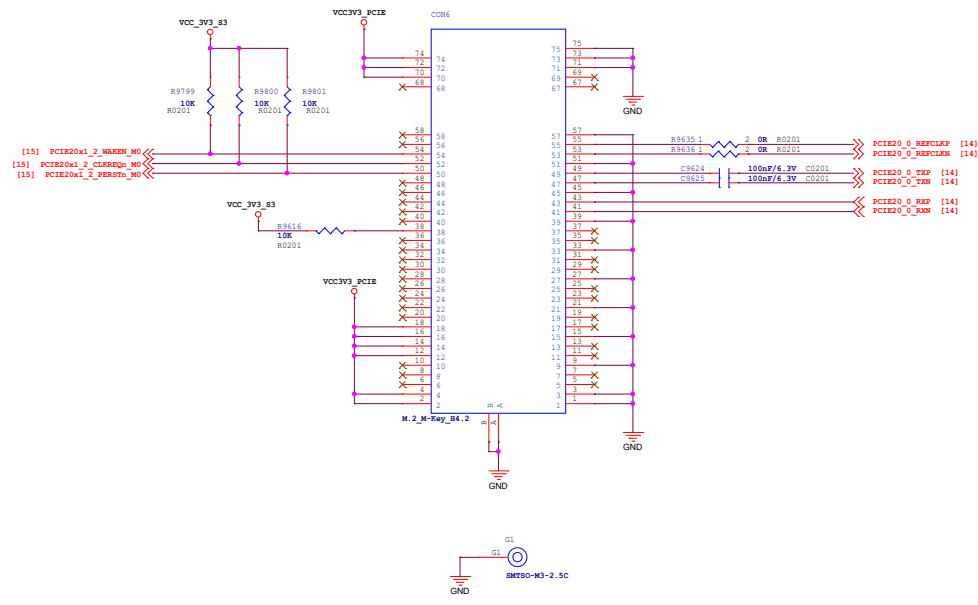




# 1G Ethernet

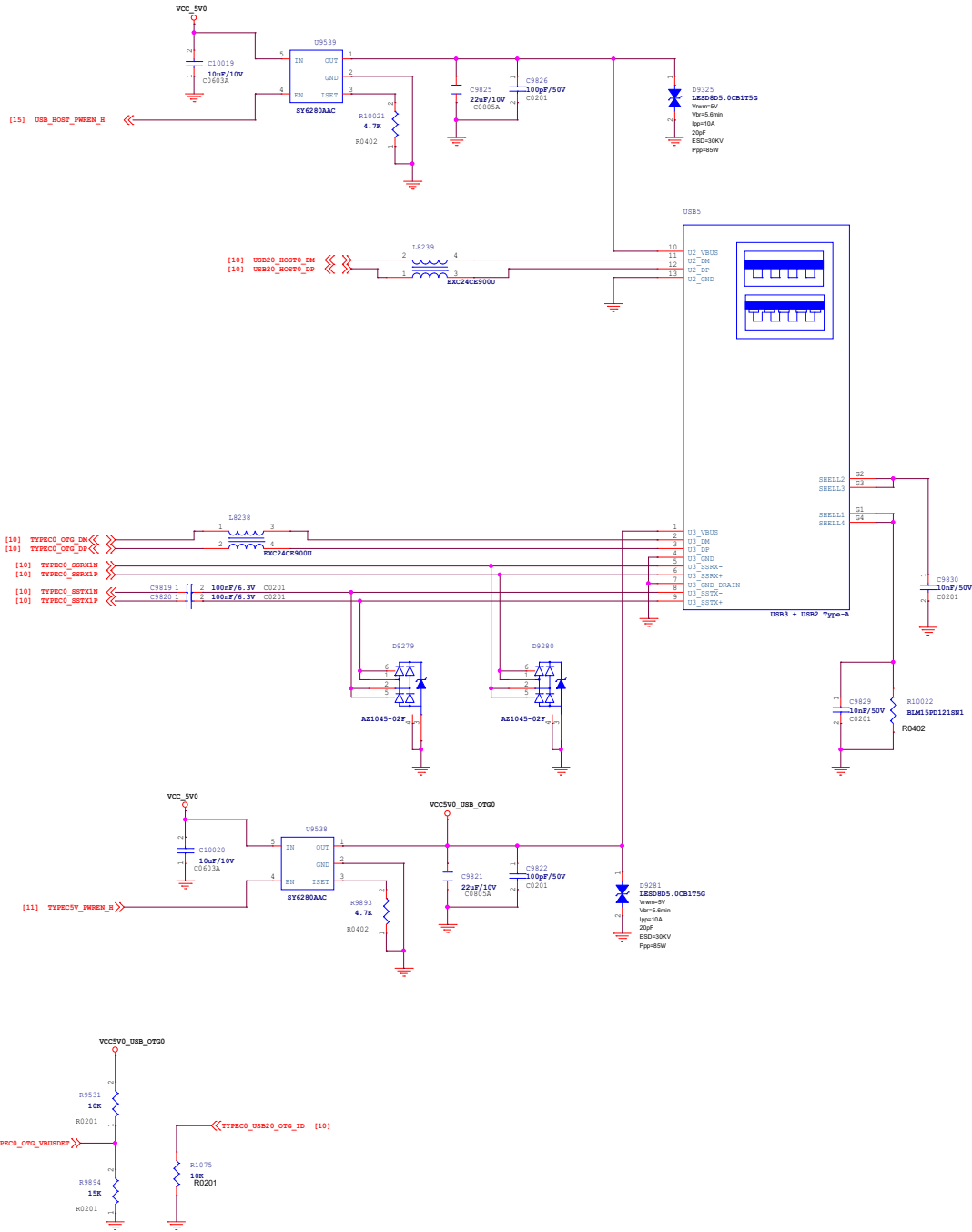


M.2 SSD 2280

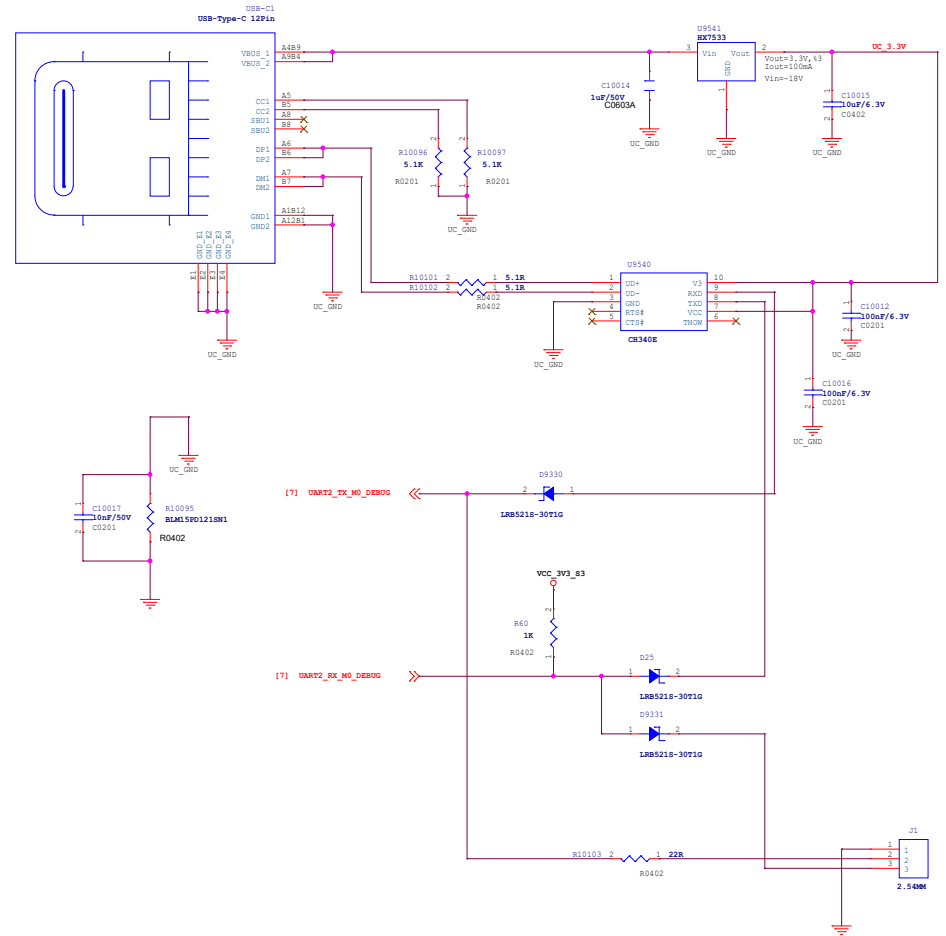


# USB 3.0/ADB/MASK

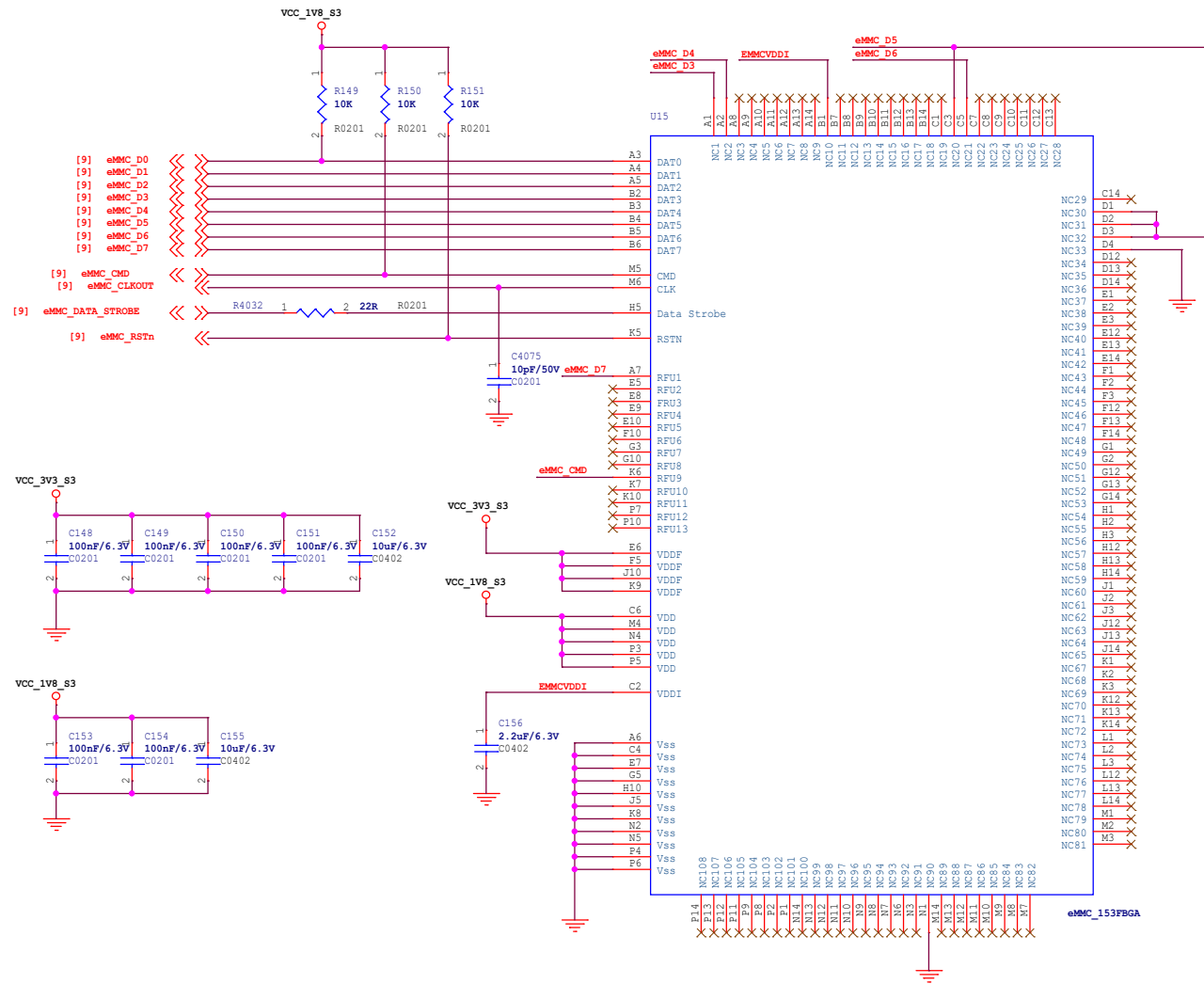
## USB 2.0



# Debug

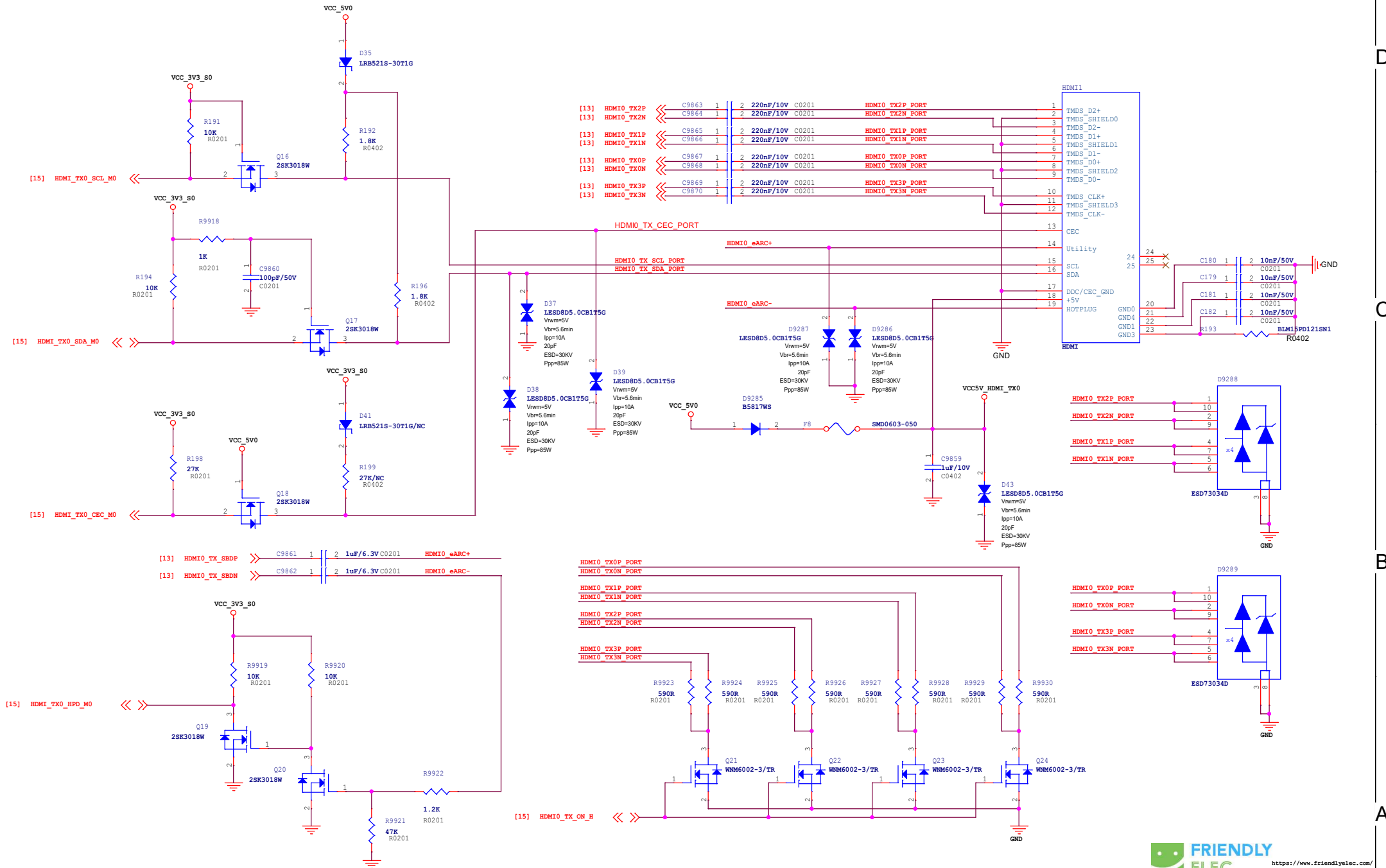


# eMMC

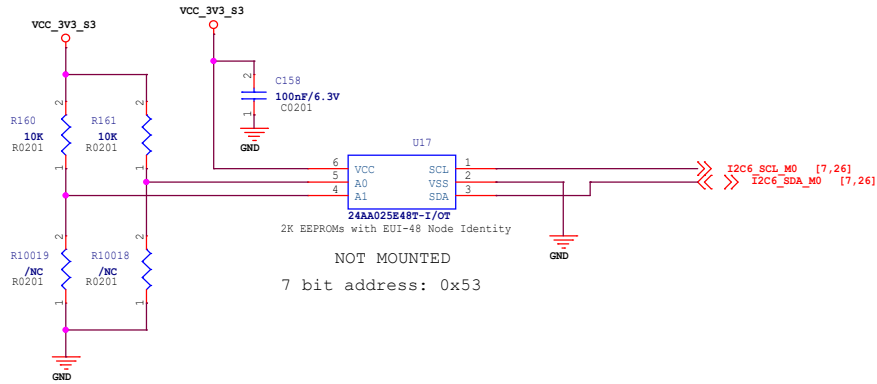




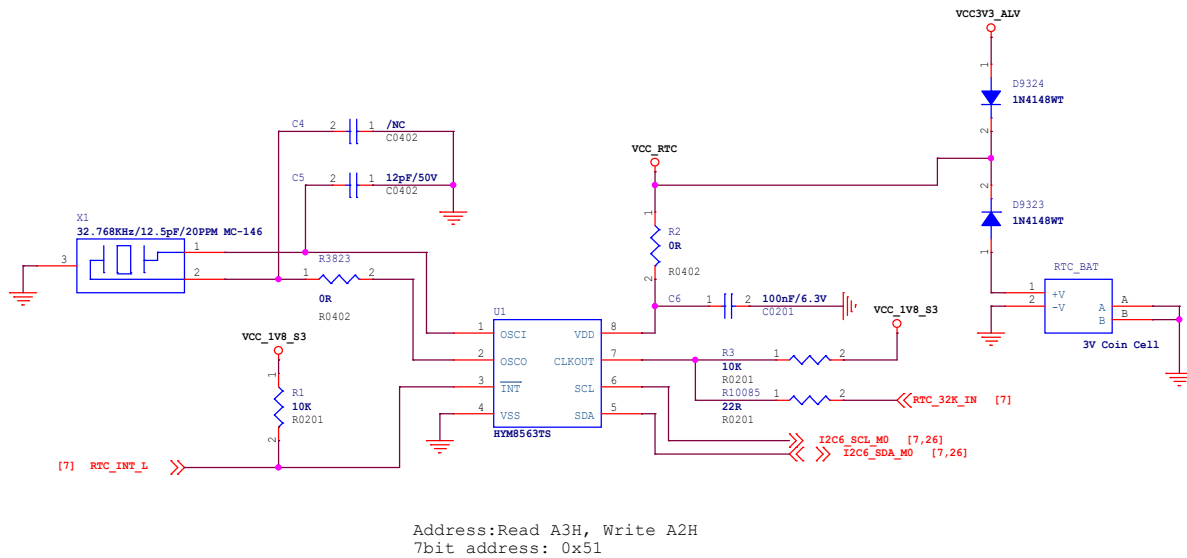
# HDMI TX0



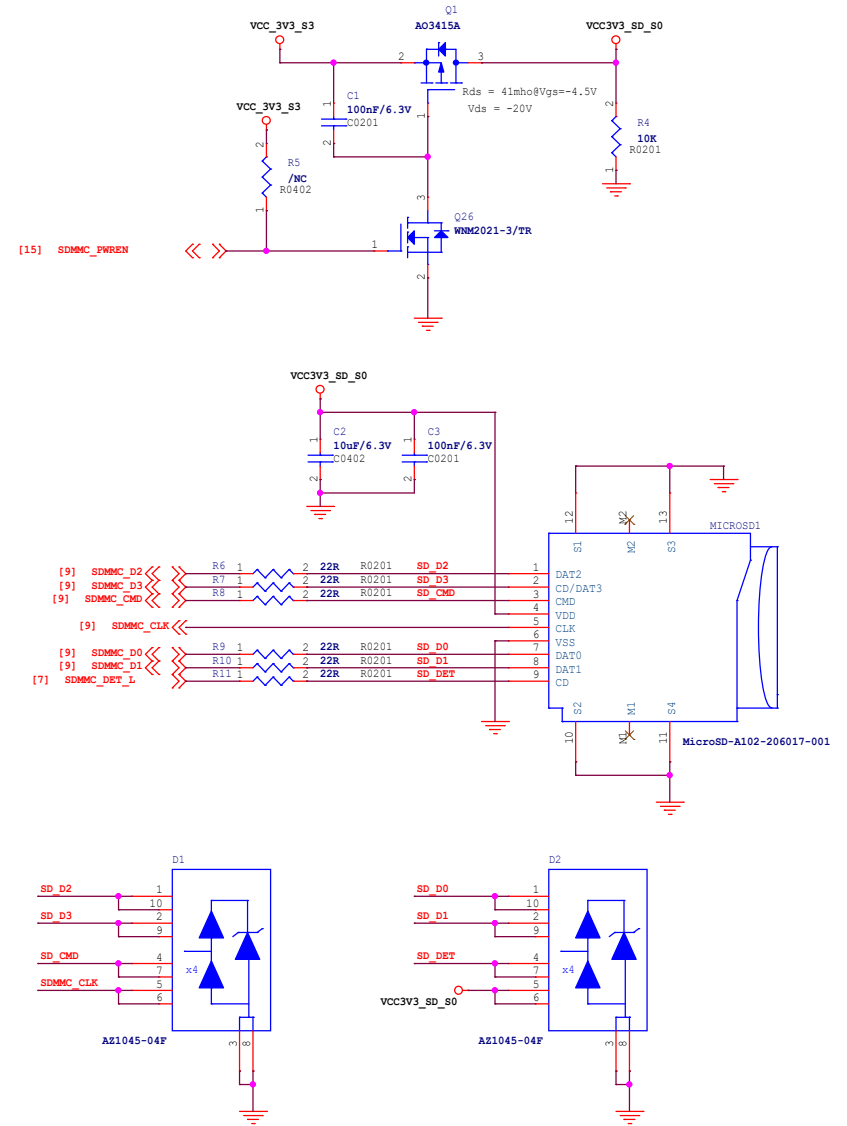
# EUI-48 Node Identity



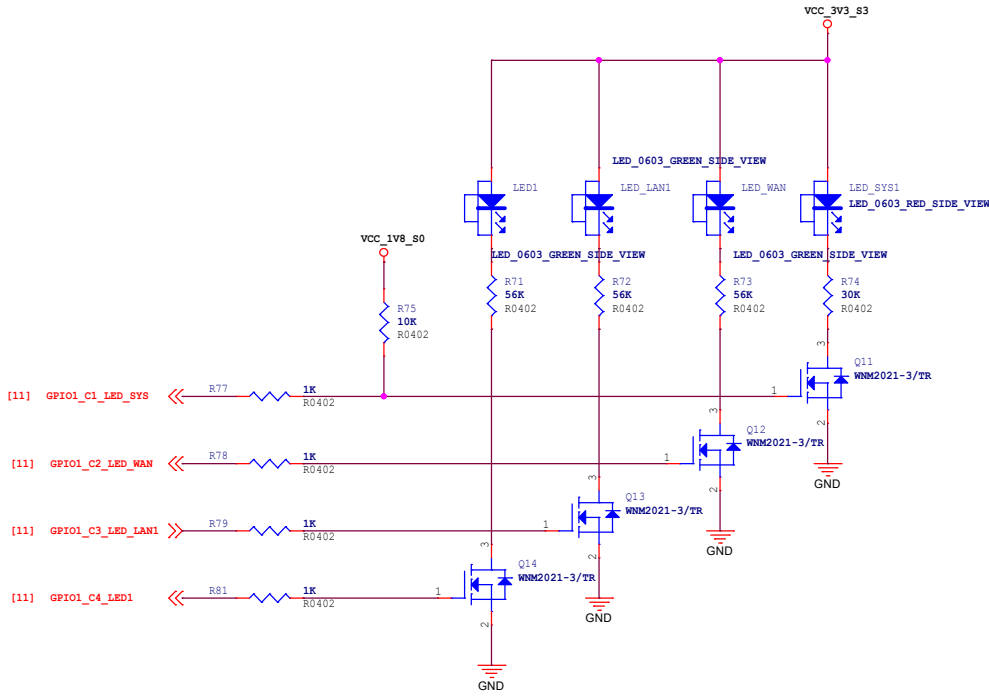
# RTC



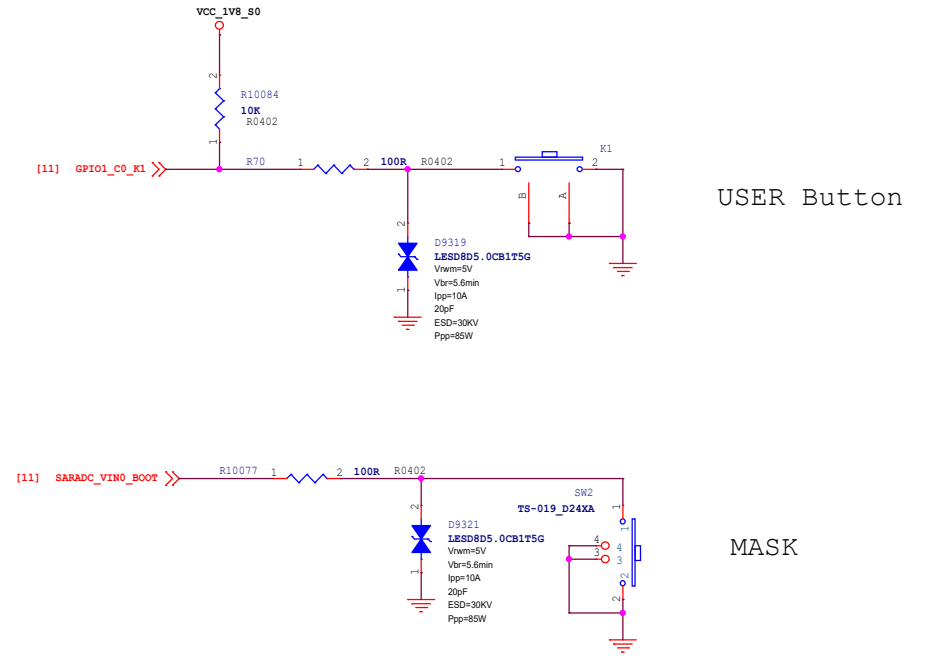
# microSD



# LED



# Button



# GPIO

