NanoPi R6S

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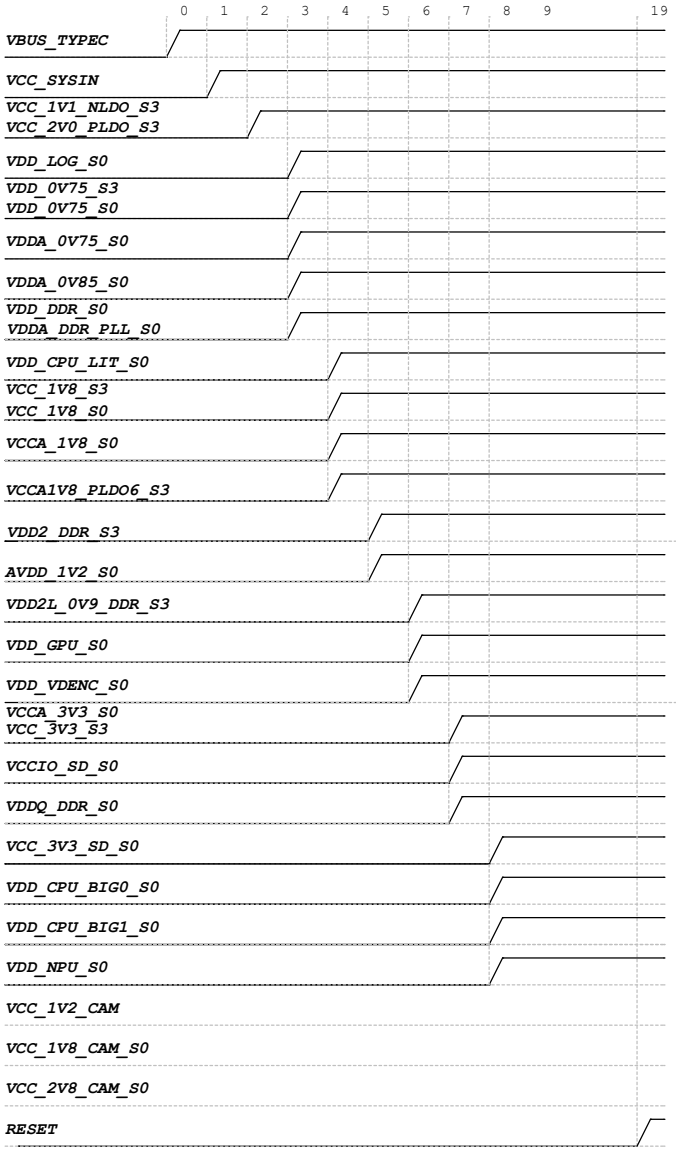
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

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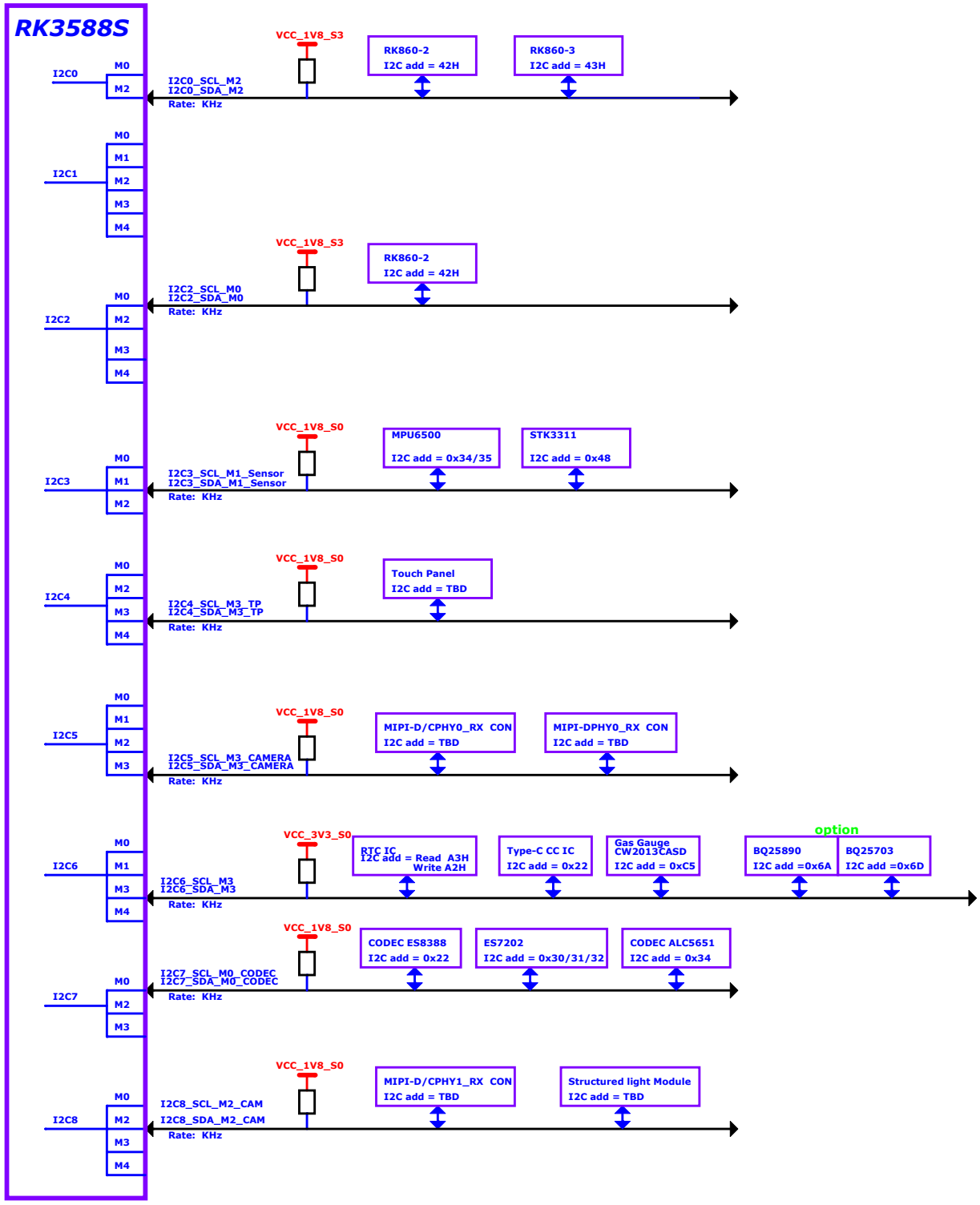
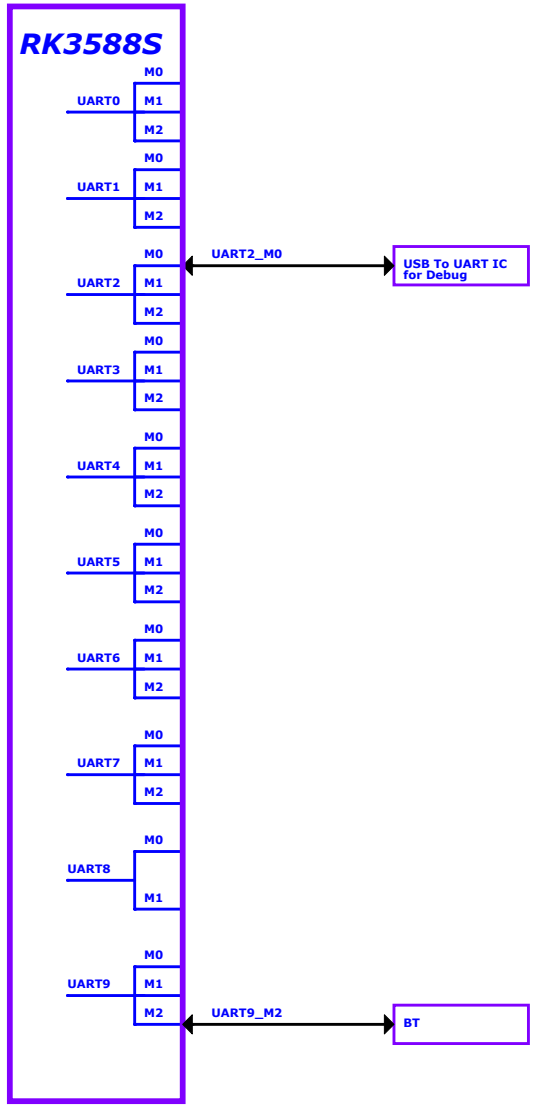
I2C MAP



UART MAP



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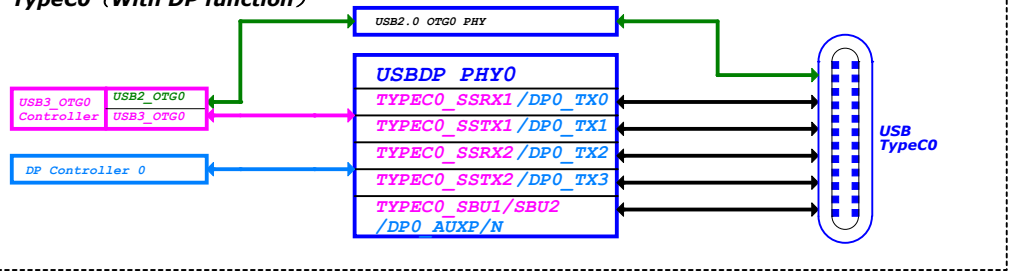
USB Controller Configure Table

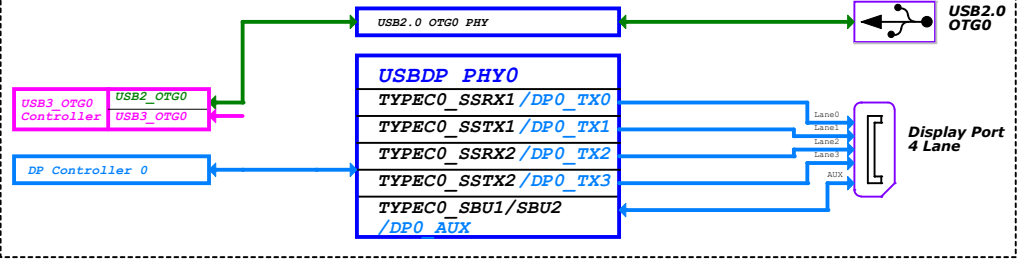
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1M/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2M/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2M	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2M/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

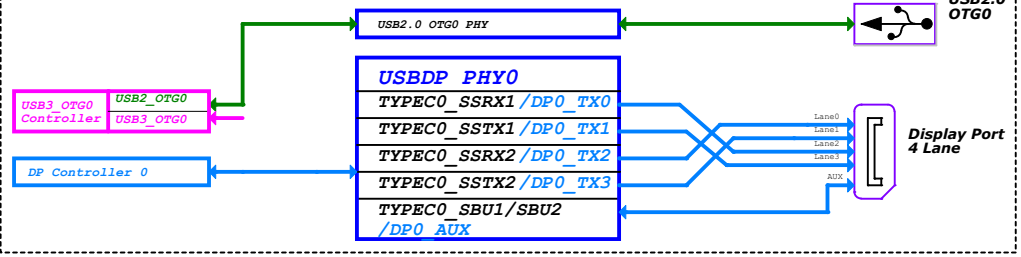
Config0:
TypeC0（With DP function）



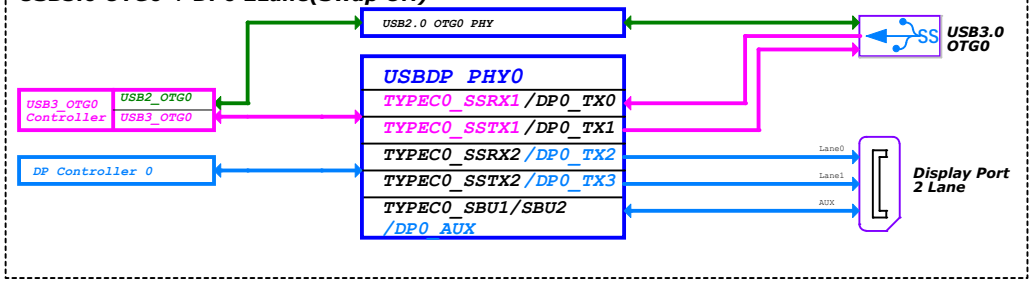
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



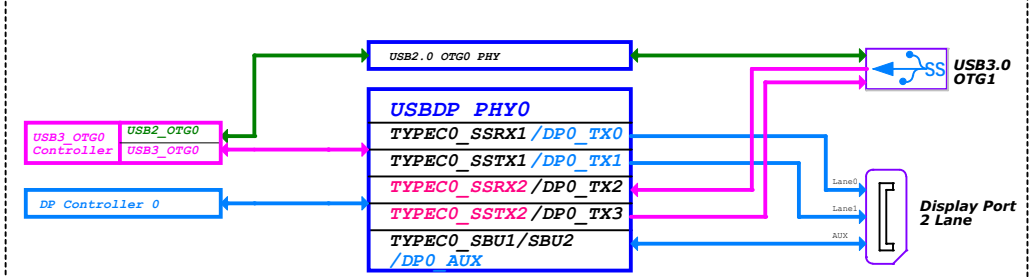
Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



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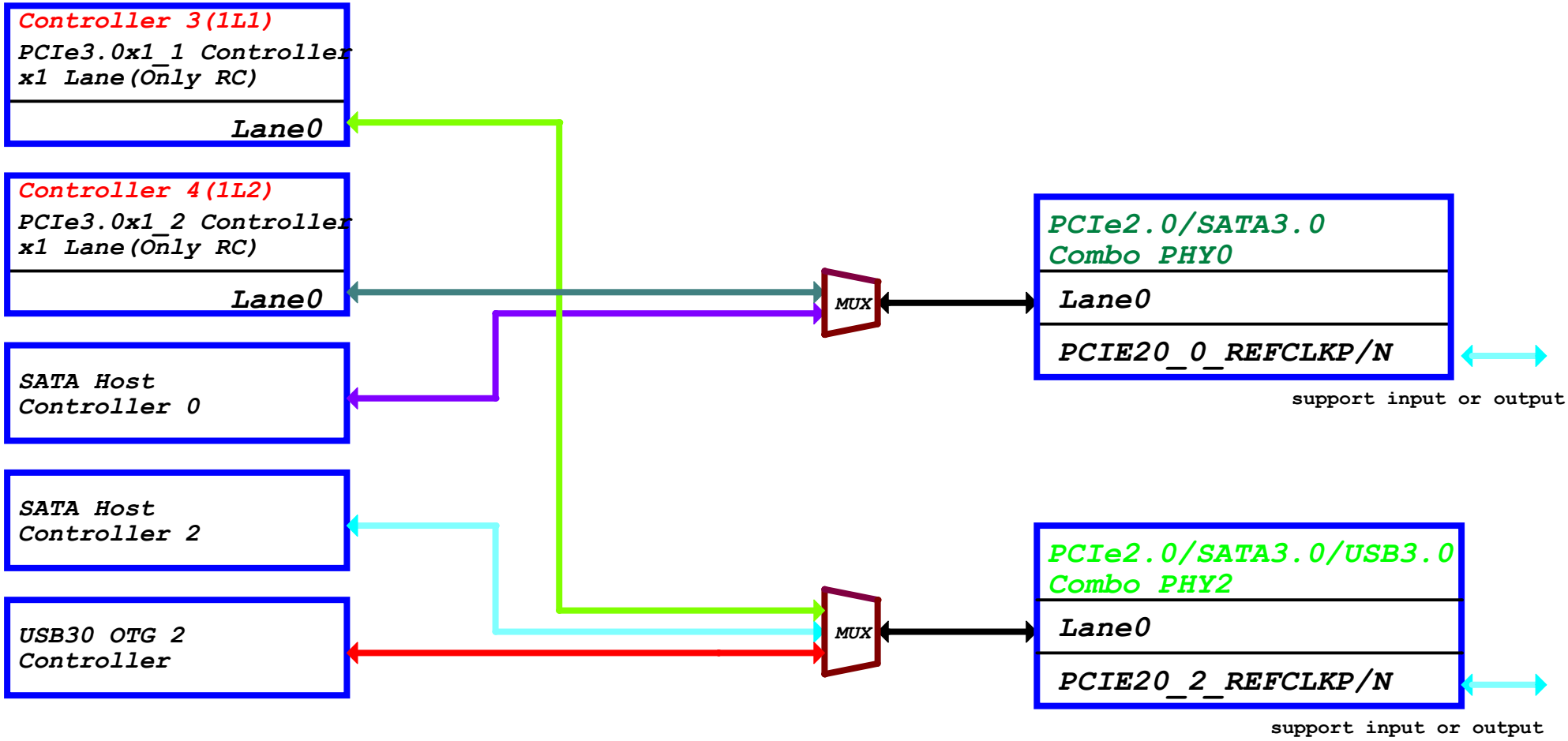
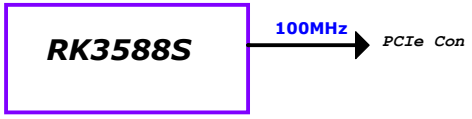
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

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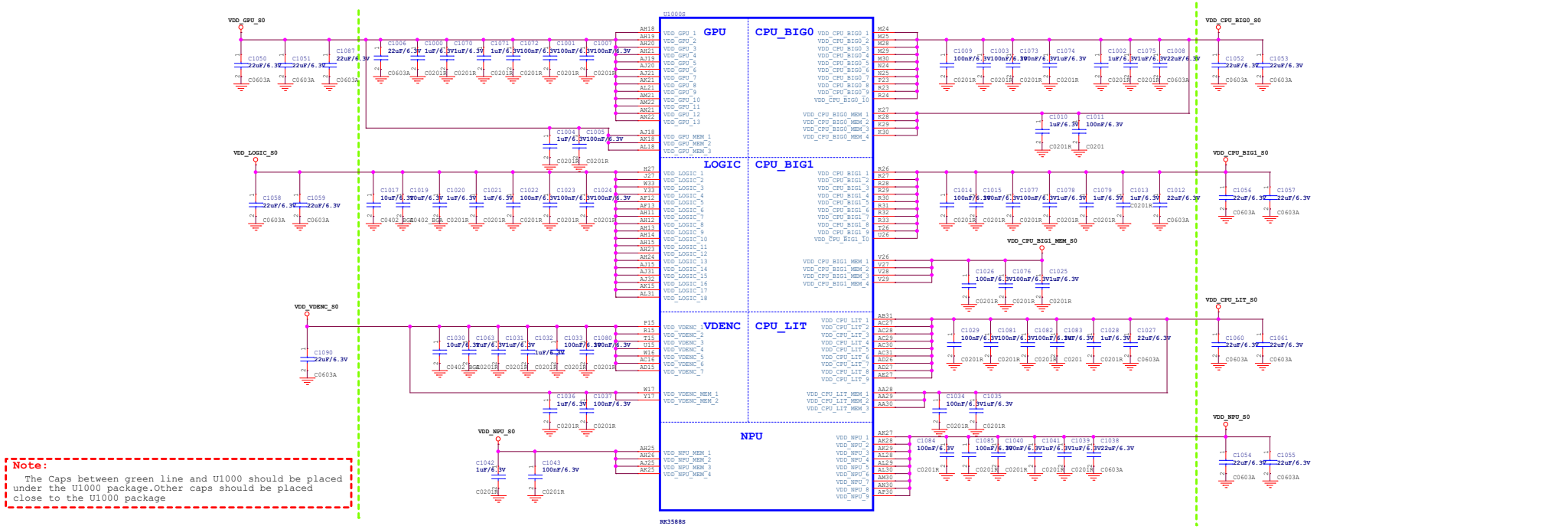
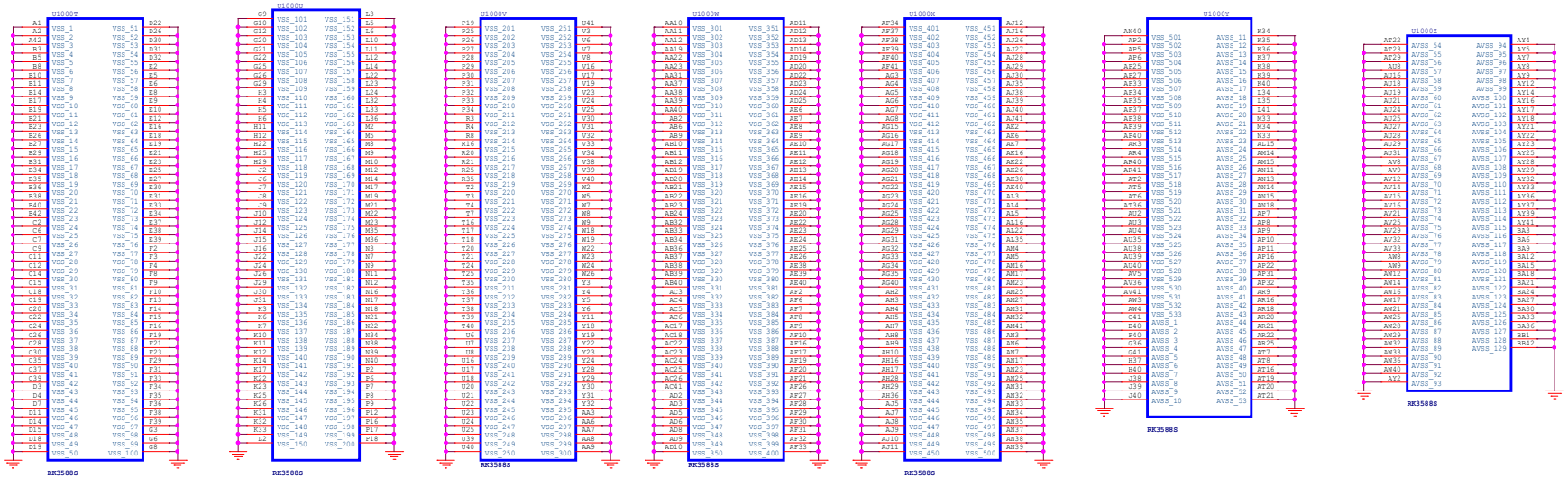
RK3588S(Power&Gnd)





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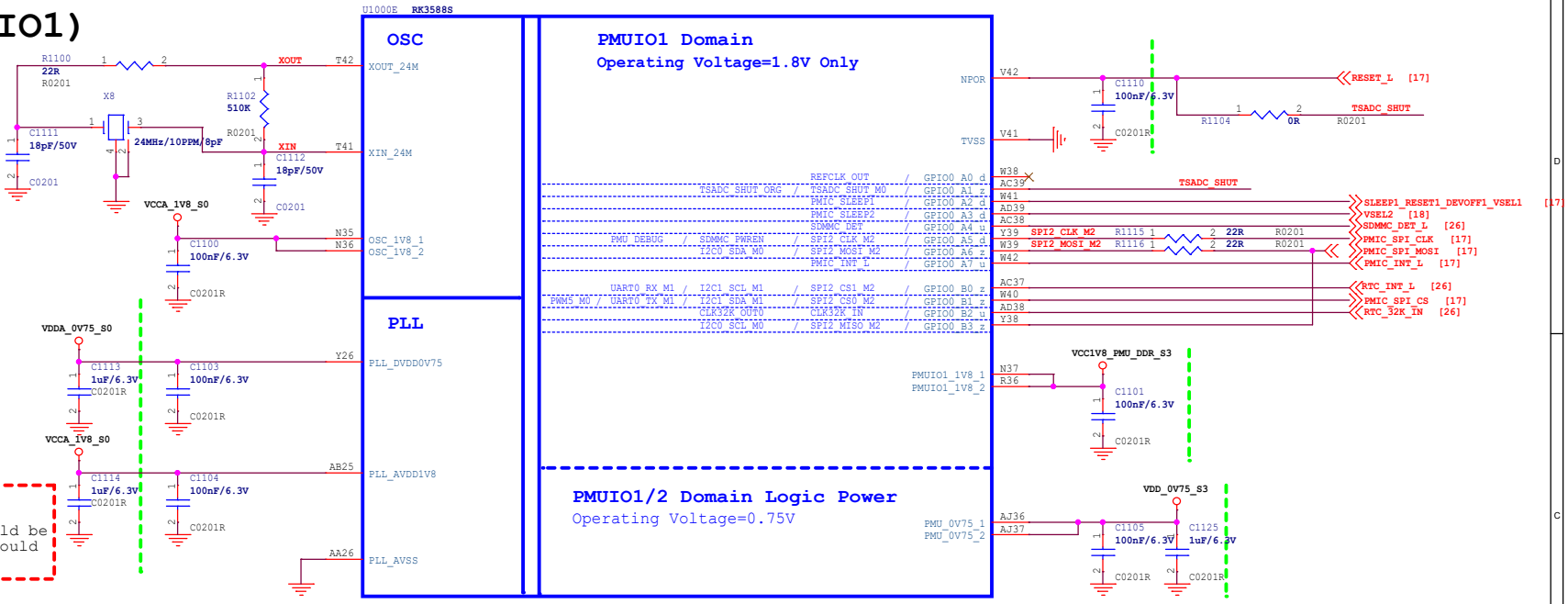
RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

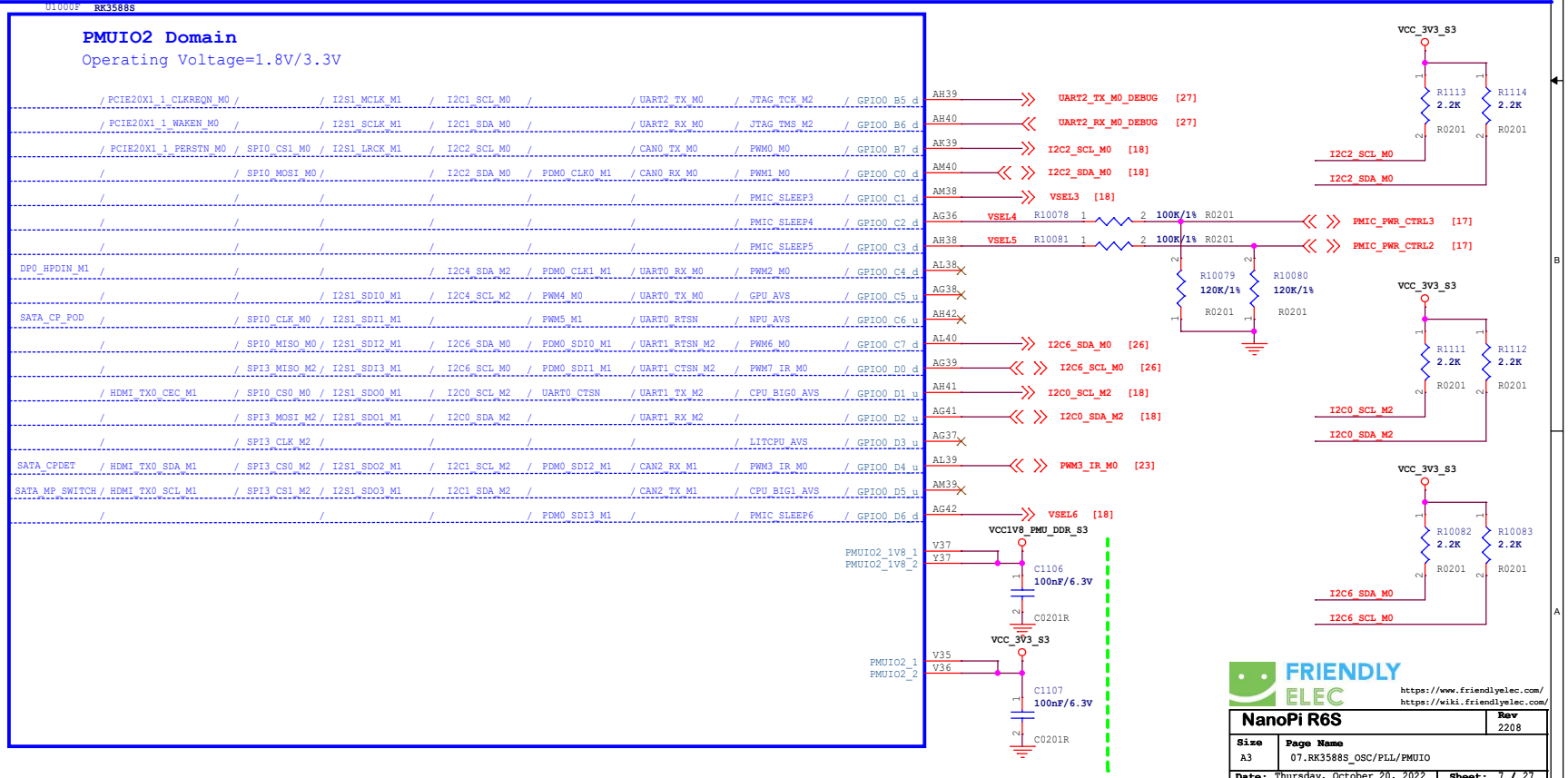
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588S(PMUIO2)



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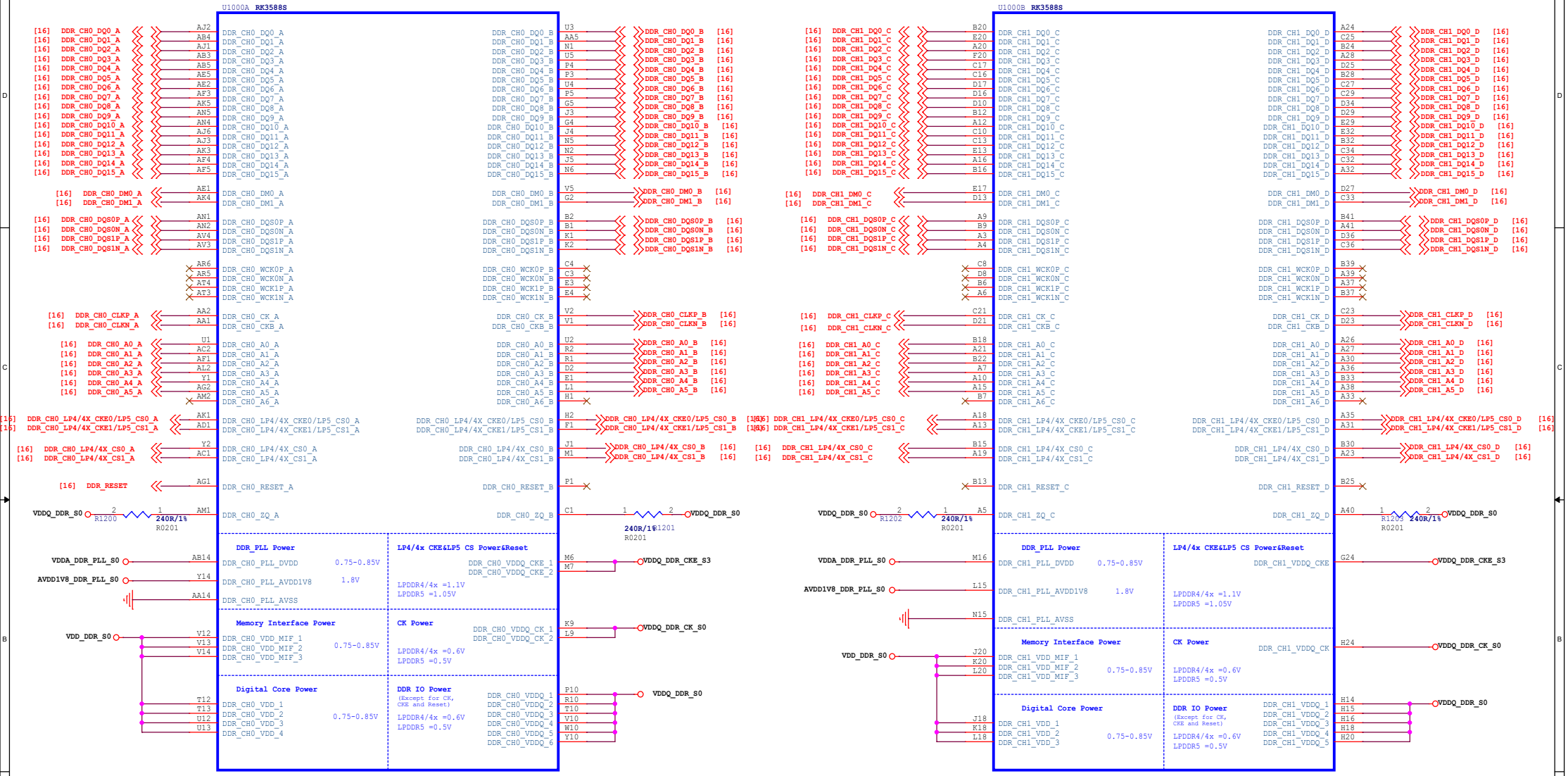
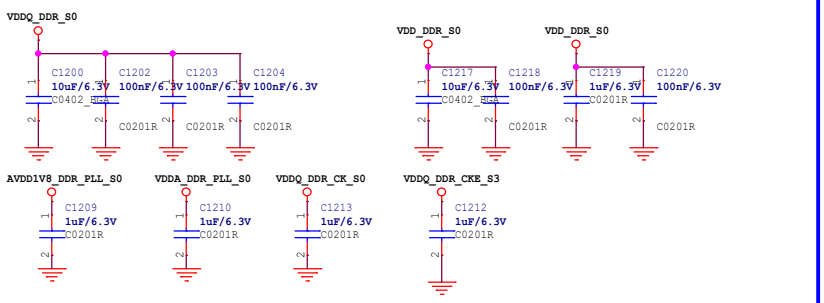
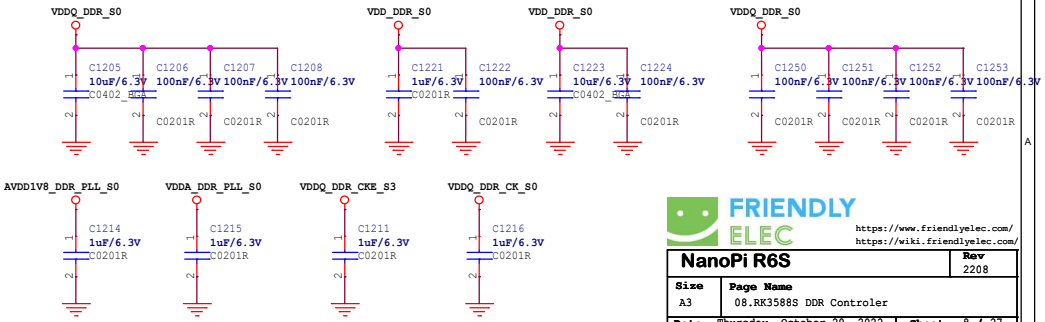
RK3588S(DDR PHY)



DDR FILTER





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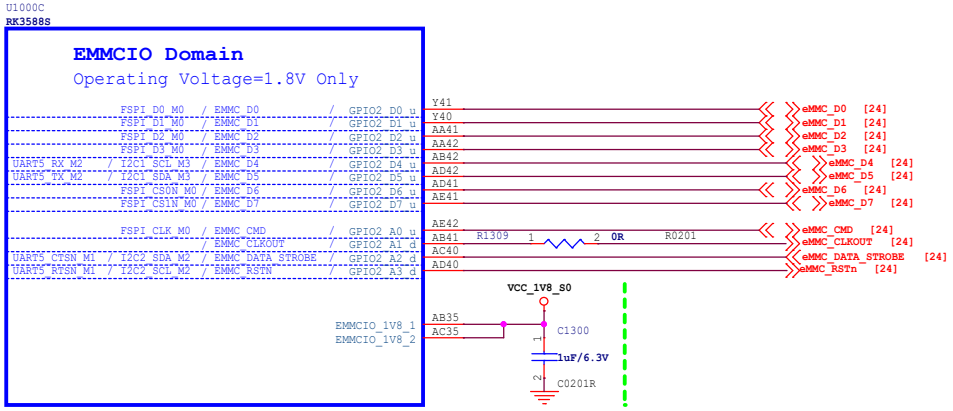
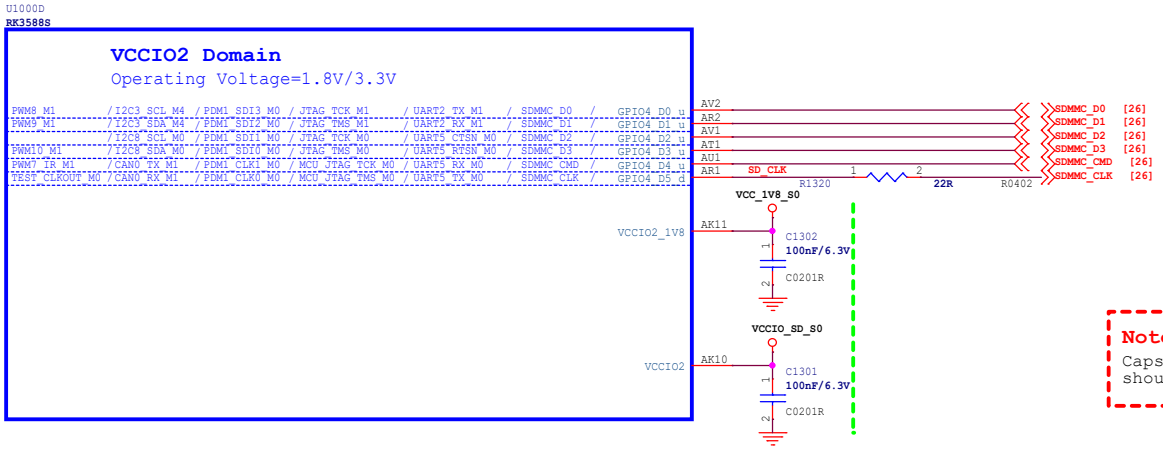
RK3588S(EMMCIO Domain)



RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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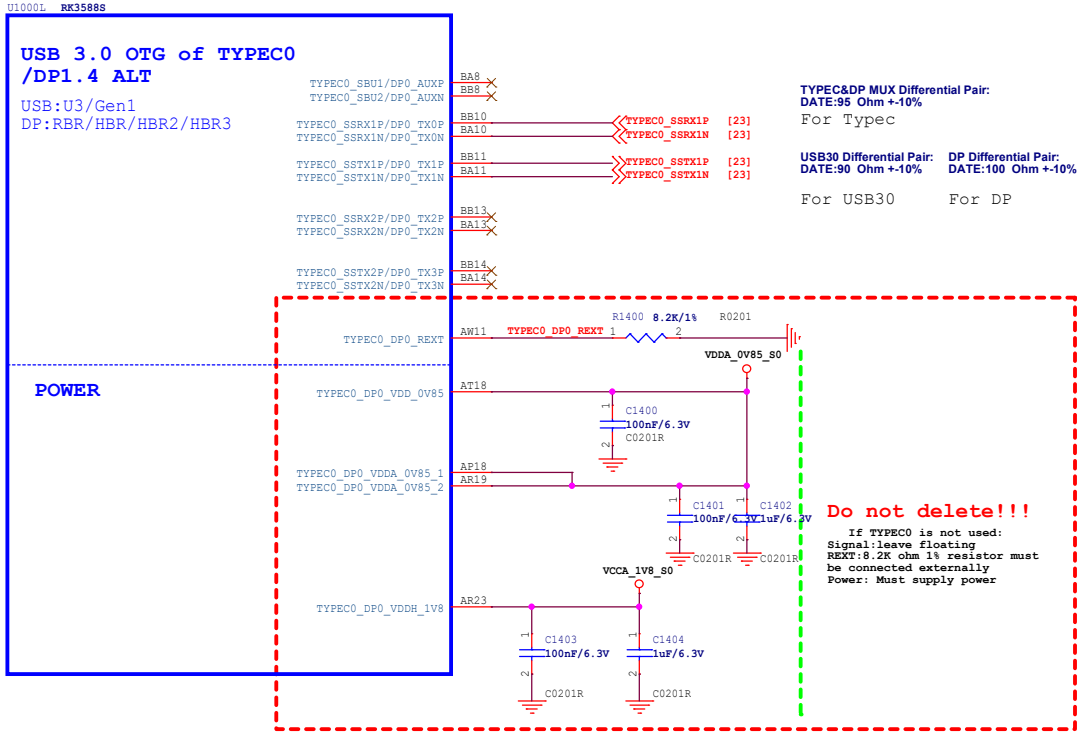
RK3588S(USB3.0/DP1.4)

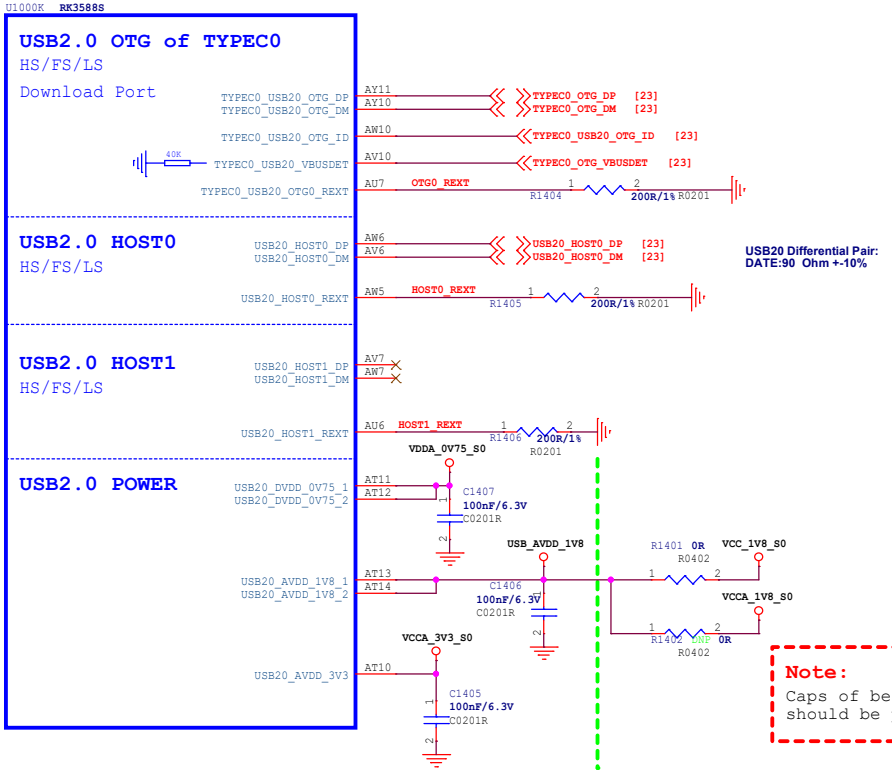


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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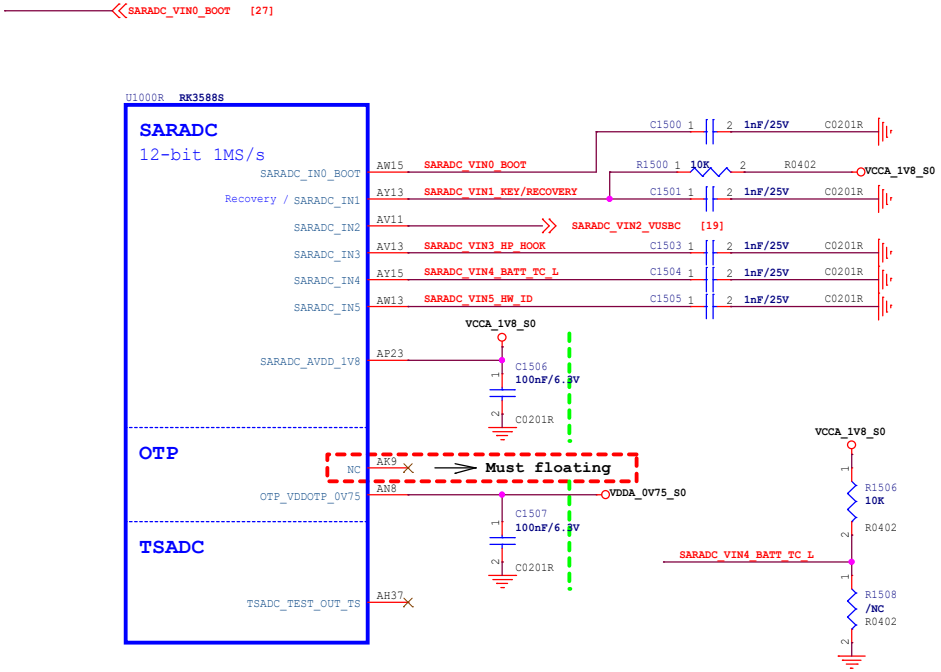
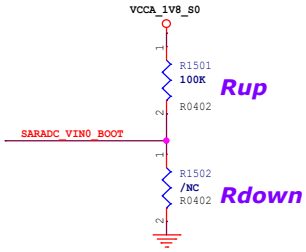
RK3588S(SARADC/OTP/TSADC)

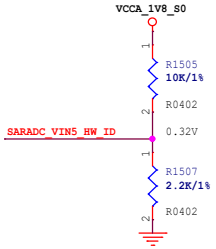


BOOT MODE CONFIG



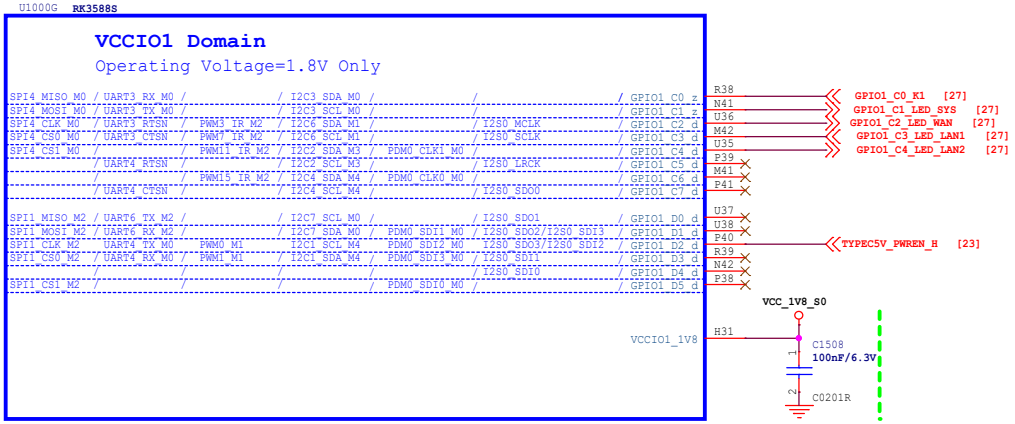
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



	0.325V (8GB)	0.429V (4GB)
R1505	10K/1%	15K/1%
R1507	2.2K/1%	4.7K/1%

RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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NanoPi R6S	Rev 2208
Size A3	Page Name 11.RK3588S_SARADC/1.8V GPIO
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RK3588S(MIPI_DPHY CSI0 RX)

U1000N RK3588S

MIPI DPHY CSI_RX Port0

MIPI V1.2
2.5Gbps

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI0_CLK0P	AN42
MIPI_CSI0_CLK0N	AN41
MIPI_CSI0_D0P	AL42
MIPI_CSI0_D0N	AL41
MIPI_CSI0_D1P	AK41
MIPI_CSI0_D1N	AK42
MIPI_CSI0_CLK1P	AU41
MIPI_CSI0_CLK1N	AU42
MIPI_CSI0_D2P	AT41
MIPI_CSI0_D2N	AT42
MIPI_CSI0_D3P	AP42
MIPI_CSI0_D3N	AP41
MIPI_CSI0_AVCC0V75	AM37
MIPI_CSI0_AVCC1V8	AM35

Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)

U1000Q RK3588S

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	BB34
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	BA34
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	BB31
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	BA31
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	BA32
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	BB32
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	BA35
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	BB35
MIPI_DPHY0_TX_D3P/NO_USE	BB37
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	BA37

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	BB41
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	BA41
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	BA38
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	BB38
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	BA40
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AY40
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AY42
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	BA42
MIPI_DPHY0_RX_D3P/NO_USE	AW41
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AW42

Power

MIPI_D/C_PHY0_VREG	AT33
MIPI_D/C_PHY0_VDD	AR33
MIPI_D/C_PHY_VDD_1V2_1	AR34
MIPI_D/C_PHY_VDD_1V8_1	AR30

TX and RX port must work in the same mode, DPHY or CPHY

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)

U1000P RK3588S

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	BB18
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	BA18
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	BB16
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	BA16
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	BA17
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	BB17
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	BA20
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	BB20
MIPI_DPHY1_TX_D3P/NO_USE	BB22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	BA22

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	BA26
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	BB26
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	BA23
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	BB23
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	BB25
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	BA25
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	BB28
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	BA28
MIPI_DPHY1_RX_D3P/NO_USE	BA29
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	BB29

Power

MIPI_D/C_PHY1_VREG	AT27
MIPI_D/C_PHY1_VDD	AR27
MIPI_D/C_PHY_VDD_1V2_2	AR35
MIPI_D/C_PHY_VDD_1V8_2	AT30

TX and RX port must work in the same mode DPHY or CPHY

Note:
If not used:
Signal:leave floating
Power: Floating

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NanoPi R6S	Rev 2208
Size A2	Page Name 12.RK3588S_MIPI Interface
Date: Thursday, October 20, 2022	Sheet: 12/ 27

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

HDMI TX
100 Ohm ±10%

U1000Q

HDMI TX/eDP1.3 MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P	BB4	HDMI0_TX0P [25]
HDMI_TX0_D0N/EDP_TX0_D0N	BA4	HDMI0_TX0N [25]
HDMI_TX0_D1P/EDP_TX0_D1P	BA5	HDMI0_TX1P [25]
HDMI_TX0_D1N/EDP_TX0_D1N	BB5	HDMI0_TX1N [25]
HDMI_TX0_D2P/EDP_TX0_D2P	BB7	HDMI0_TX2P [25]
HDMI_TX0_D2N/EDP_TX0_D2N	BA7	HDMI0_TX2N [25]
HDMI_TX0_D3P/EDP_TX0_D3P	BA2	HDMI0_TX3P [25]
HDMI_TX0_D3N/EDP_TX0_D3N	BB2	HDMI0_TX3N [25]
HDMI_TX0_SBDP/EDP_TX0_AUXP	BA1	HDMI0_TX_SBDP [25]
HDMI_TX0_SBDN/EDP_TX0_AUXN	AY1	HDMI0_TX_SBDN [25]

HDMI/eDP_TX0_REXT — AY3 — HDMI/eDP_TX0_REXT — R1708 1 — 2 — 8.2K/1% R0201 — VDDA_0V75_S0

POWER

HDMI/EDP_TX0_VDD_0V75_1	AM13	C1710 100nF/6.3V C0201R	C1711 4.7uF/6.3V C0402_BGA	C1718 10uF/6.3V C0402_BGA
HDMI/EDP_TX0_VDD_0V75_2	AN12			
HDMI/EDP_TX0_AVDD_0V75	AN10	C1712 100nF/6.3V C0201R	C1725 1uF/6.3V C0201R	
HDMI/EDP_TX0_VDD_IO_1V8	AK12	C1713 100nF/6.3V C0201R	C1714 4.7uF/6.3V C0402_BGA	C1716 4.7uF/6.3V C0402_BGA
HDMI/EDP_TX0_VDD_CMN_1V8	AL14			

VCCA_1V8_S0

RK3588S

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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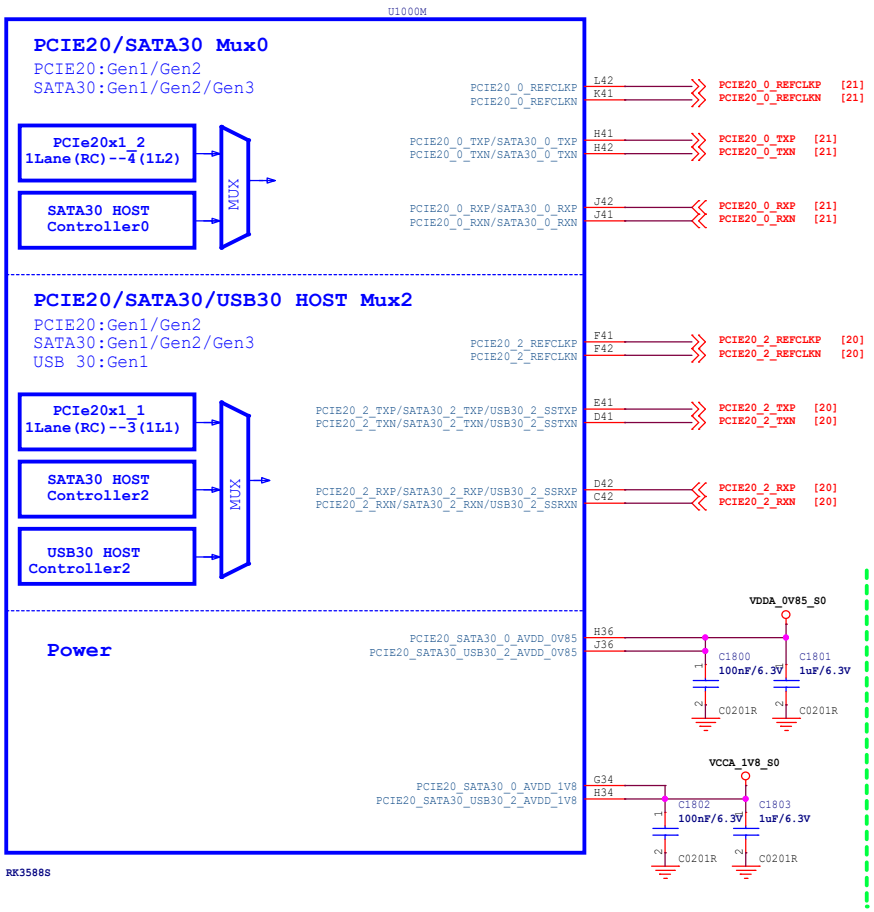
Size A4	Page Name 13.RK3588S_HDMI/eDP Interface	
Date: Thursday, October 20, 2022	Sheet: 13/ 27	

RK3588S(PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

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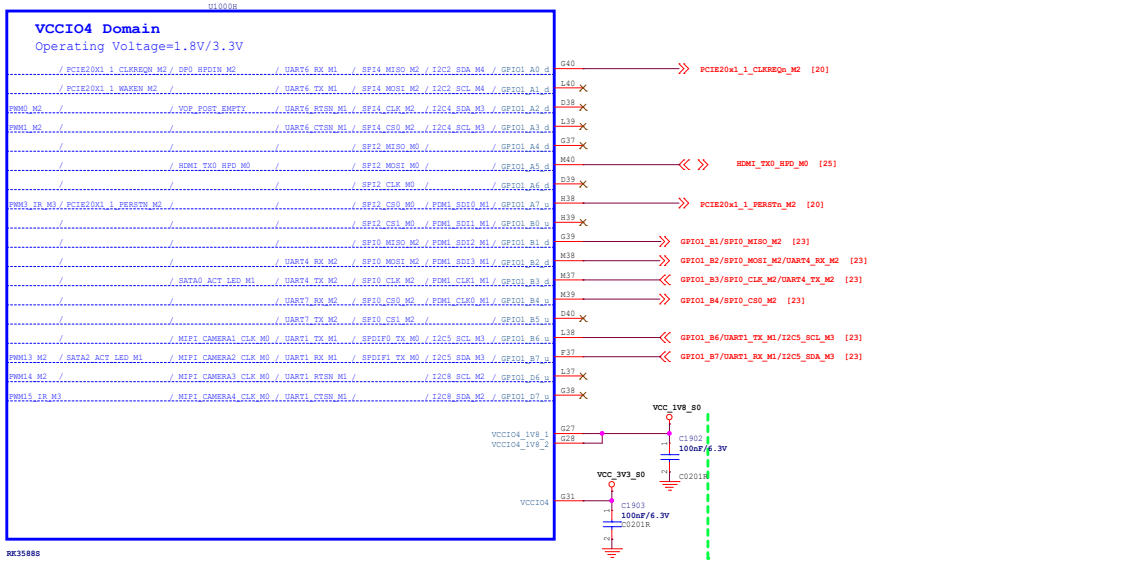
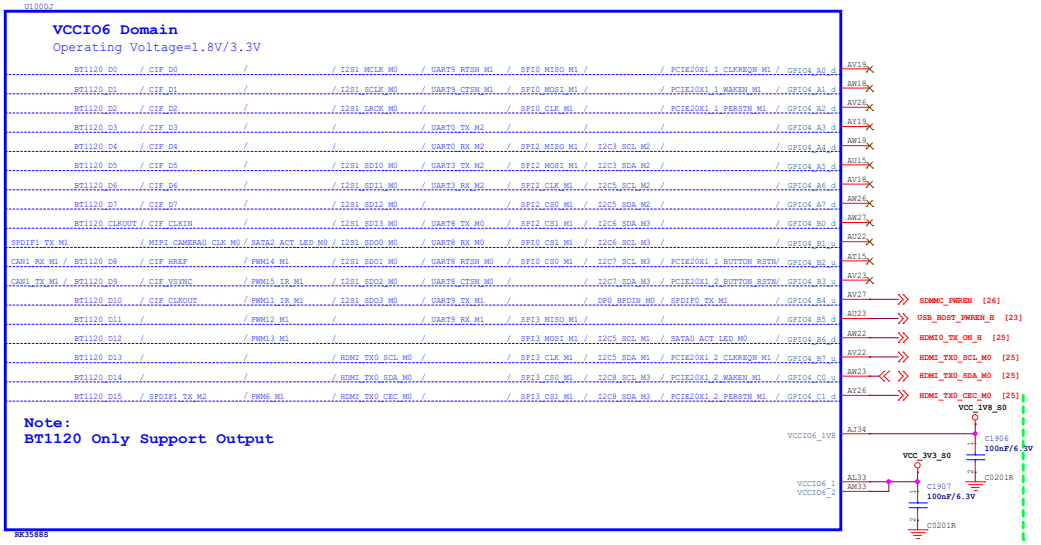
Size A3	Page Name 14.RK3588S PCIE2/SATA3/USB3 PHY
Date: Thursday, October 20, 2022	Sheet: 14/ 27

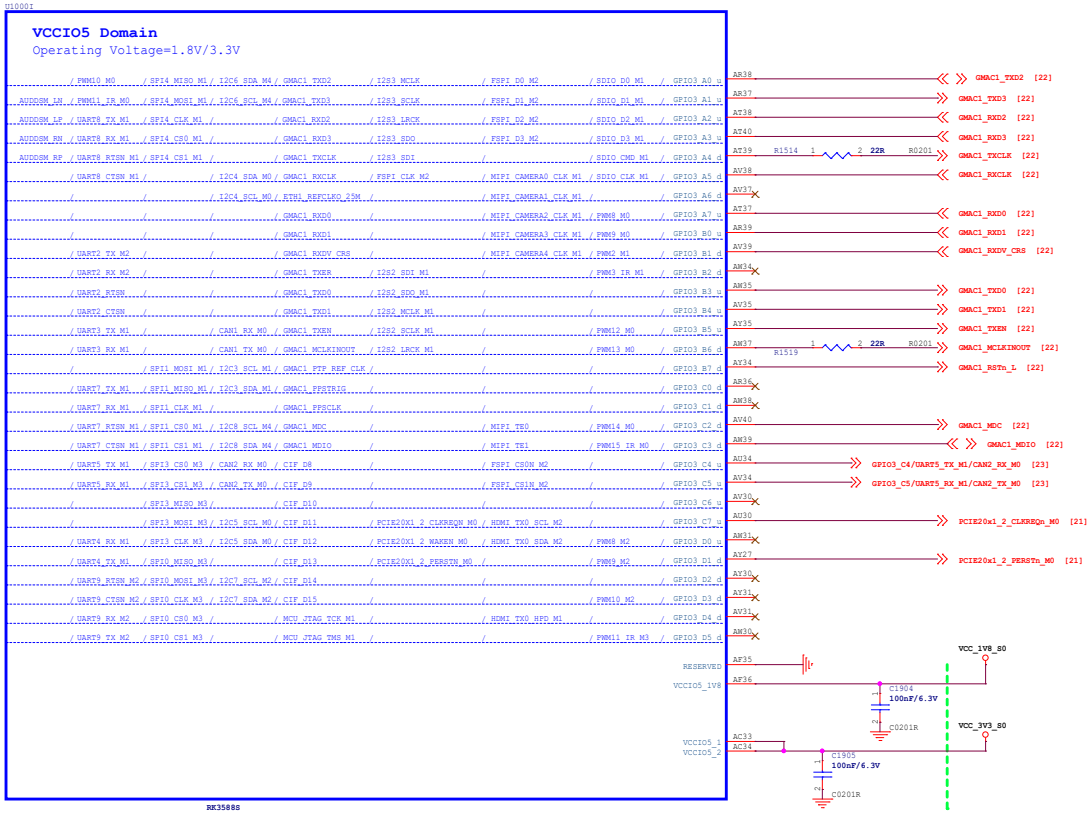
RK3588S(VCCIO4 Domain)



RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)



Note:
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Size A2	Page Name 15.RK3588S GPIO	
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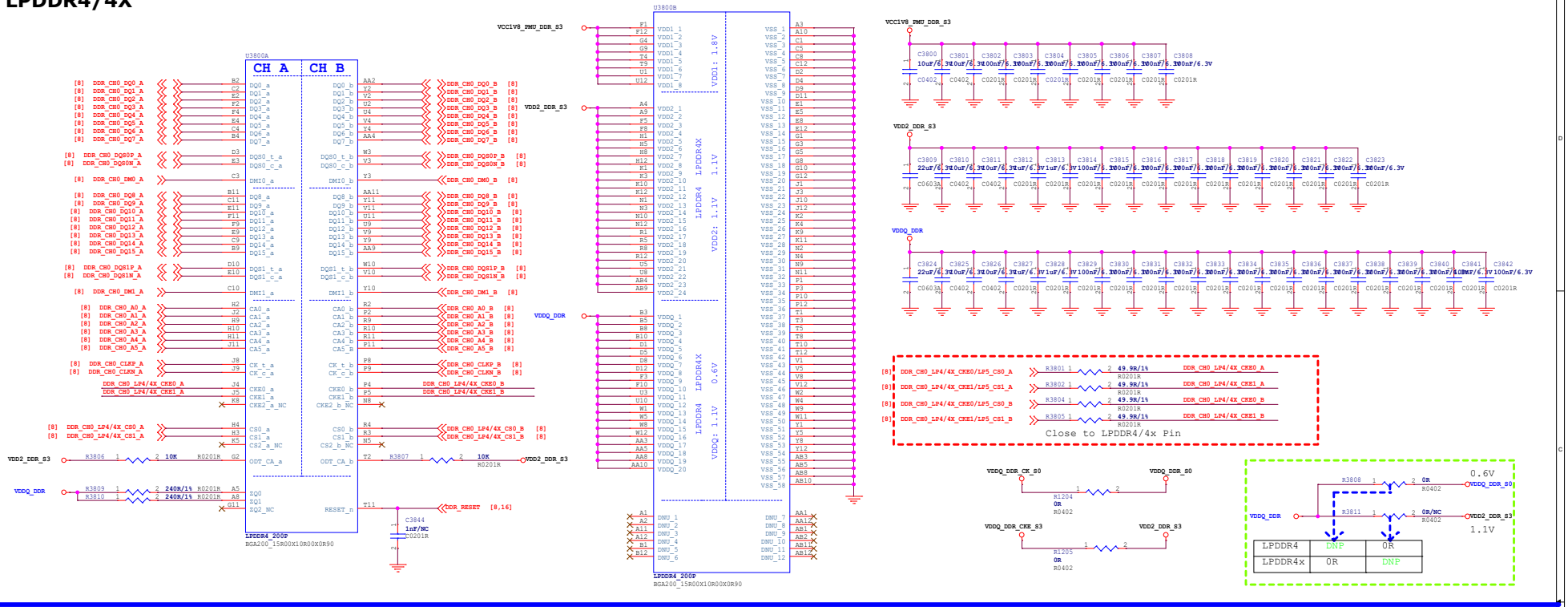
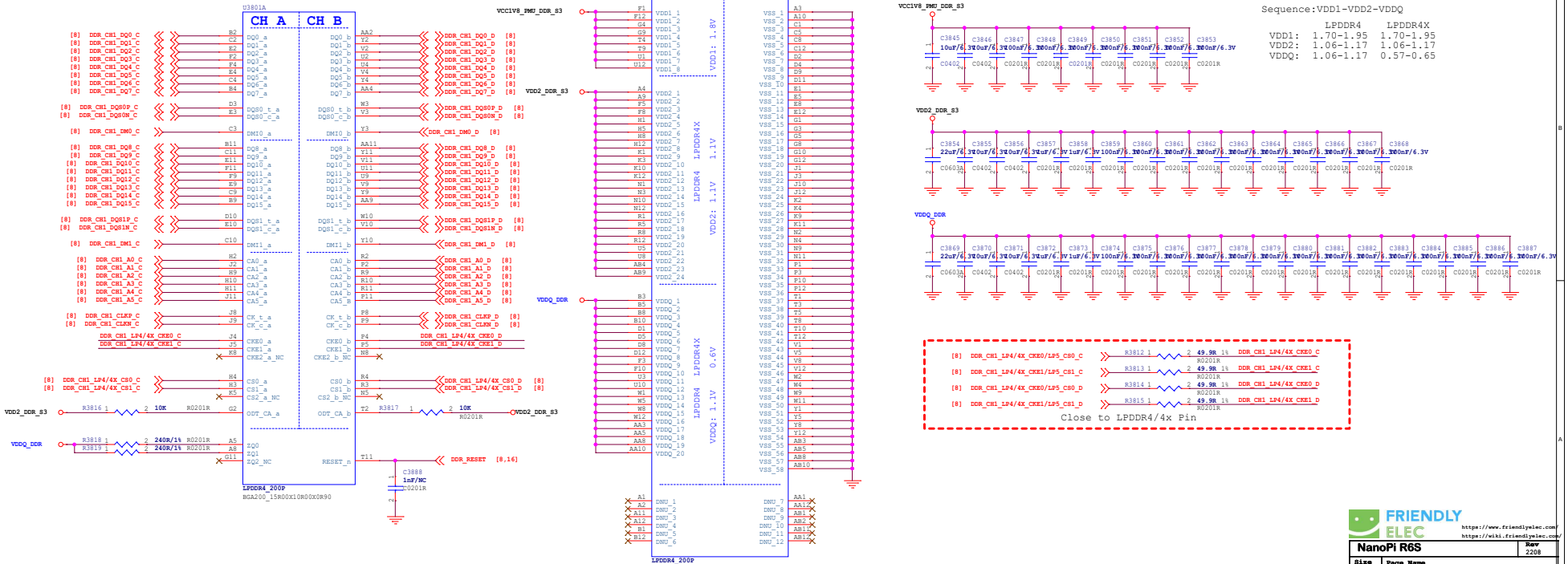
LPDDR4/4X





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Size: Custom	Page Name: 16.DRAM-LPDDR4X_200P_2x32bit
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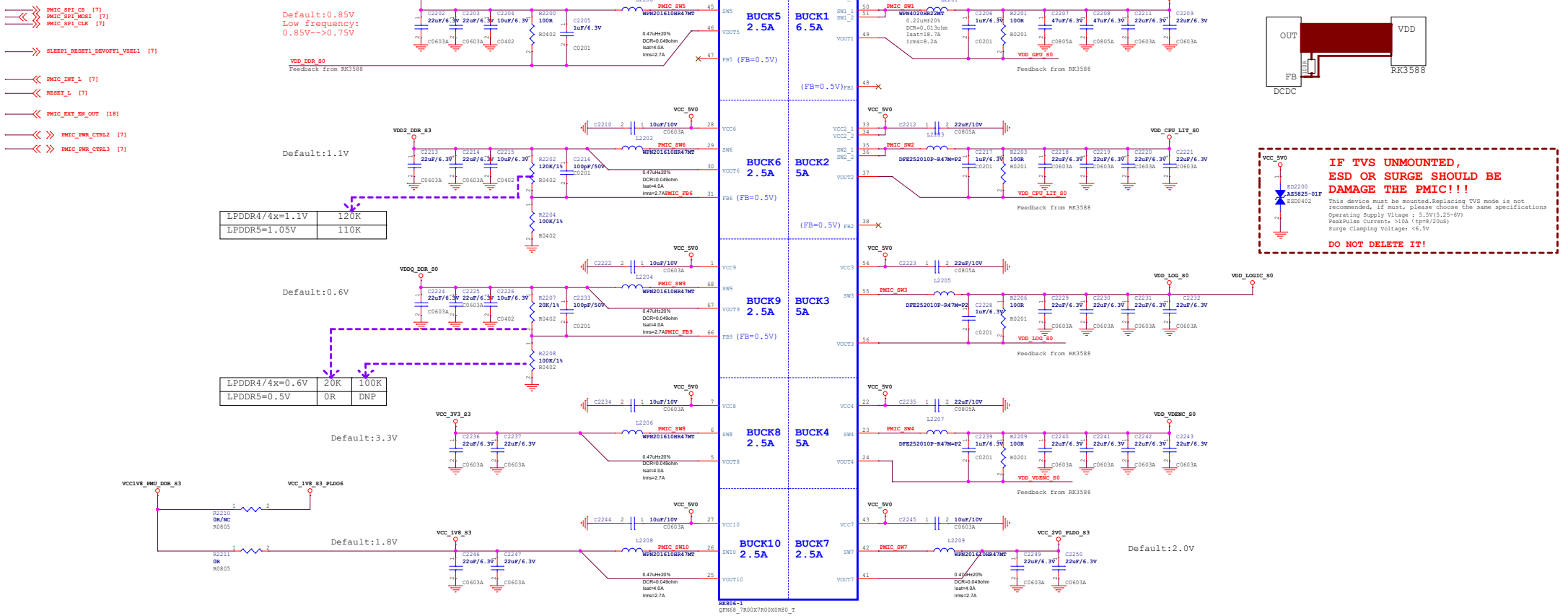
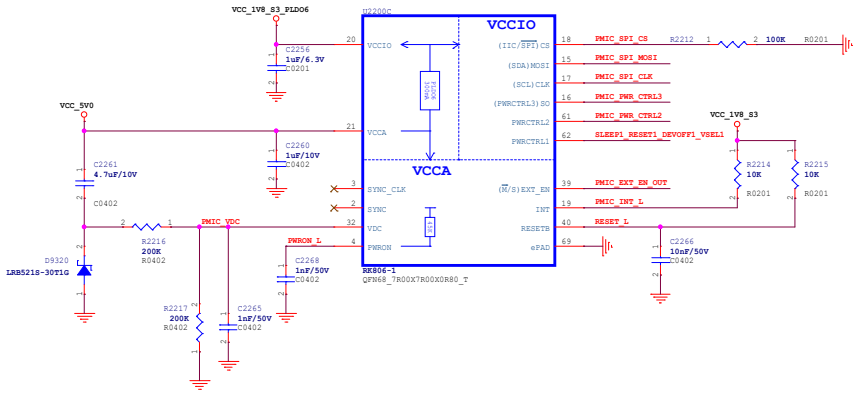
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO

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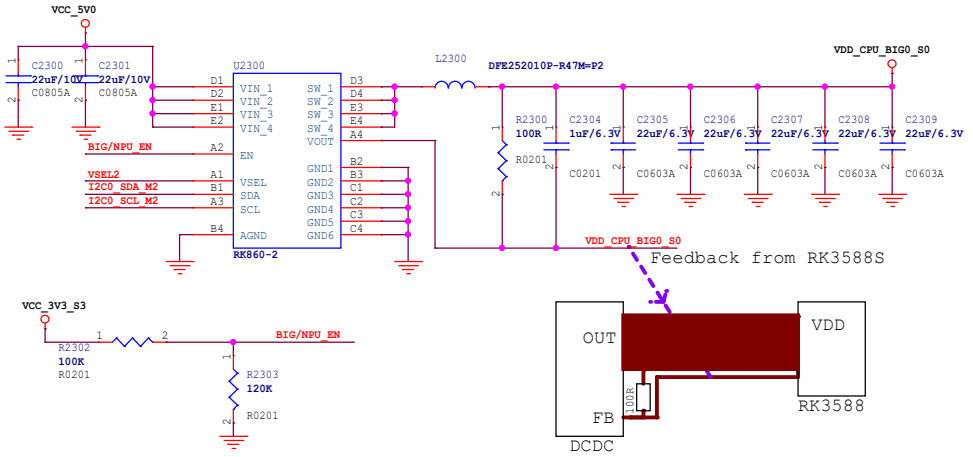
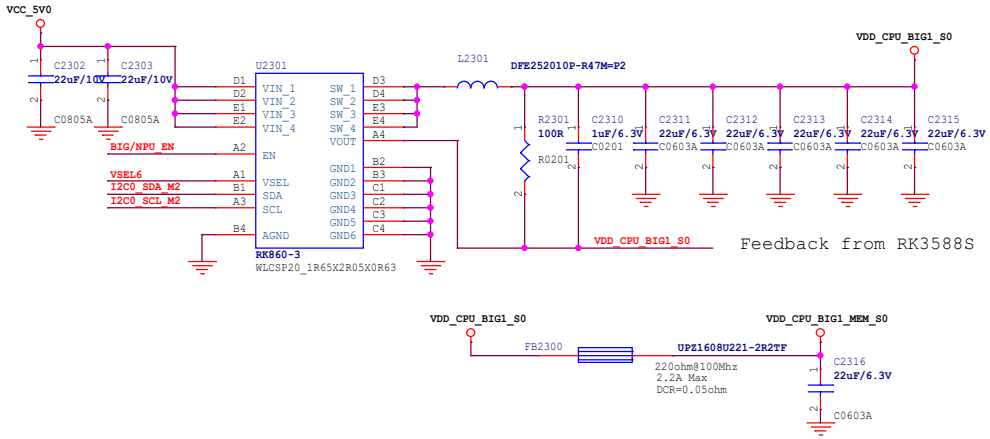
Size A2	Page Name 17.Power-PMIC_RK806-1	
Date: Thursday, October 20, 2022	Sheet: 17/ 27	

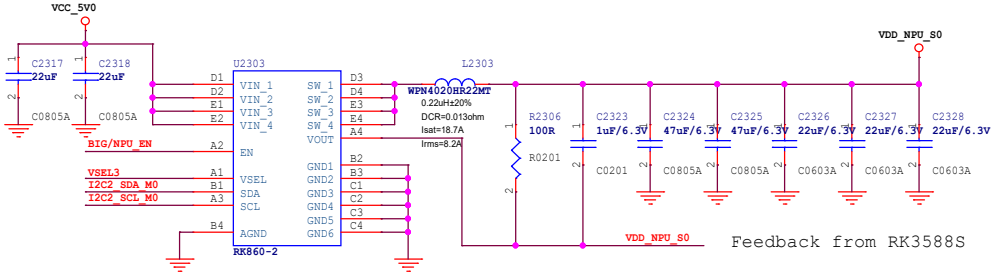
VDD_CPU_BIG0



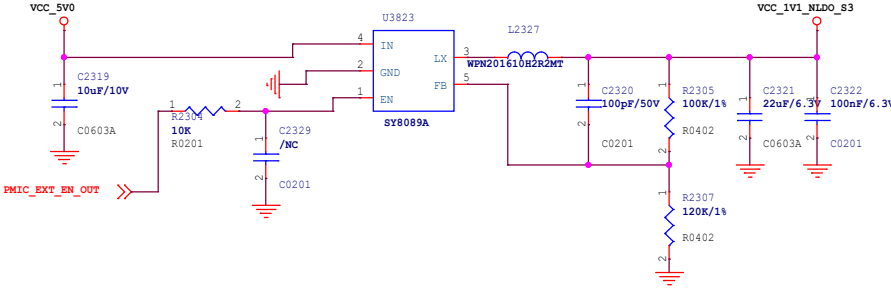
VDD_CPU_BIG1

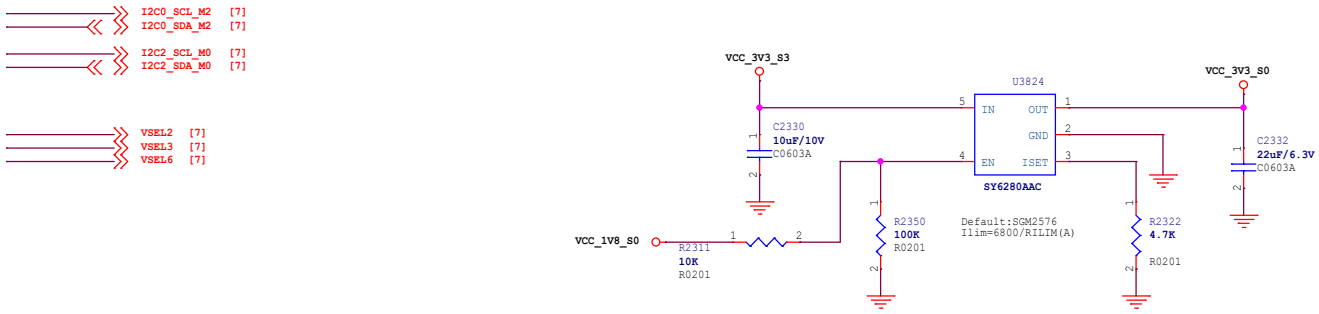


VDD_NPU



VCC_1V1_NLDO_S3





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Size A3	Page Name 18.Power_Ext Discrete	
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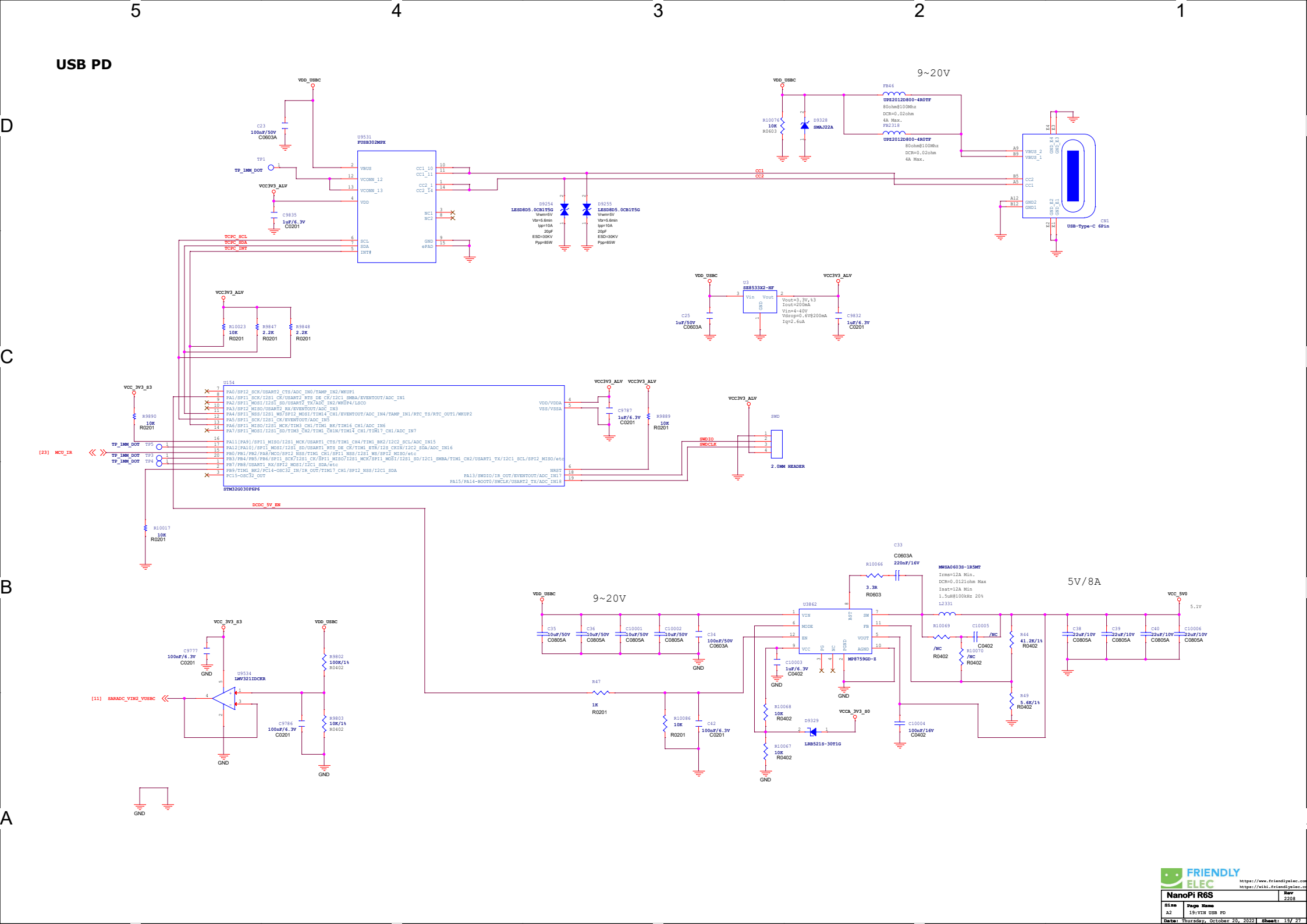
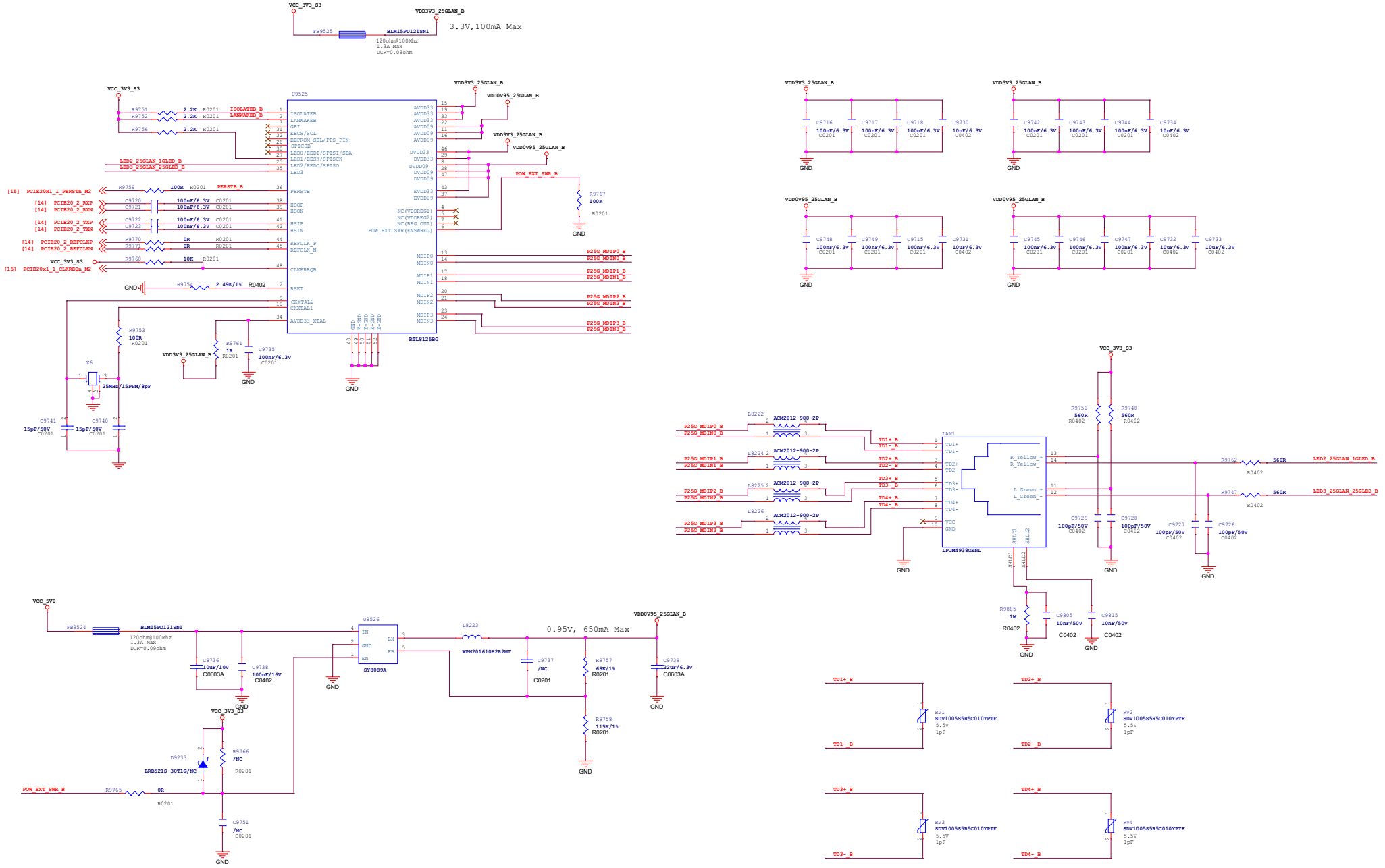
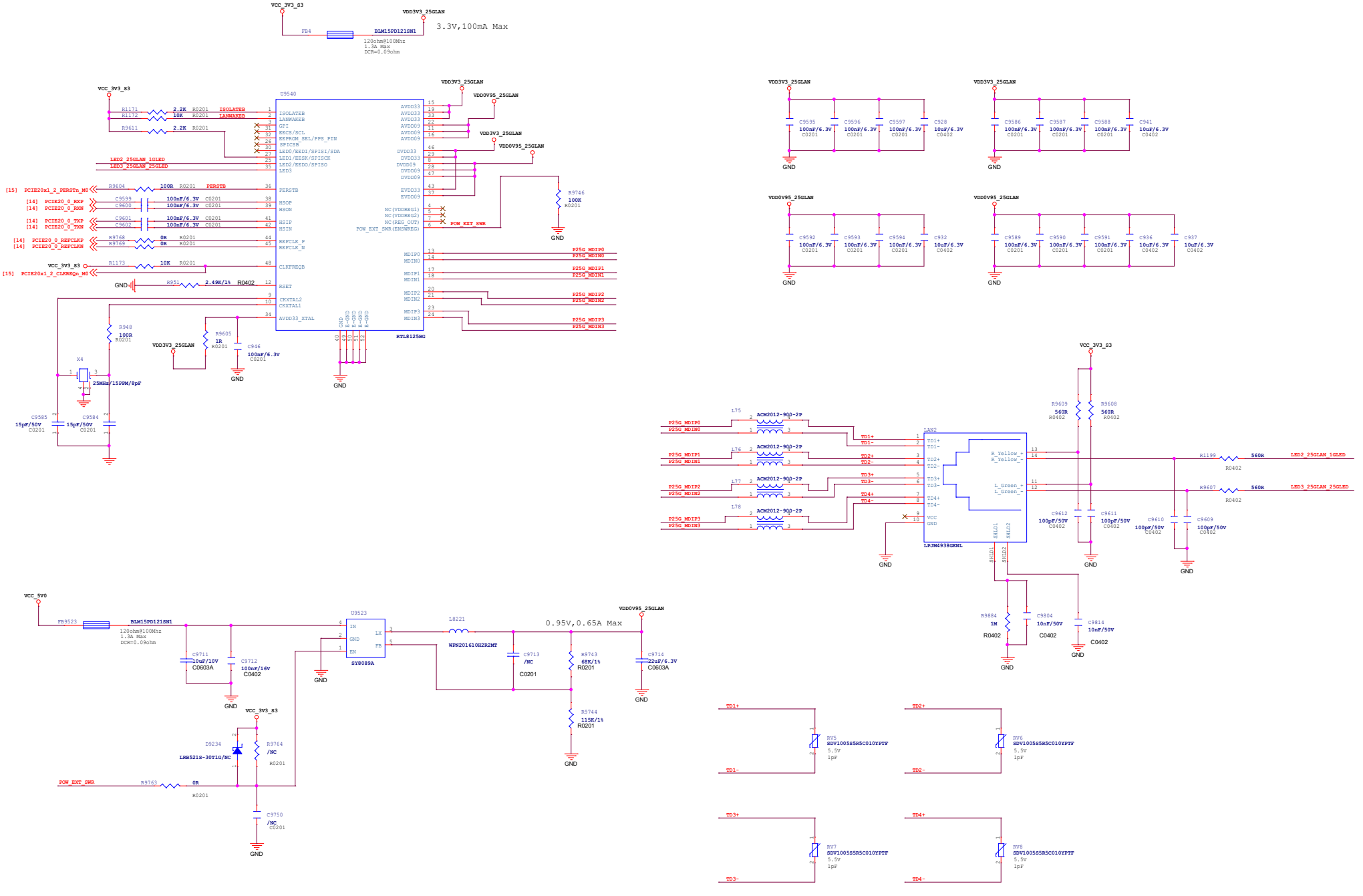


NanoPi R6S	Rev 2208
Size: A2	Page Name: 19:VIN USB PD
Date: Thursday, October 20, 2022	Sheet: 19/ 27

2.5Gbps Ethernet



2.5Gbps Ethernet



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Size A2	Page Name 21:2.5Gbps Ethernet B
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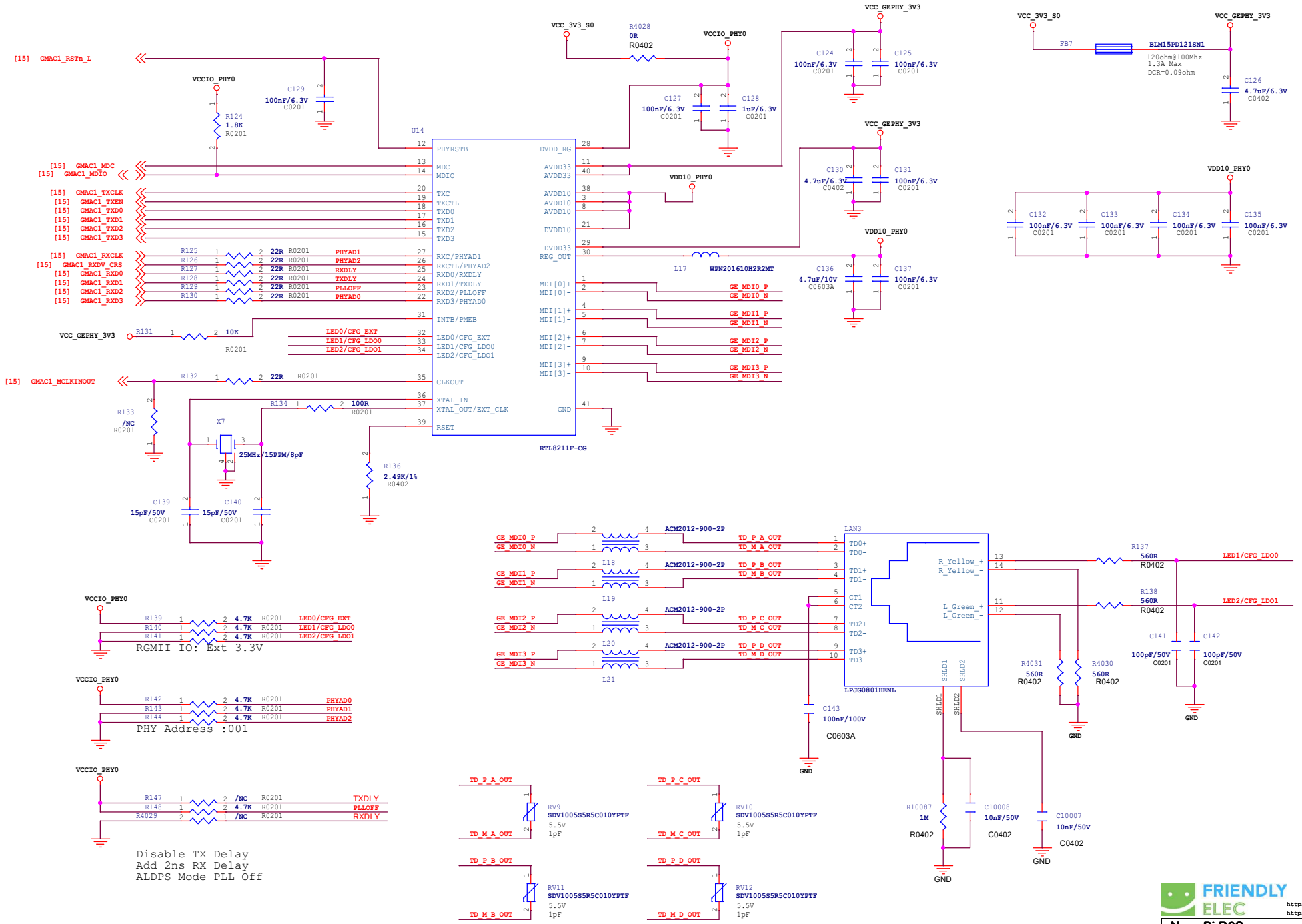
1G Ethernet



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NanoPi R6S	Rev 2208
Size A3	Page Name 22:1Gbps Ethernet
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5 4 3 2 1

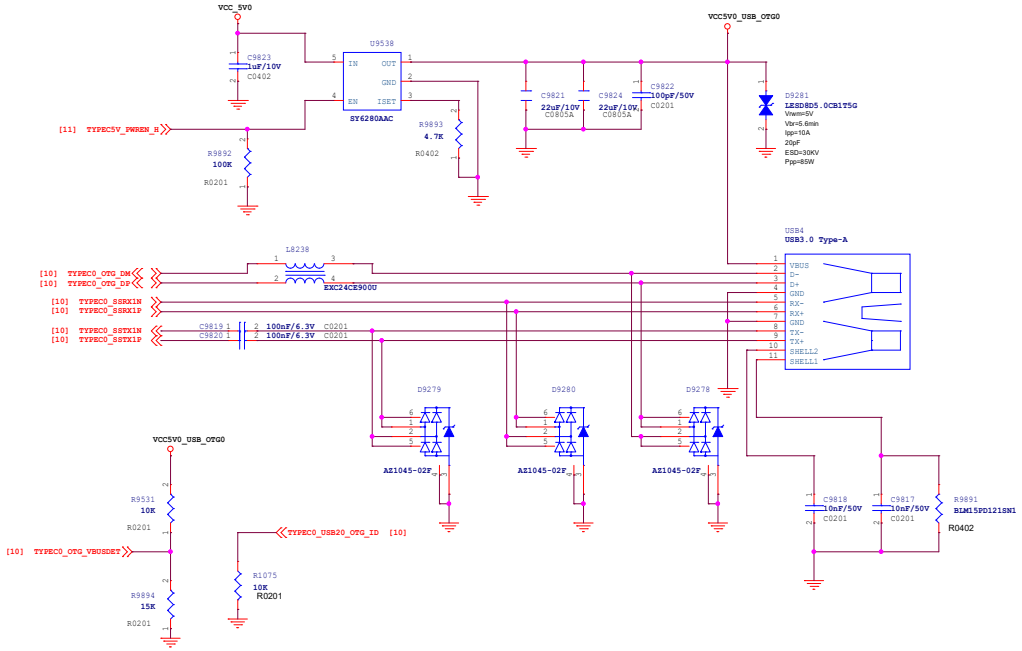
D

C

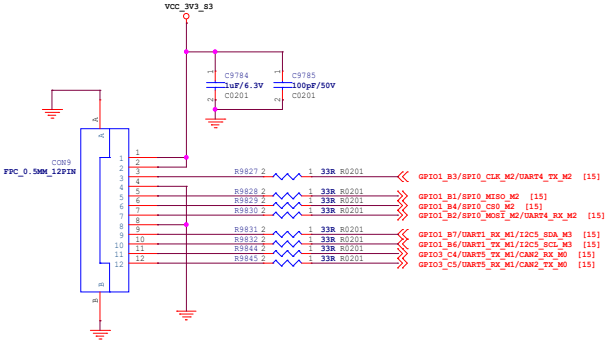
B

A

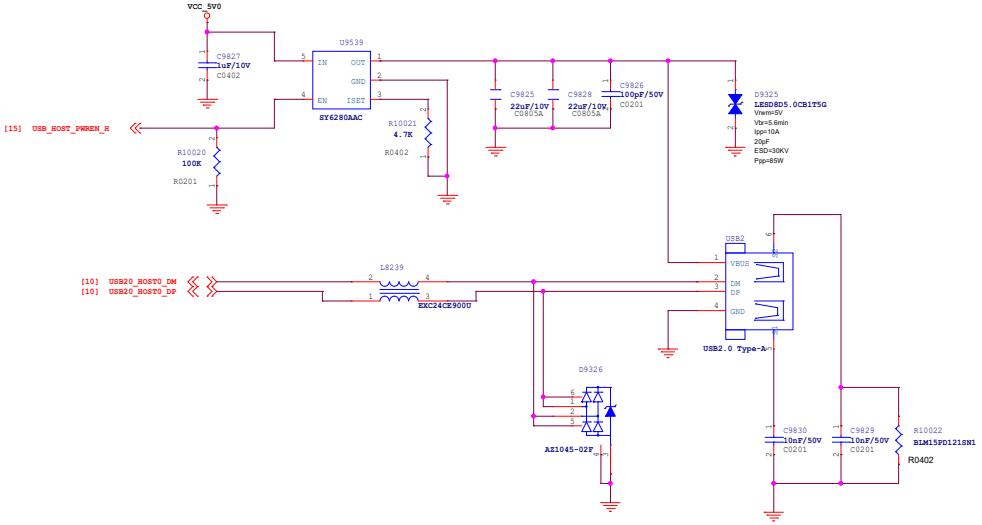
USB 3.0/ADB/MASK



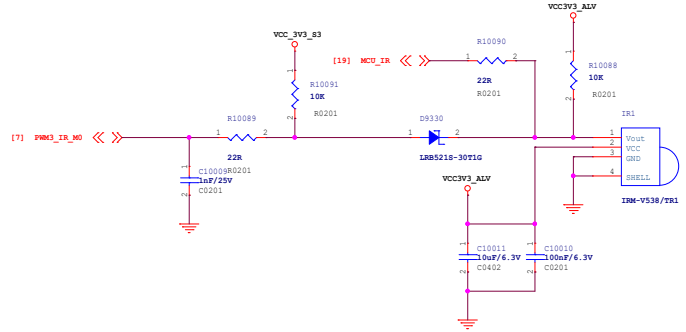
GPIO



USB 2.0



IR



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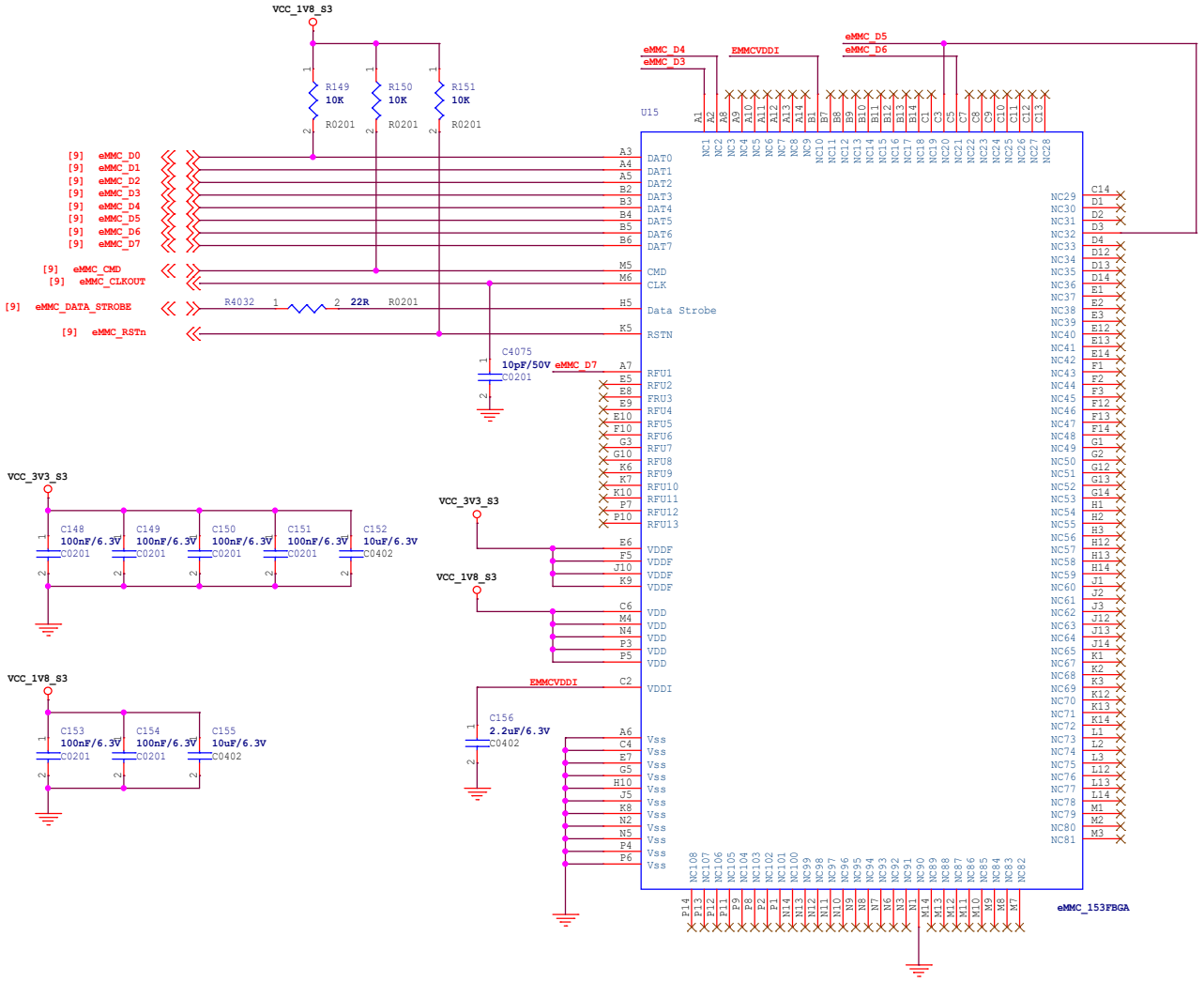
eMMC



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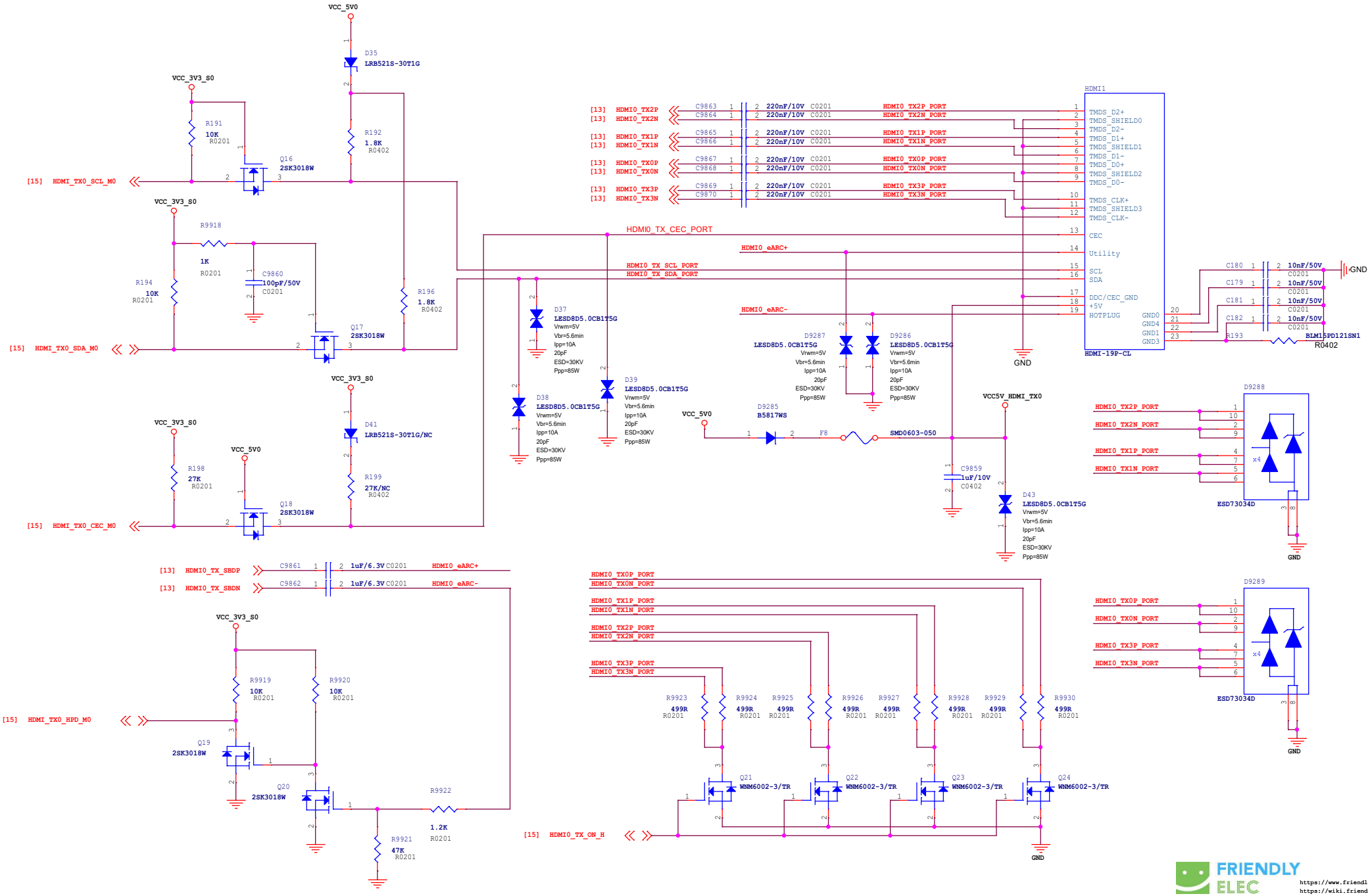
HDMI TX0



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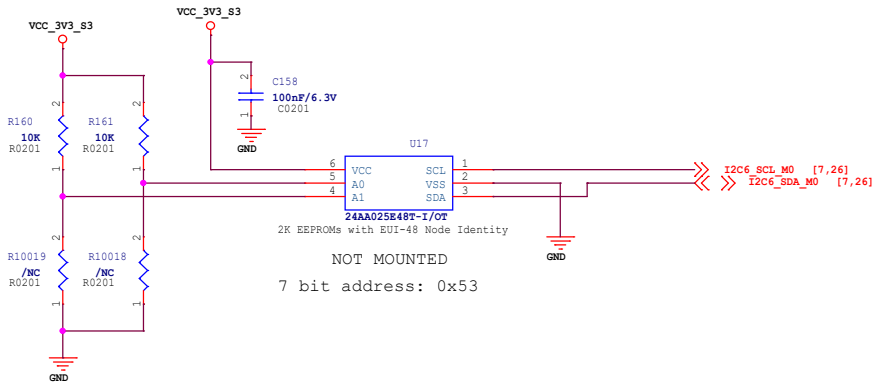
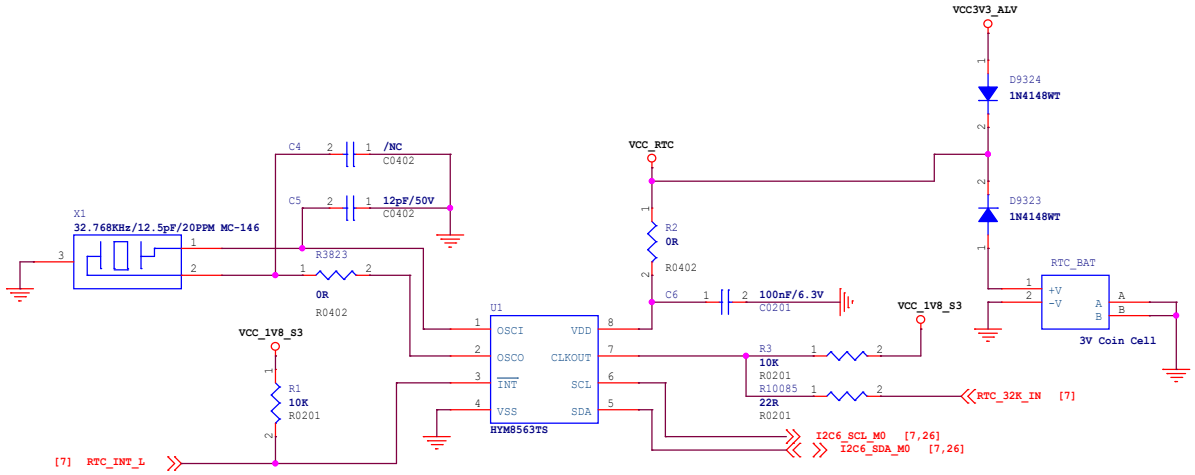
EUI-48 Node Identity

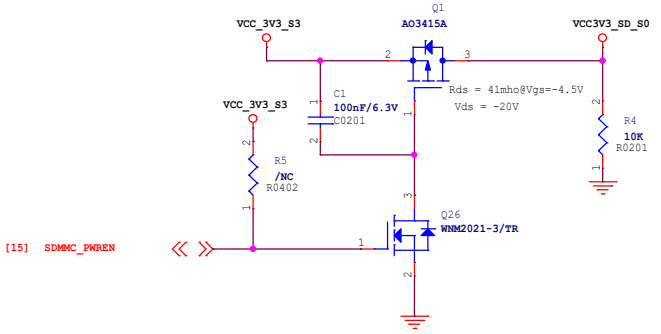


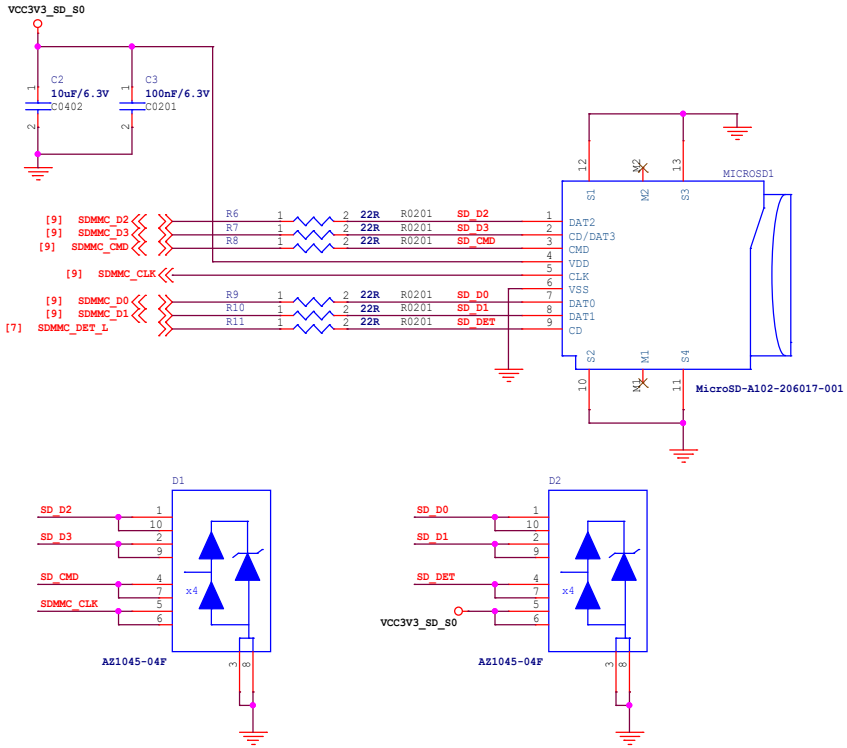
RTC



Address:Read A3H, Write A2H
7bit address: 0x51

microSD





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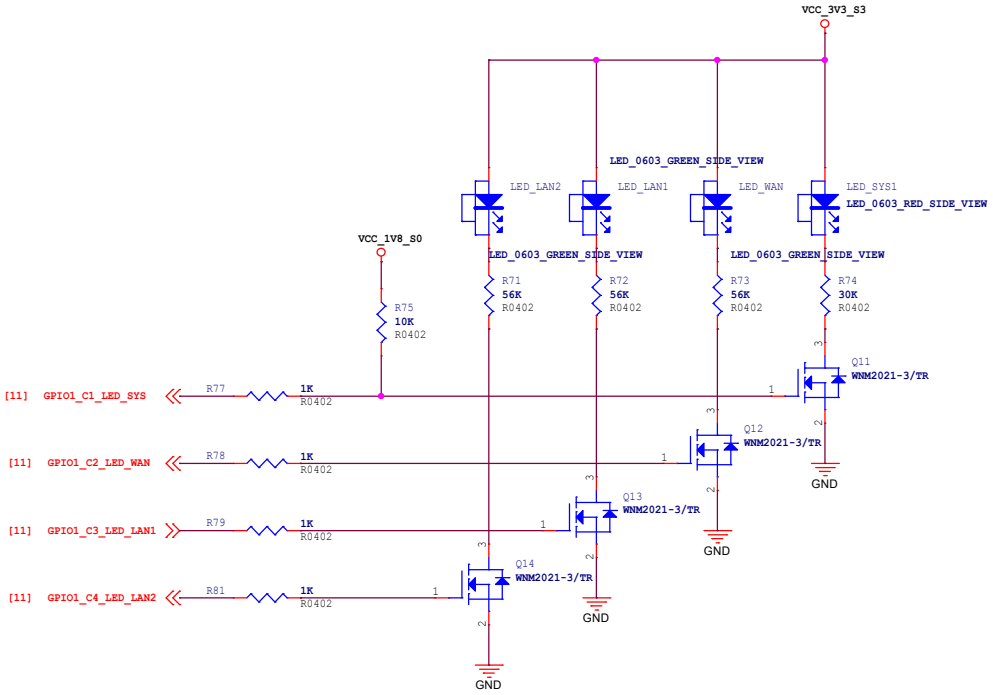
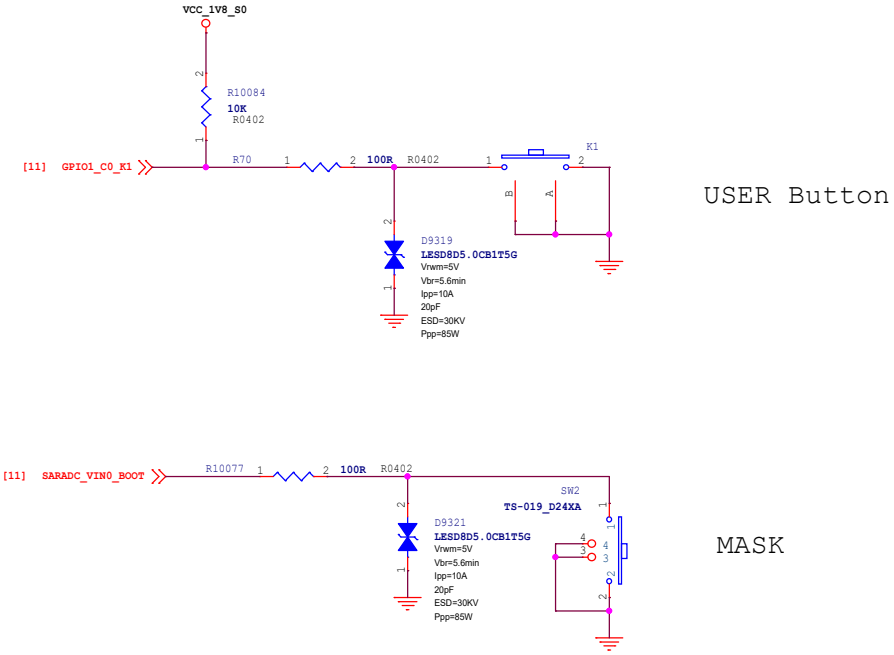
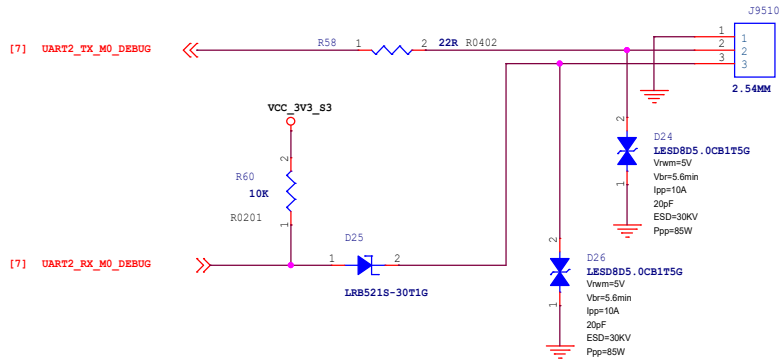
LED

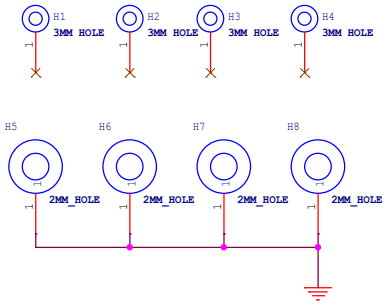


Button



Debug UART





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