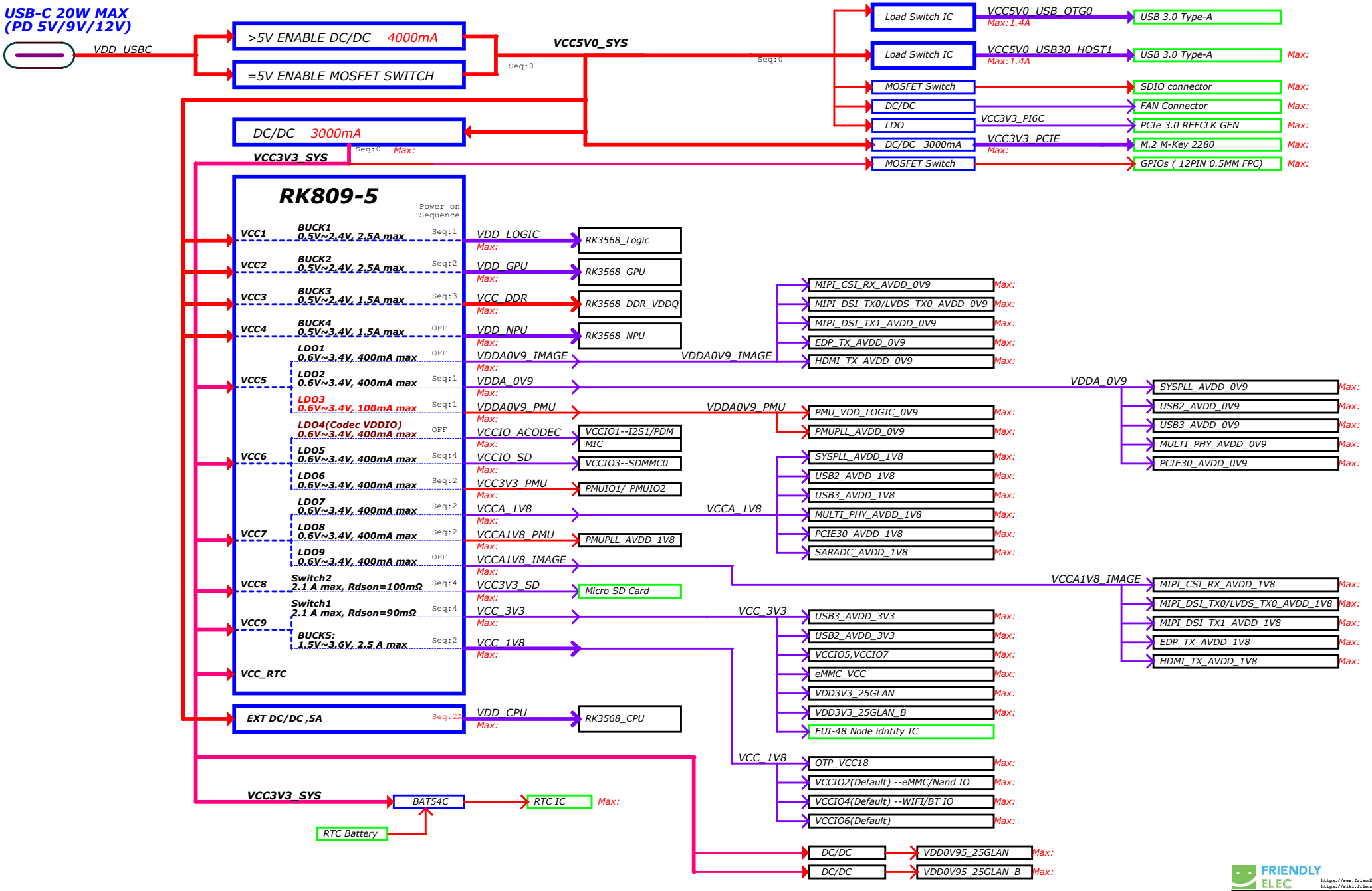
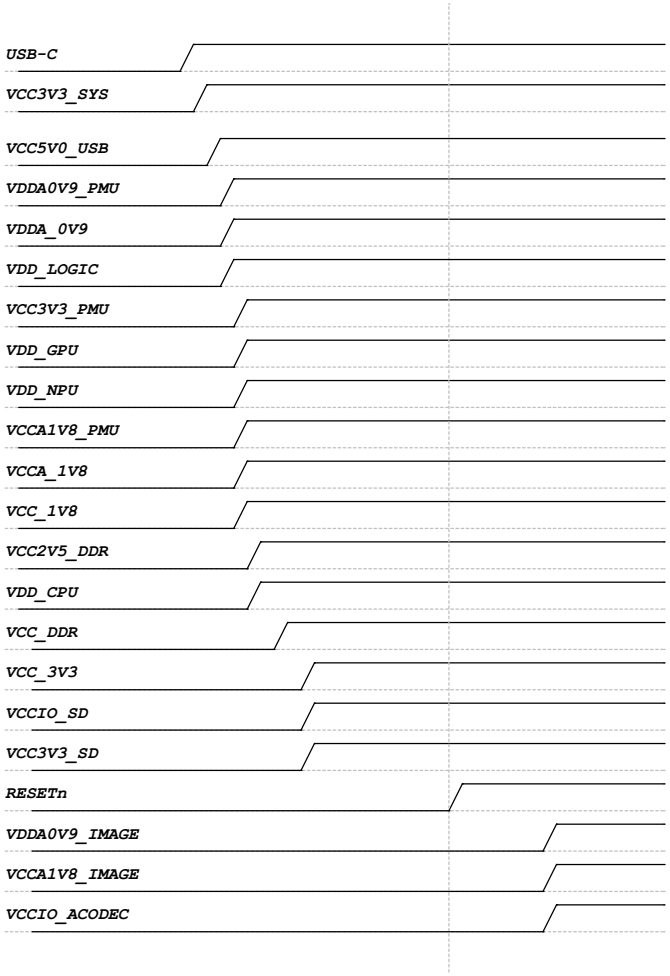
Power Diagram



Power Sequence




```
# I2C5,  7bit address
- 0x51,  HYM8563TS, RTC IC
- 0x53,  24AA025E48T, EUI-48 Node Identity
```

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYSP	Slot:0	3.3V	ON	ON		
VCC3V3_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD

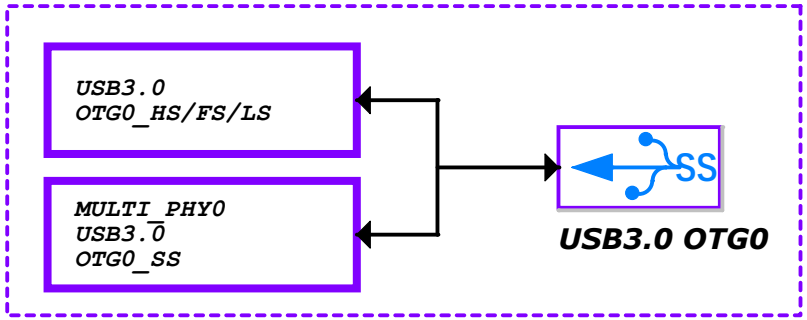
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

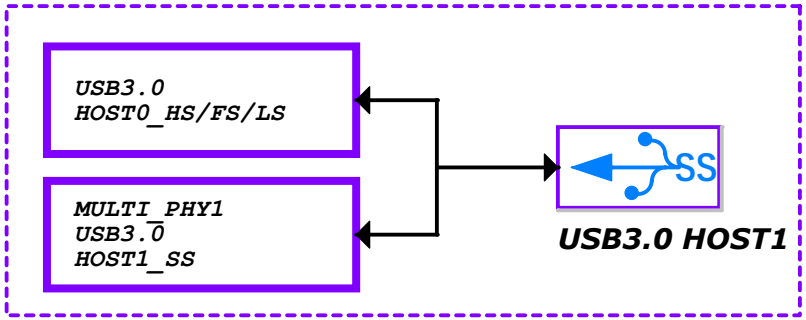
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 02.Power Sequence/IO Domain Map
Date: Thursday, May 05, 2022	Sheet: 2 / 25

USB3.0 OTG0



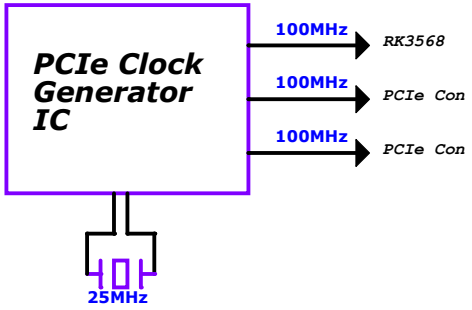
USB3.0 HOST1



PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

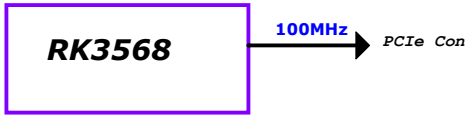
PCIe REFCLK



PCIe2.0 PHY

MULTI_ PHY2	PCIe2.0 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

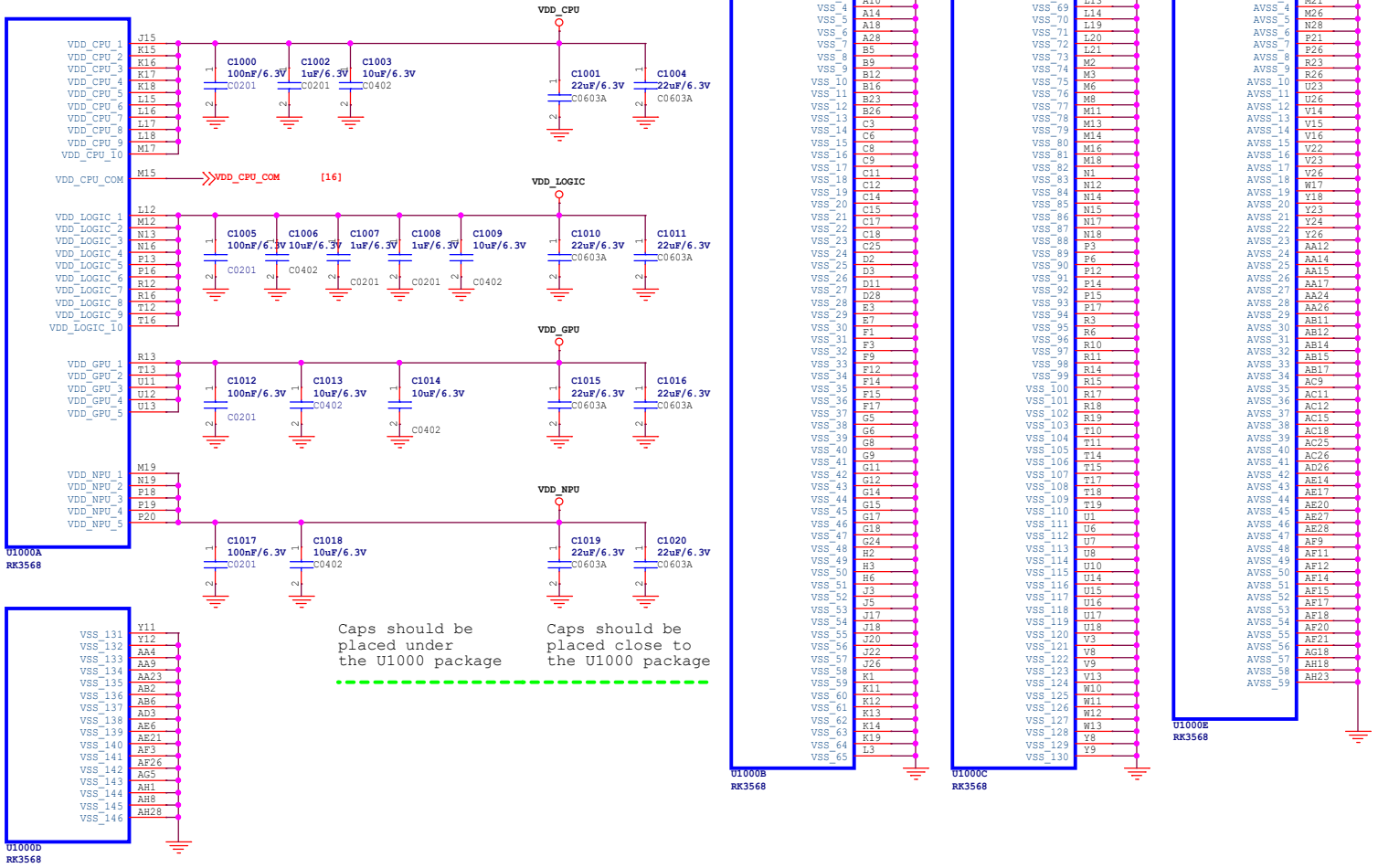
PCIe2.0 REFCLK



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 03.USB3/PCIE30 Fun Map
Date: Thursday, May 19, 2022	Sheet: 3 / 25

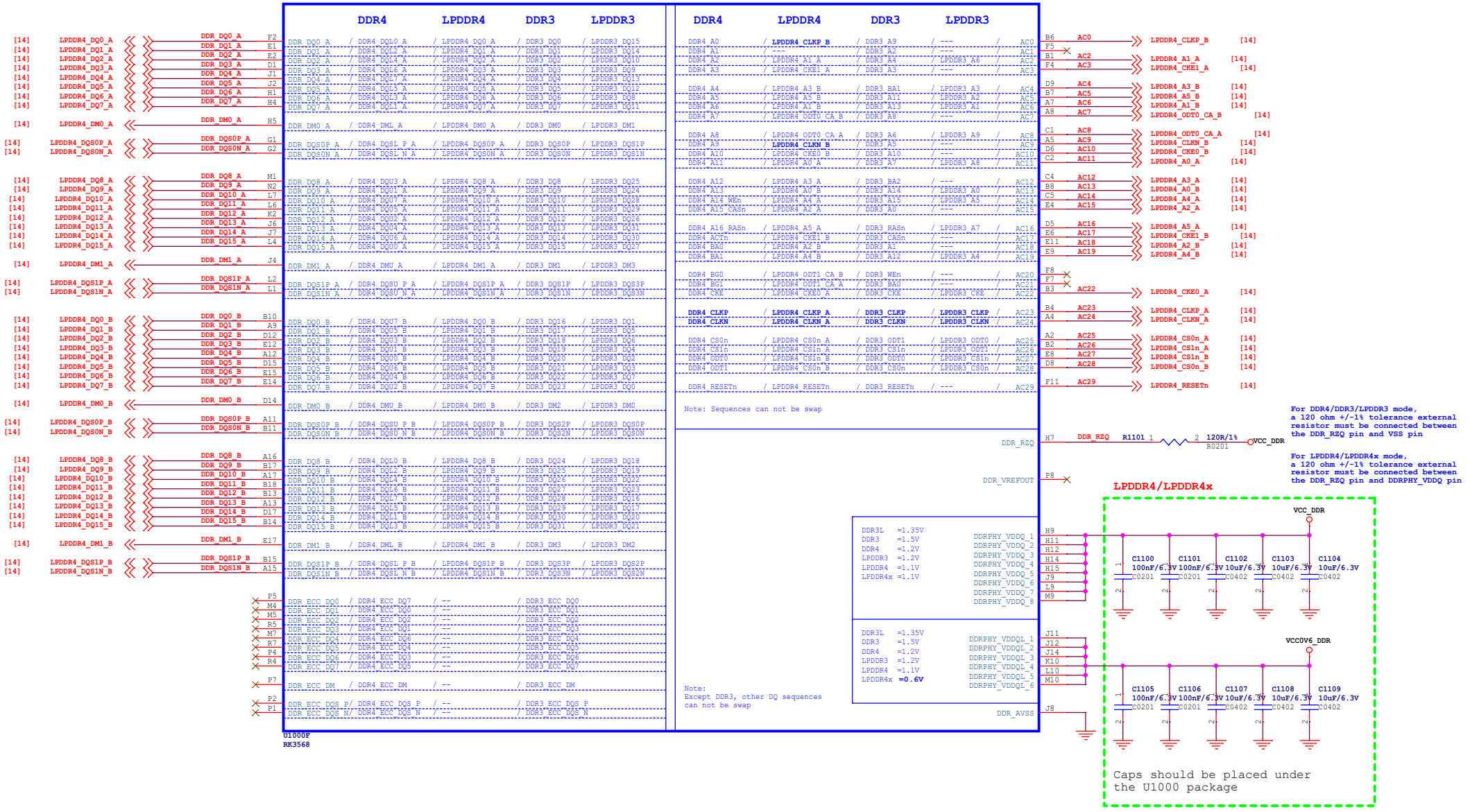
RK3568_ABCDE (Power&Gnd)



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 04.RK3568_Power/GND
Date: Thursday, May 05, 2022	Sheet: 4 / 25

RK3568_F (DDR PHY)



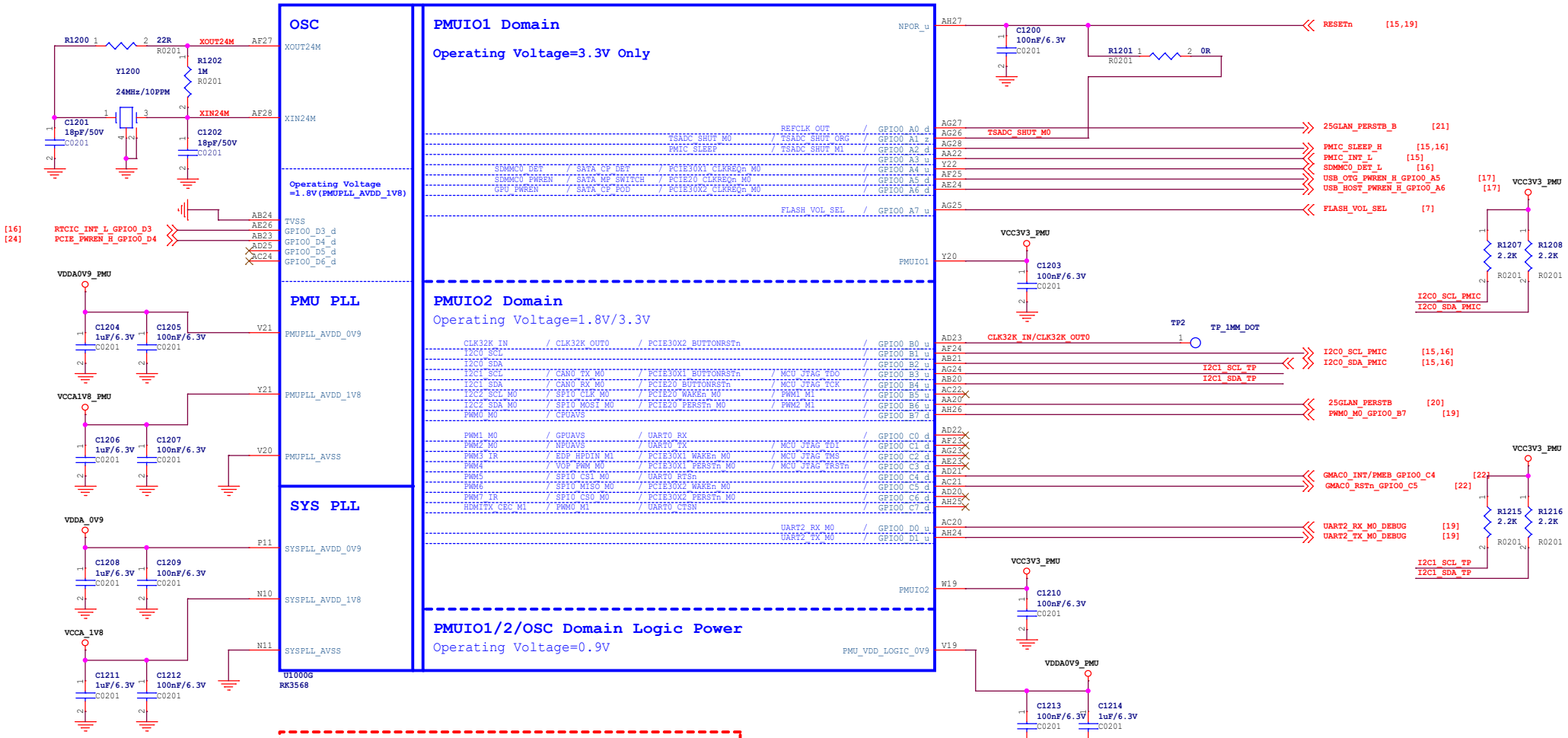
For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 05.RK3568_DDR PHY
Date: Thursday, May 05, 2022	Sheet: 5 / 25

RK3568_G(OSC/PLL/PMUIO1/2)

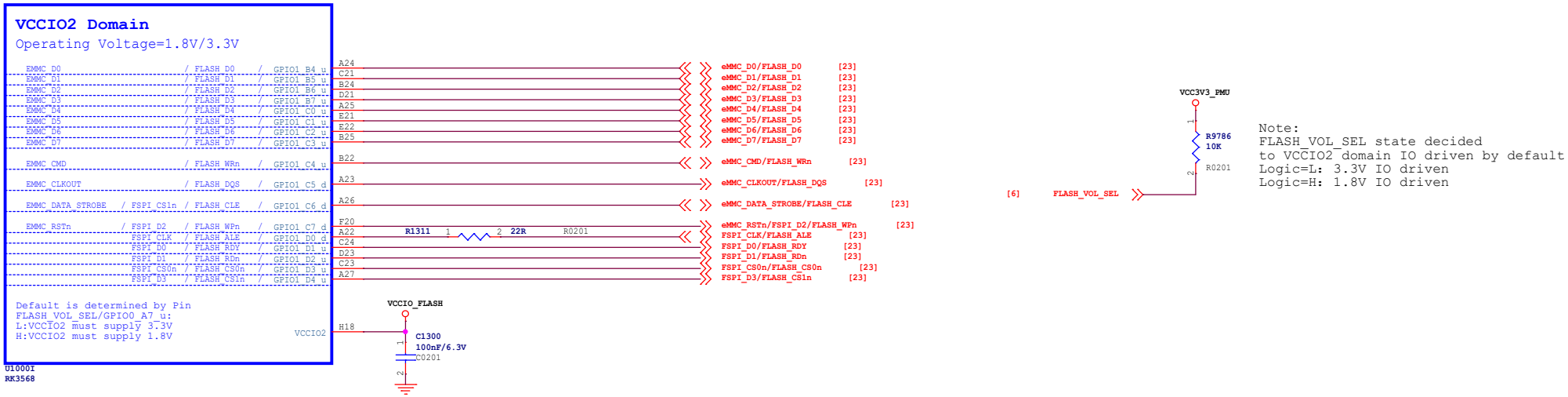


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

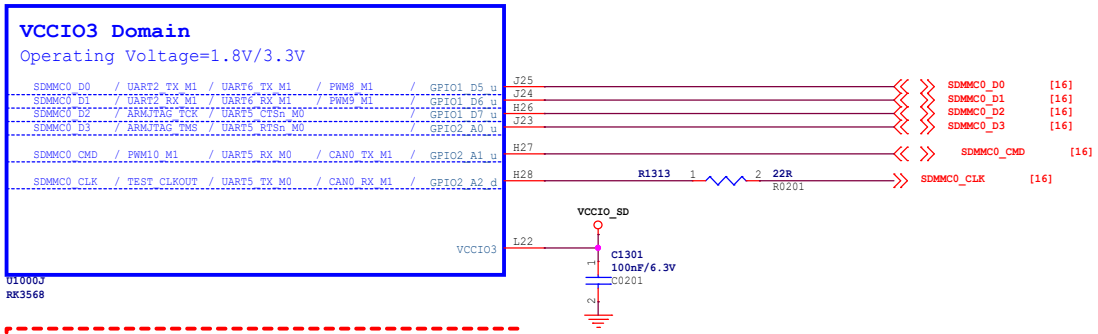
NanoPi R5S	Rev 2204
Size A3	Page Name 06.RK3568_OSC/PLL/PMUIO
Date: Thursday, May 05, 2022	Sheet: 6 / 25

RK3568_I(VCCIO2 Domain)



Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

RK3568_J(VCCIO3 Domain)

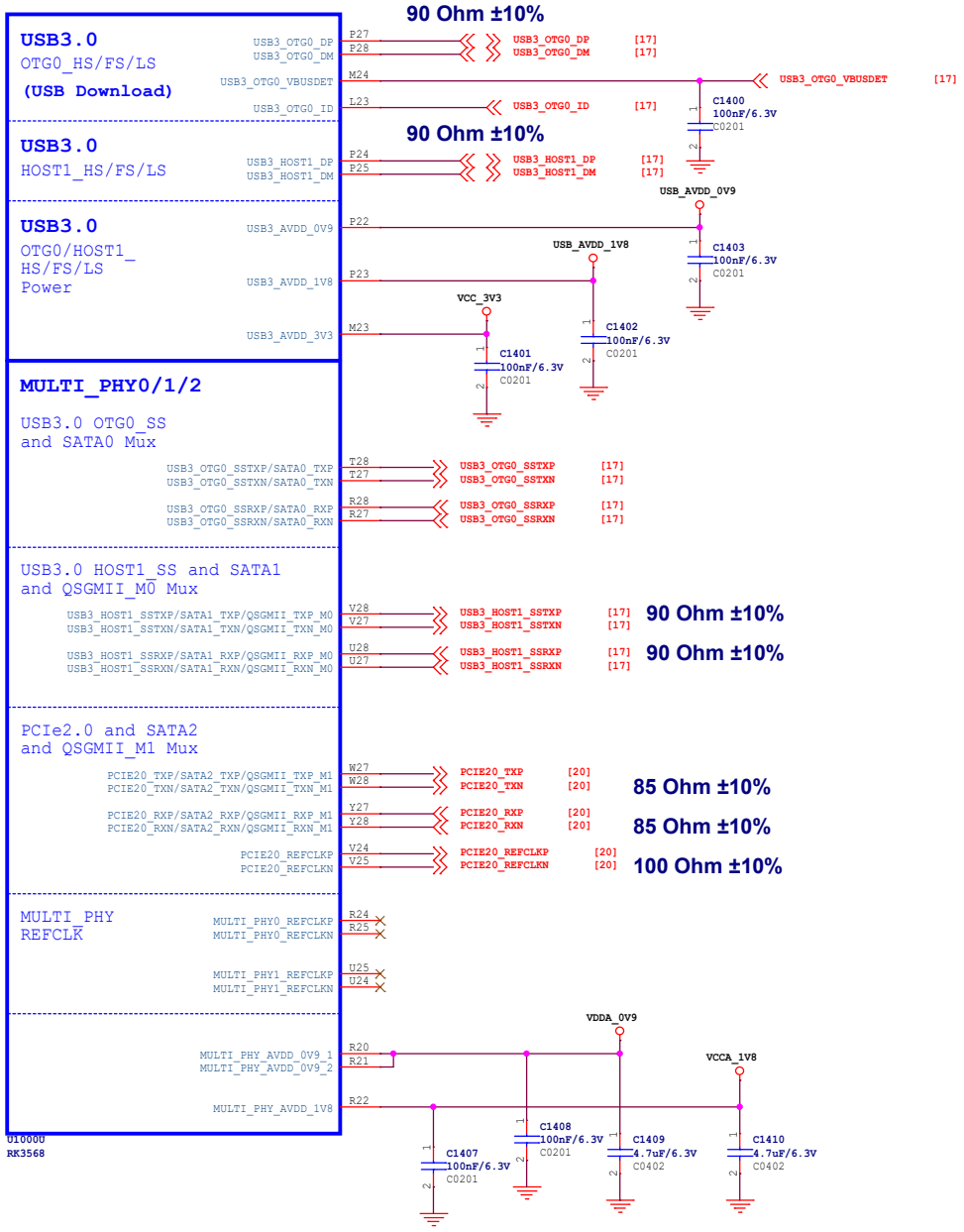


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

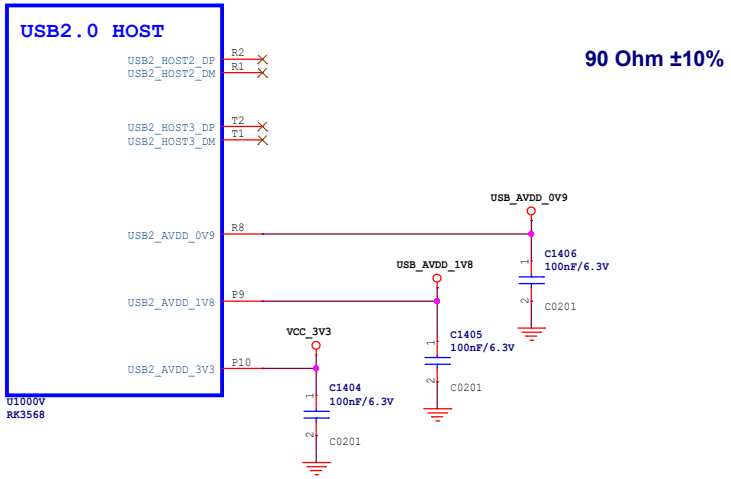
NanoPi R5S	Rev 2204
Size A3	Page Name 07.RK3568_Flash/SD Controller
Date: Thursday, May 05, 2022	Sheet: 7 / 25

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

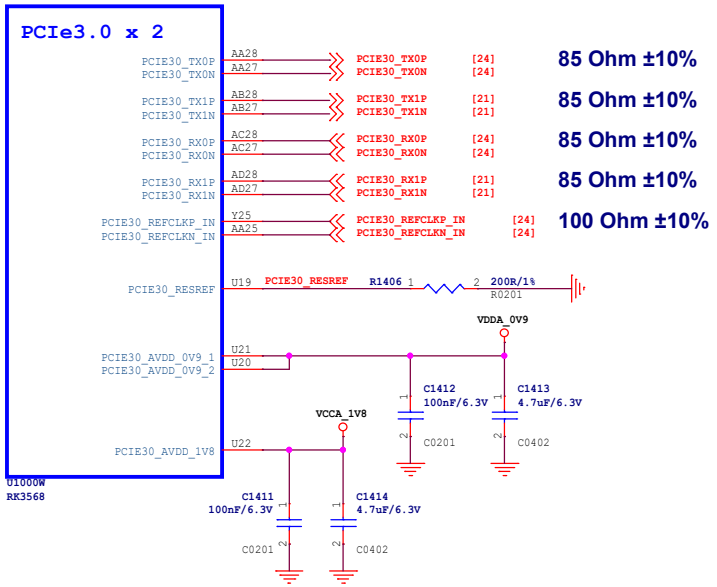


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



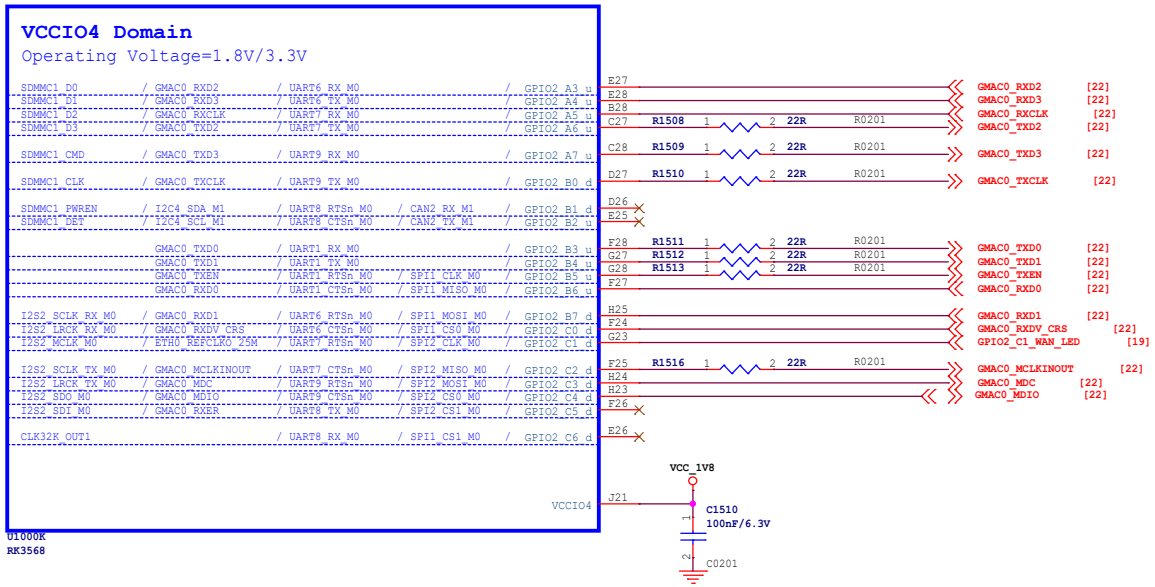
RK3568_W(PCIe3.0 x2)



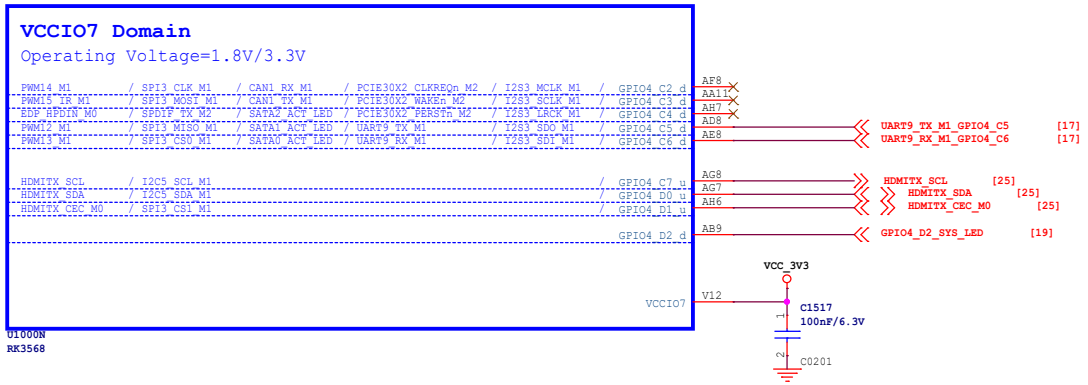
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 08.RK3568_USB/PCIe/SATA PHY
Date: Thursday, May 05, 2022	Sheet: 8 / 25

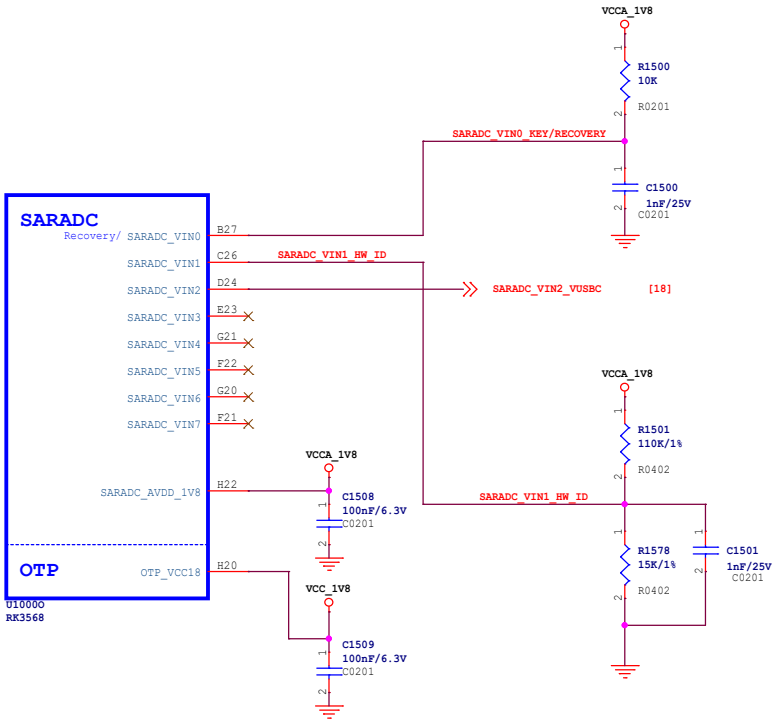
RK3568_K(VCCIO4 Domain)



RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)

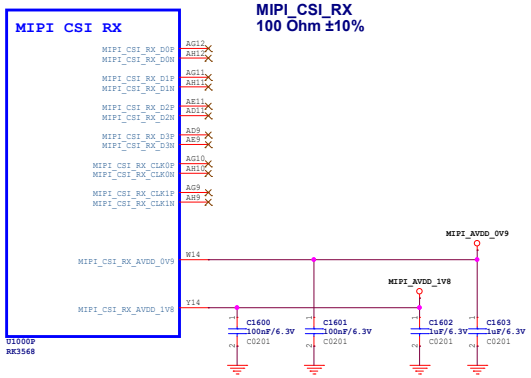


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

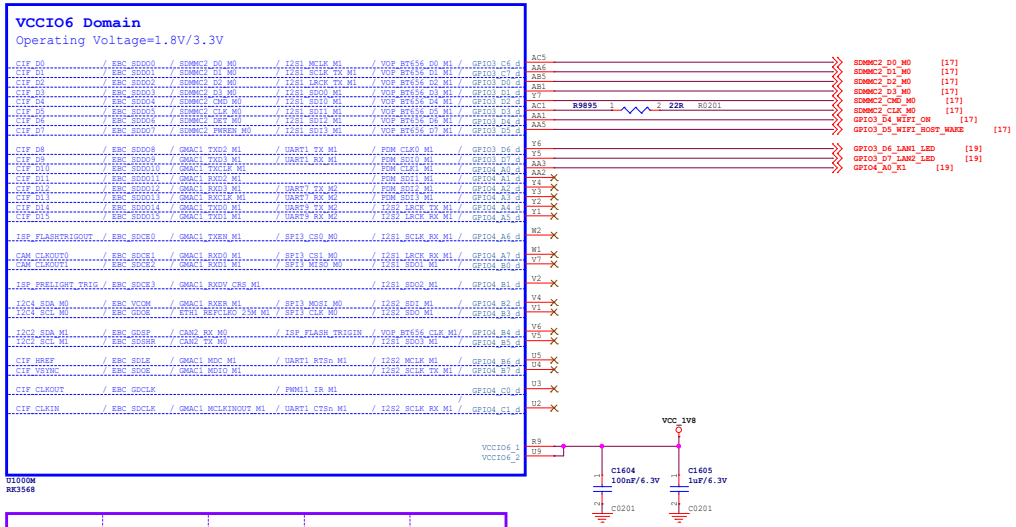
NanoPi R5S	Rev 2204
Size A3	Page Name 09.RK3568_SARADC/GPIO
Date: Thursday, May 05, 2022	Sheet: 9 / 25

RK3568_P(MIPI_CSI_RX)



Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

RK3568_M(VCCIO6 Domain)



Mode	*16bit*	*12bit*	*10bit*	*8bit*
CIF_D0	*D0*	*--*	*--*	*--*
CIF_D1	*D1*	*--*	*--*	*--*
CIF_D2	*D2*	*--*	*--*	*--*
CIF_D3	*D3*	*--*	*--*	*--*
CIF_D4	*D4*	*D0*	*--*	*--*
CIF_D5	*D5*	*D1*	*--*	*--*
CIF_D6	*D6*	*D2*	*D0*	*--*
CIF_D7	*D7*	*D3*	*D1*	*--*
CIF_D8	*D8*	*D4*	*D2*	*D0*
CIF_D9	*D9*	*D5*	*D3*	*D1*
CIF_D10	*D10*	*D6*	*D4*	*D2*
CIF_D11	*D11*	*D7*	*D5*	*D3*
CIF_D12	*D12*	*D8*	*D6*	*D4*
CIF_D13	*D13*	*D9*	*D7*	*D5*
CIF_D14	*D14*	*D10*	*D8*	*D6*
CIF_D15	*D15*	*D11*	*D9*	*D7*

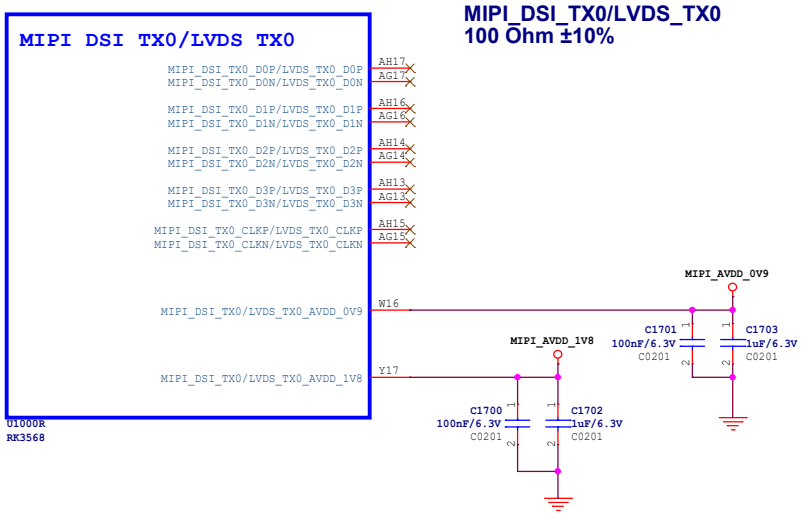
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

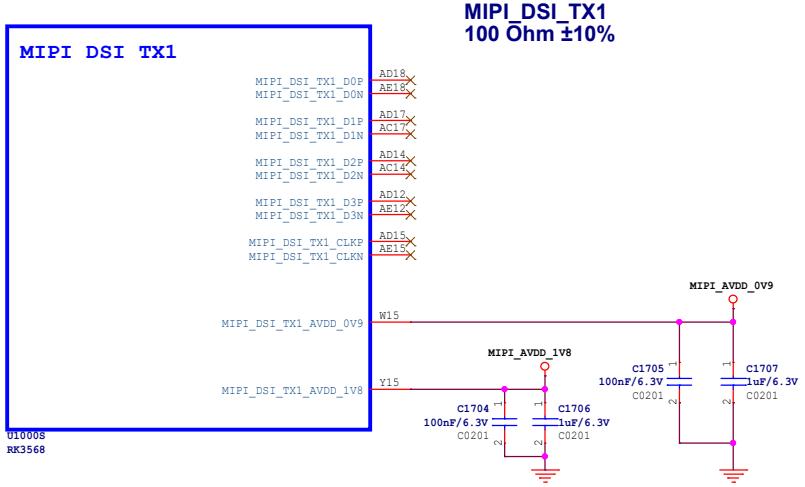
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S		Rev 2204
Size A2	Page Name 10.RK3568_VI Interface	
Date: Thursday, May 05, 2022		Sheet: 10/ 25

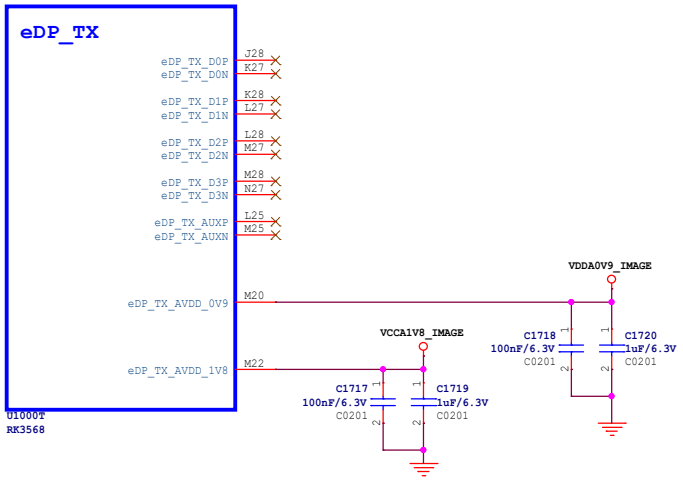
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

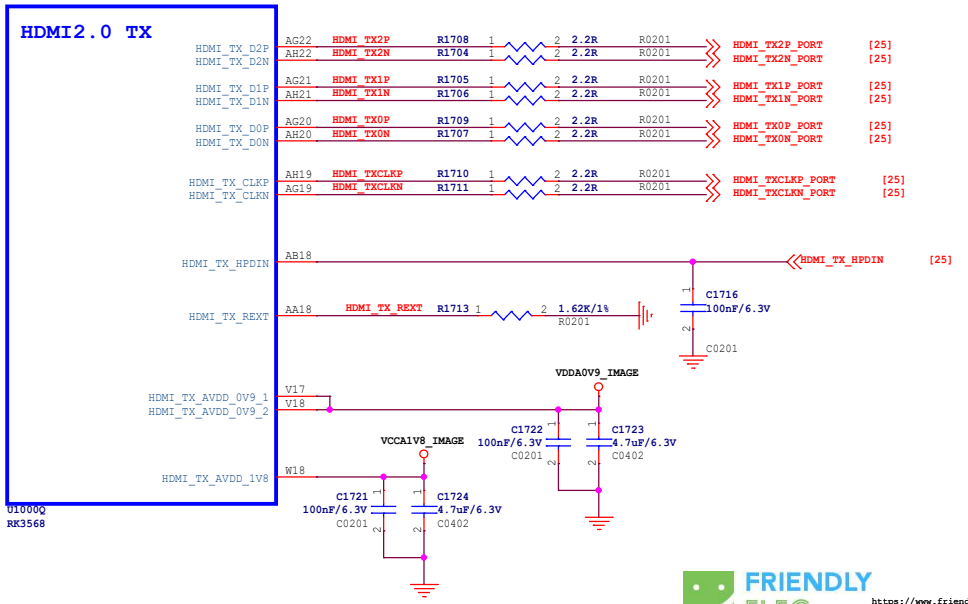


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 11.RK3568_VO Interface_1
Date: Thursday, May 05, 2022	Sheet: 11/ 25

RK3568_L(VCCIO5 Domain)

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

U1000L
RK3568

AG6 AD7 AC8 AC7 AF5 AF6 AD6 AH5 AH4 AB8 AE5 AG4 AF4 AH3 AG3 AH2 AG2 AG1 AF2 AF1 AE1 AE2 AE3 AD4 AD2 AD1 AA7 AC4 AC3 AC2 V10 V11

VCCIO5_1
VCCIO5_2

PCIE30X2_CLKREQn_M1 [24]
PCIE30X2_WAKEn_M1 [24]
PCIE30X2_PERSTn_M1 [24]

SPI1_CS0_M1_GPIO3_A1 [17]

I2C5_SCL_M0 [16,24]
I2C5_SDA_M0 [16,24]

SPI1_MOSI_M1_GPIO3_C1 [17]
SPI1_MISOI_M1_UART5_TX_M1_GPIO3_C2 [17]
SPI1_CLK_M1_UART5_RX_M1_GPIO3_C3 [17]

PWM14_M0_UART7_TX_M1_GPIO3_C4 [17]
PWM15_IR_M0_UART7_RX_M1_GPIO3_C5 [17]

VCC_3V3

C1800 100nF/6.3V C0201

C1801 1uF/6.3V C0201

VCC_3V3

R1802 2.2K R0201

R1803 2.2K R0201

I2C5_SCL_M0
I2C5_SDA_M0

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

FRIENDLY ELEC

https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A4	Page Name 12.RK3568_VO Interface_2
Date: Thursday, May 05, 2022	Sheet: 12/ 25

RK3568_H(VCCIO1 Domain)

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u	D18
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u	E18
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d	A19
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d	B19
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d	F18
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d	A20
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d	C20
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d	B20
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d	D20
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d	E20
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d	A21
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d	B21
					VCCIO1	H17

U1000H
RK3568

D18 — I2C3_SDA_M0
E18 — I2C3_SCL_M0

VCCIO_ACODEC

R1905 2.2K — R0201
R1906 2.2K — R0201

I2C3_SDA_M0
I2C3_SCL_M0

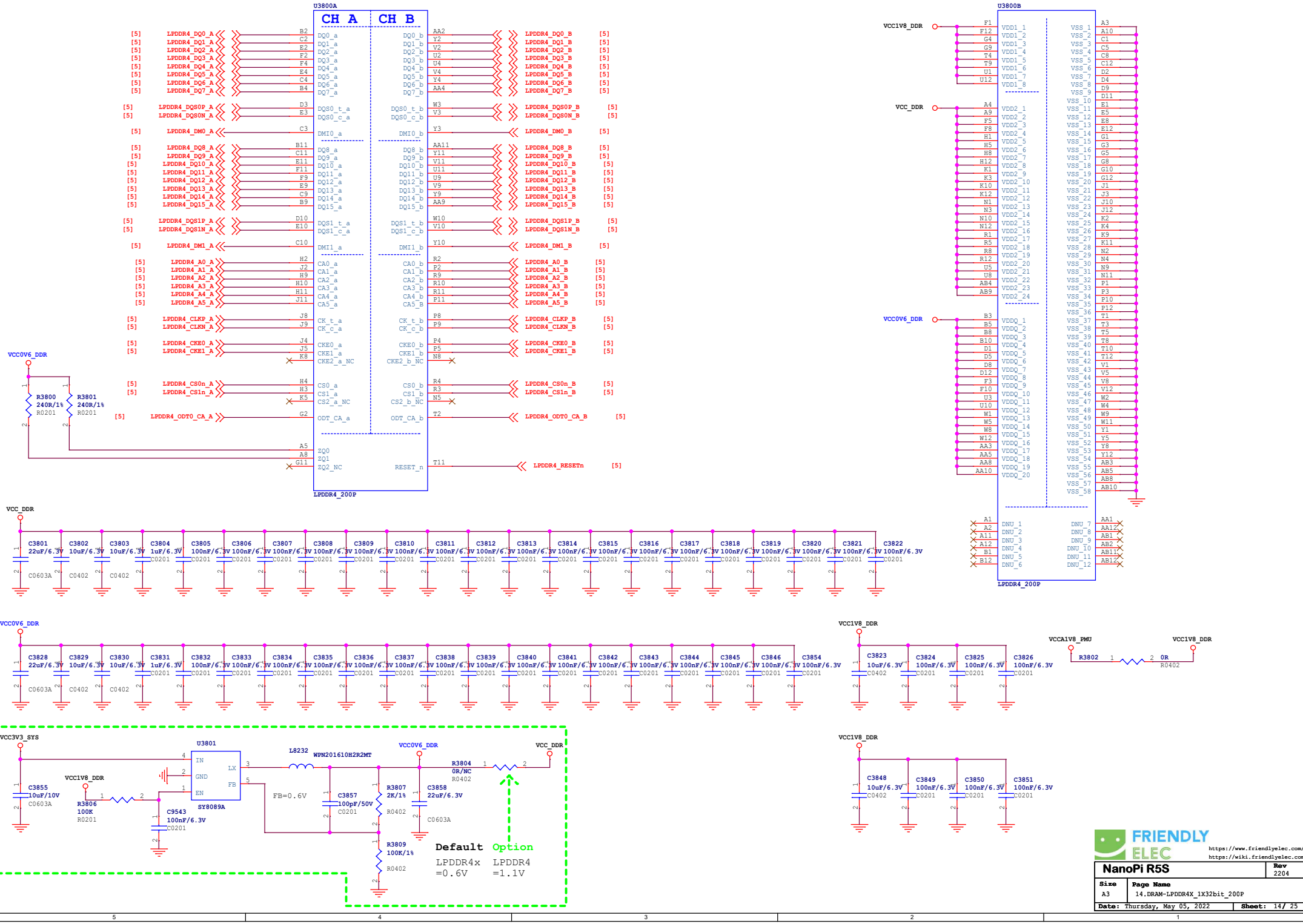
VCCIO_ACODEC

H17 — C1900 100nF/6.3V — C0201

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

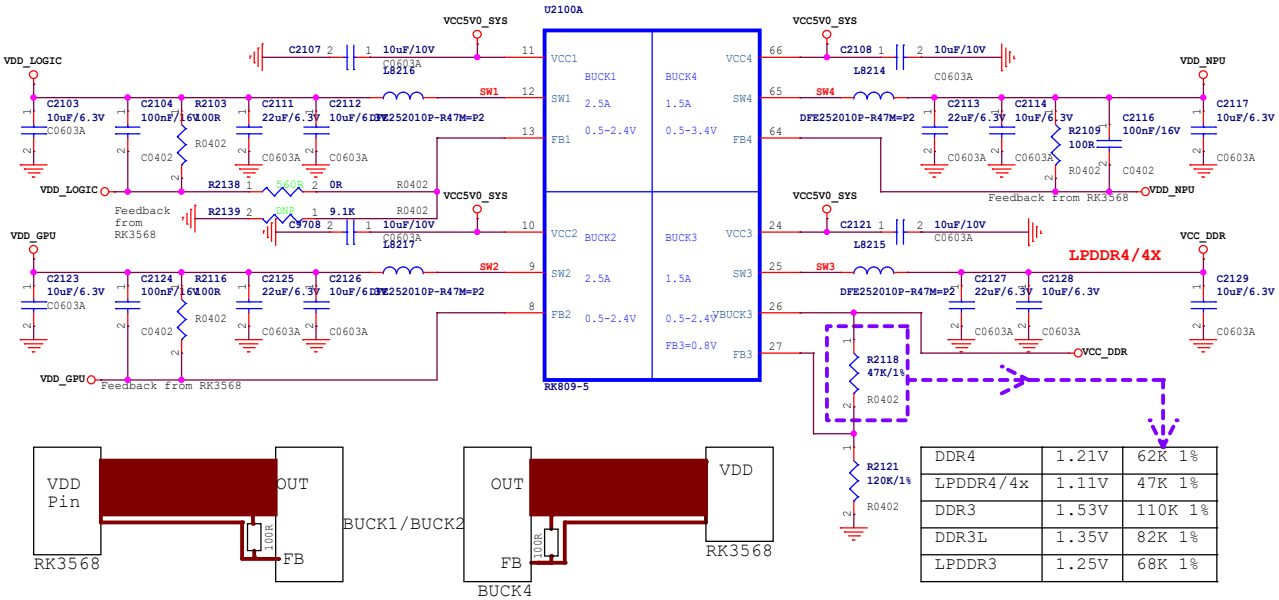
NanoPi R5S	Rev 2204
Size A4	Page Name 13.RK3568_Audio Interface
Date: Thursday, May 05, 2022	Sheet: 13/ 25



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

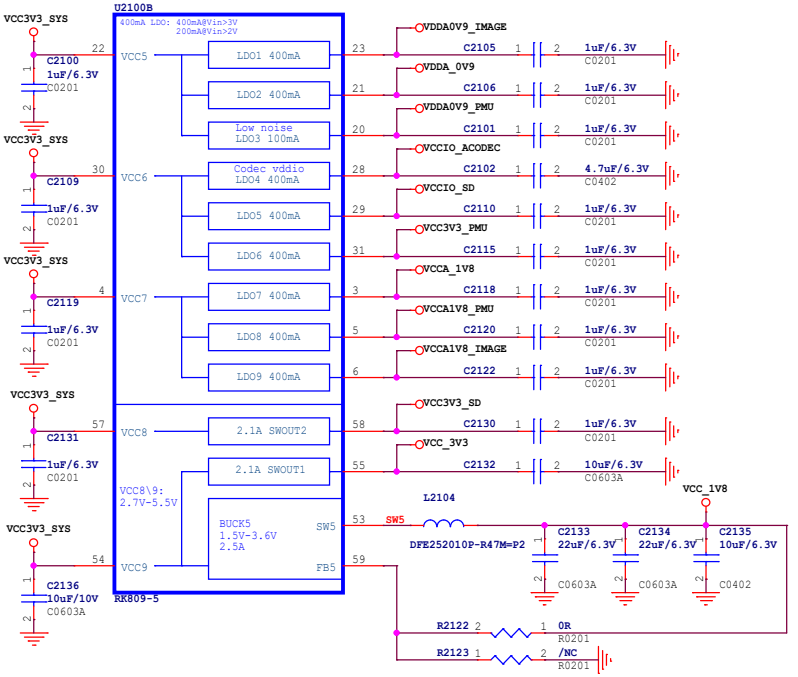
NanoPi R5S	Rev 2204
Size A3	Page Name 14.DRAM-LPDDR4X_1X32bit_200P
Date: Thursday, May 05, 2022	Sheet: 14/ 25

PMIC RK809 DCDC

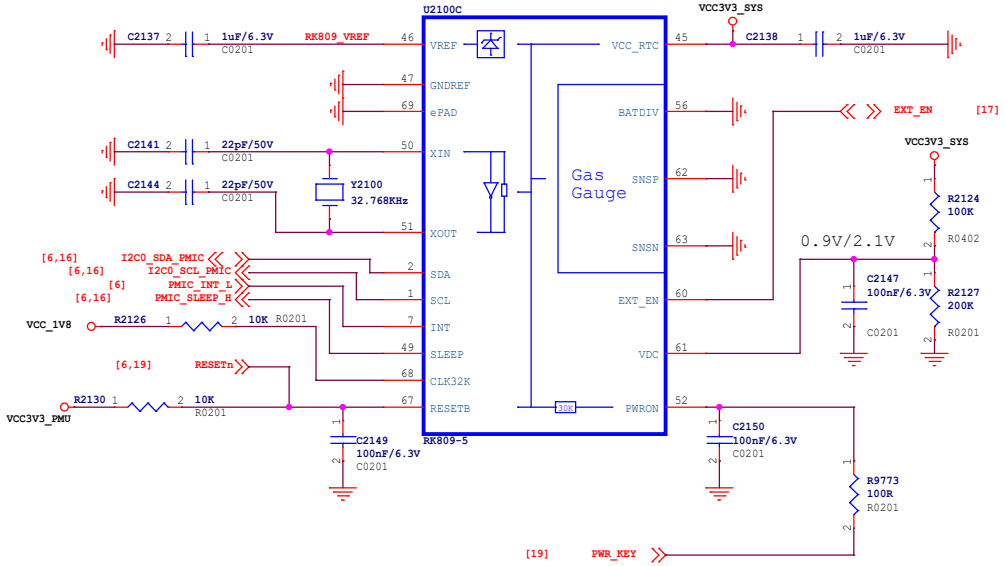


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

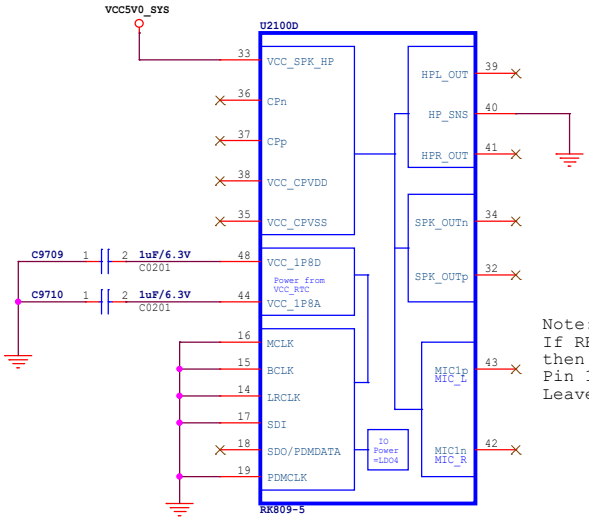
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC

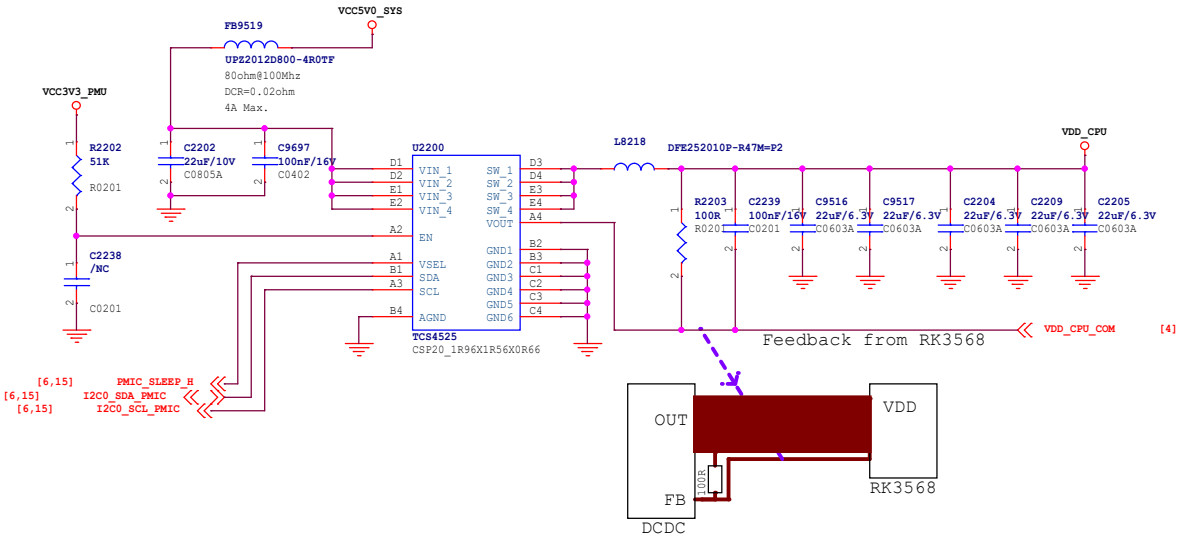


Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

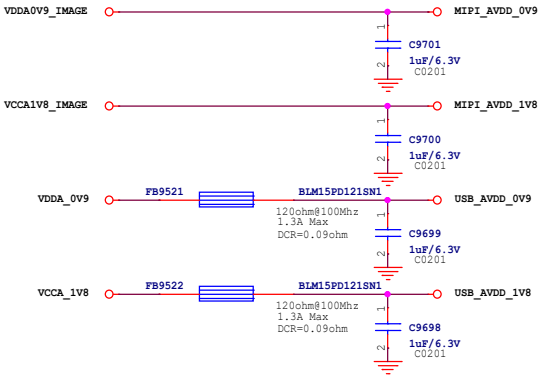
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 15.Power_PMIC
Date: Thursday, May 05, 2022	Sheet: 15/ 25

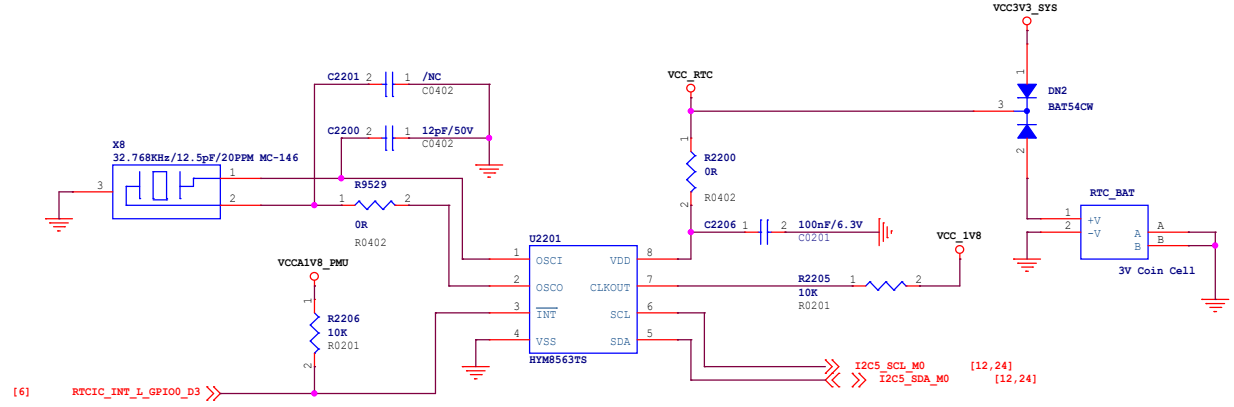
VDD_CPU



VDD_USB,VDD_MIPI

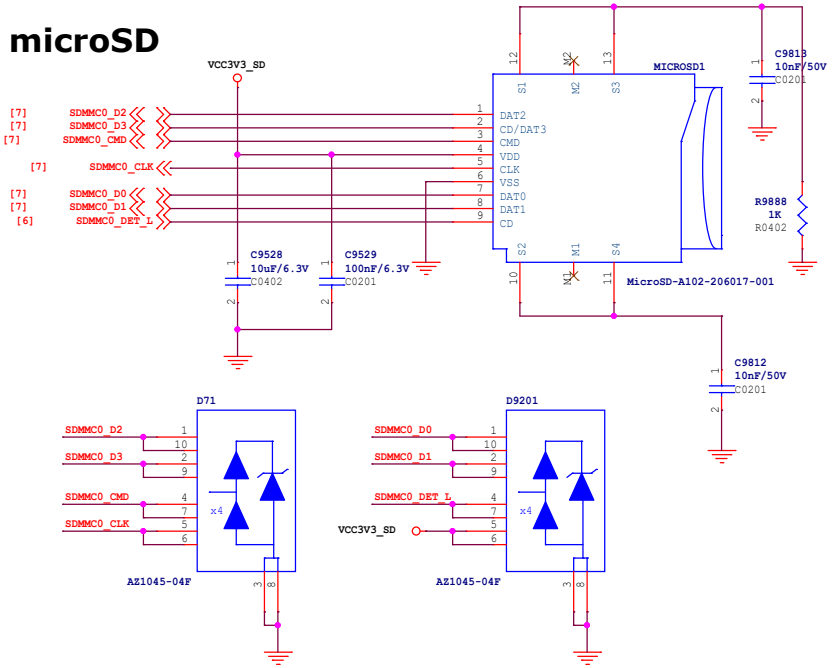


RTC



Address:Read A3H, Write A2H
7bit address: 0x51

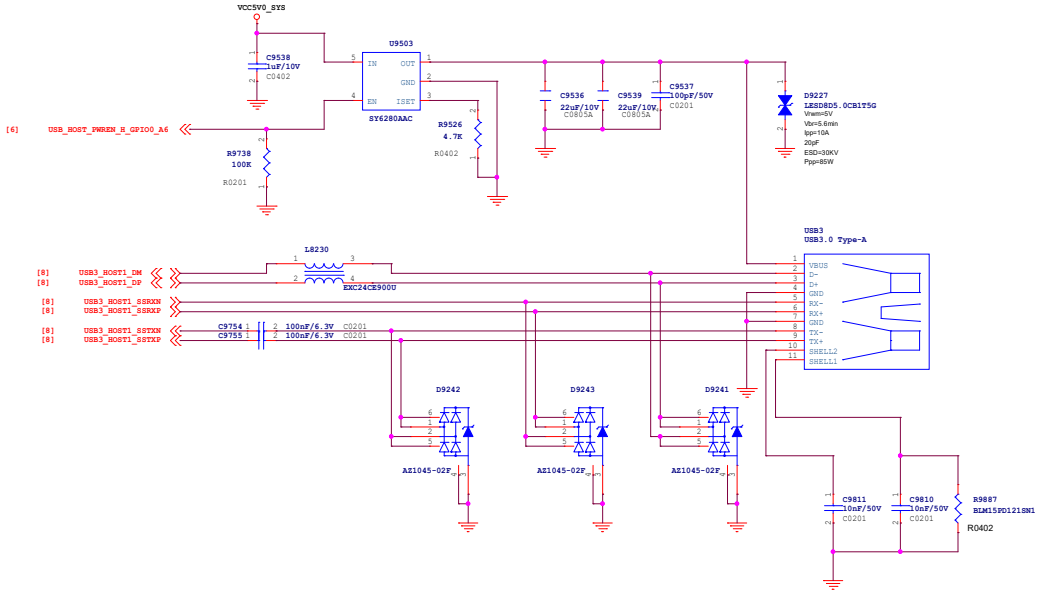
microSD



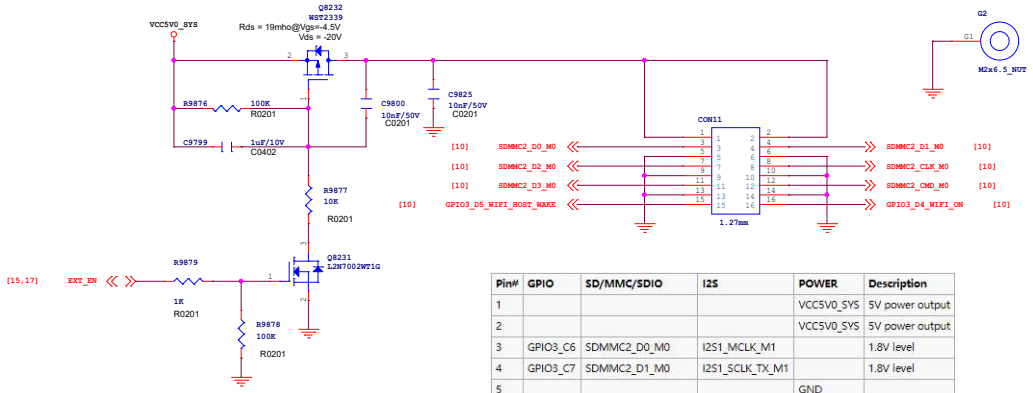
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 16.Power_other/RTC/microSD
Date: Thursday, May 05, 2022	Sheet: 16/ 25

USB 3.0

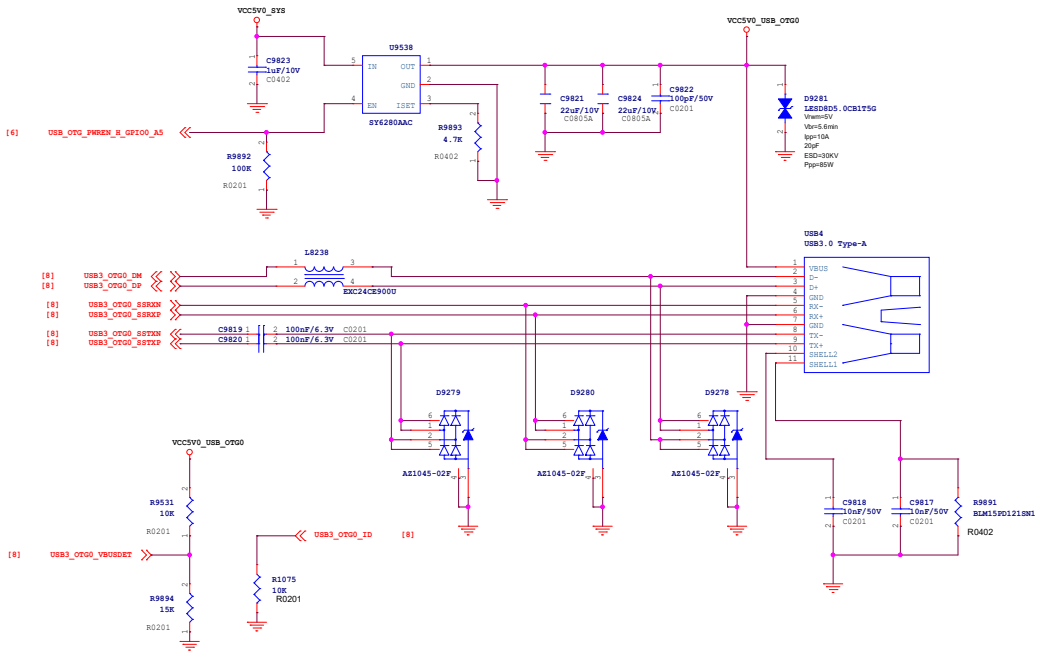


SDIO/I2S

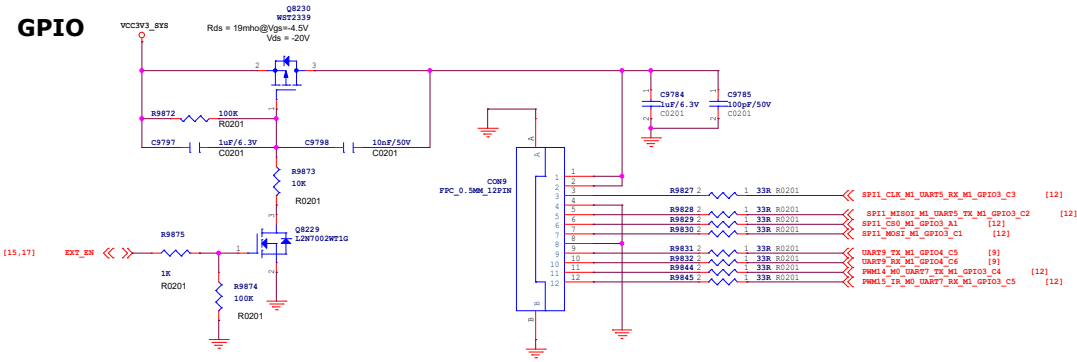


Pin#	GPIO	SD/MMC/SDIO	I2S	POWER	Description
1				VCC5V0_SYS	5V power output
2				VCC5V0_SYS	5V power output
3	GPIO3_C6	SDMMC2_D0_M0	I2S1_MCLK_M1		1.8V level
4	GPIO3_C7	SDMMC2_D1_M0	I2S1_SCLK_TX_M1		1.8V level
5				GND	
6				GND	
7	GPIO3_D0	SDMMC2_D2_M0	I2S1_LRCK_TX_M1		1.8V level
8	GPIO3_D3	SDMMC2_CLK_M0	I2S1_SDI1_M1		1.8V level
9				GND	
10				GND	
11	GPIO3_D1	SDMMC2_D3_M0	I2S1_SDO0_M1		1.8V level
12	GPIO3_D2	SDMMC2_CMD_M0	I2S1_SDI0_M1		1.8V level
13				GND	
14				GND	
15	GPIO3_D5	SDMMC2_PWREN_M0	I2S1_SDI3_M1		1.8V level
16	GPIO3_D4	SDMMC2_DET_M0	I2S1_SDI2_M1		1.8V level

USB 3.0/ADB/MASK



GPIO

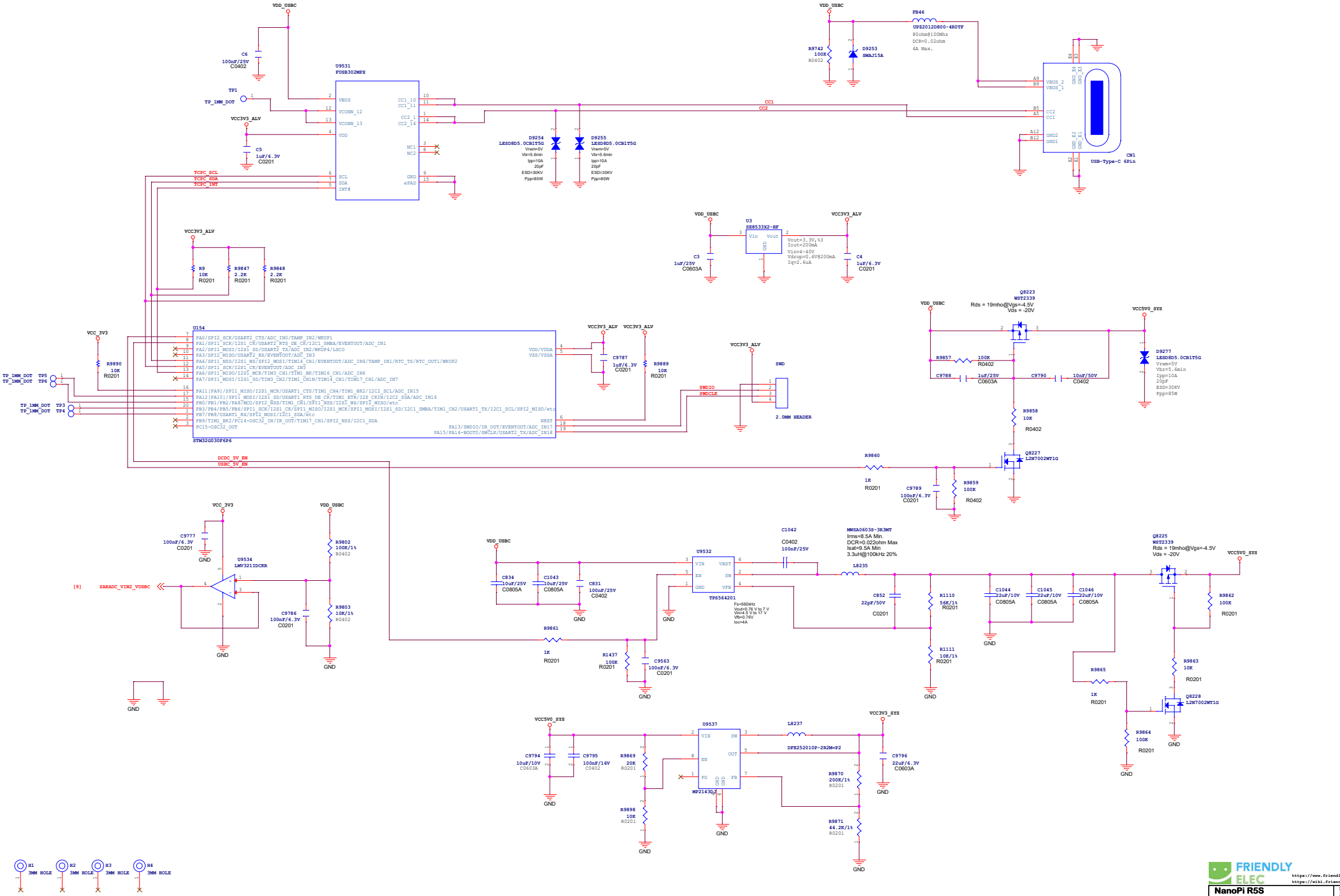


Pin#	GPIO	SPI	UART	PWM	POWER	Description
1					VCC3V3_SYS	3.3V power output
2					VCC3V3_SYS	3.3V power output
3	GPIO3_C3	SPI1_CLK_M1	UART5_RX_M1			3.3V level
4					GND	
5	GPIO3_C2	SPI1_MISOI_M1	UART5_TX_M1			3.3V level
6	GPIO3_A1	SPI1_CS0_M1				3.3V level
7	GPIO3_C1	SPI1_MOSI_M1				3.3V level
8					GND	
9	GPIO4_C5		UART9_TX_M1	PWM12_M1		3.3V level
10	GPIO4_C6		UART9_RX_M1	PWM13_M1		3.3V level
11	GPIO3_C4		UART7_TX_M1	PWM14_M0		3.3V level
12	GPIO3_C5		UART7_RX_M1	PWM15_IR_M0		3.3V level

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S		Rev 2204
Size A2	Page Name 17.USB3/SDIO/GPIO	
Date: Friday, June 10, 2022		Sheet: 17/ 25

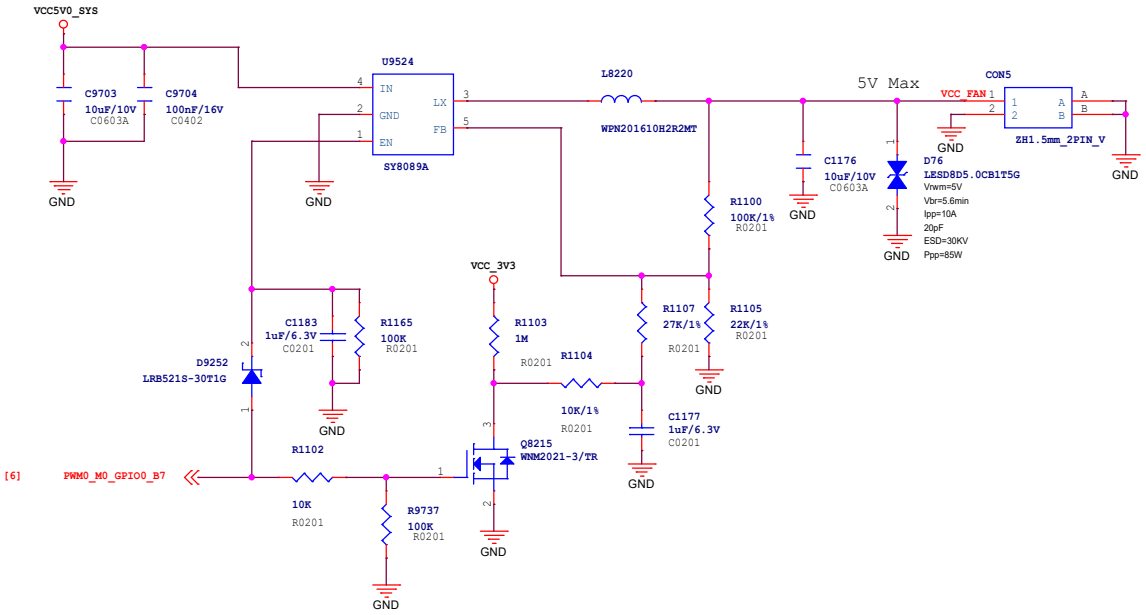
USB PD



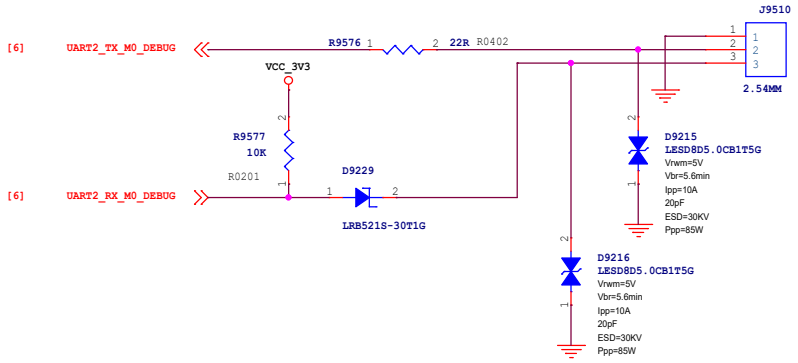
NanoPi R5S	Rev 2204
Size A2	Page Name 18.VIN/USB PD
Date: Friday, June 10, 2022	Sheet: 18/ 25

FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

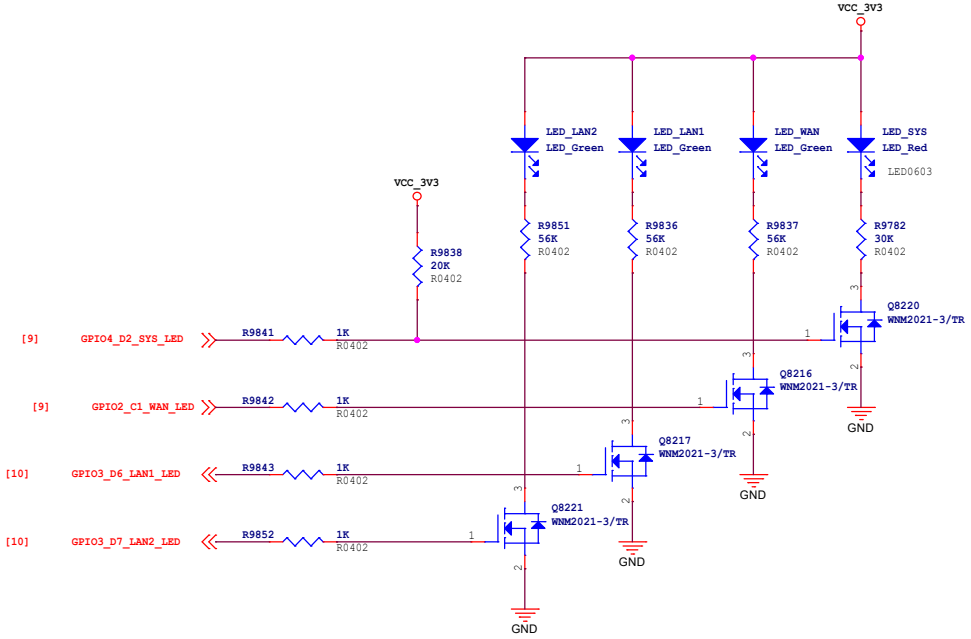
Cooling Fan



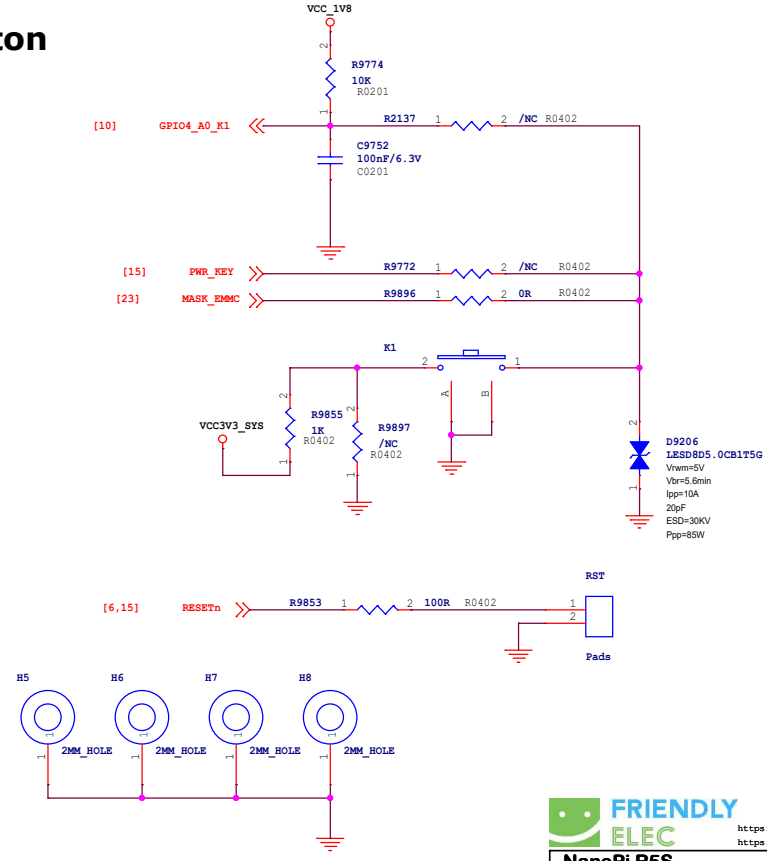
Debug UART



LED



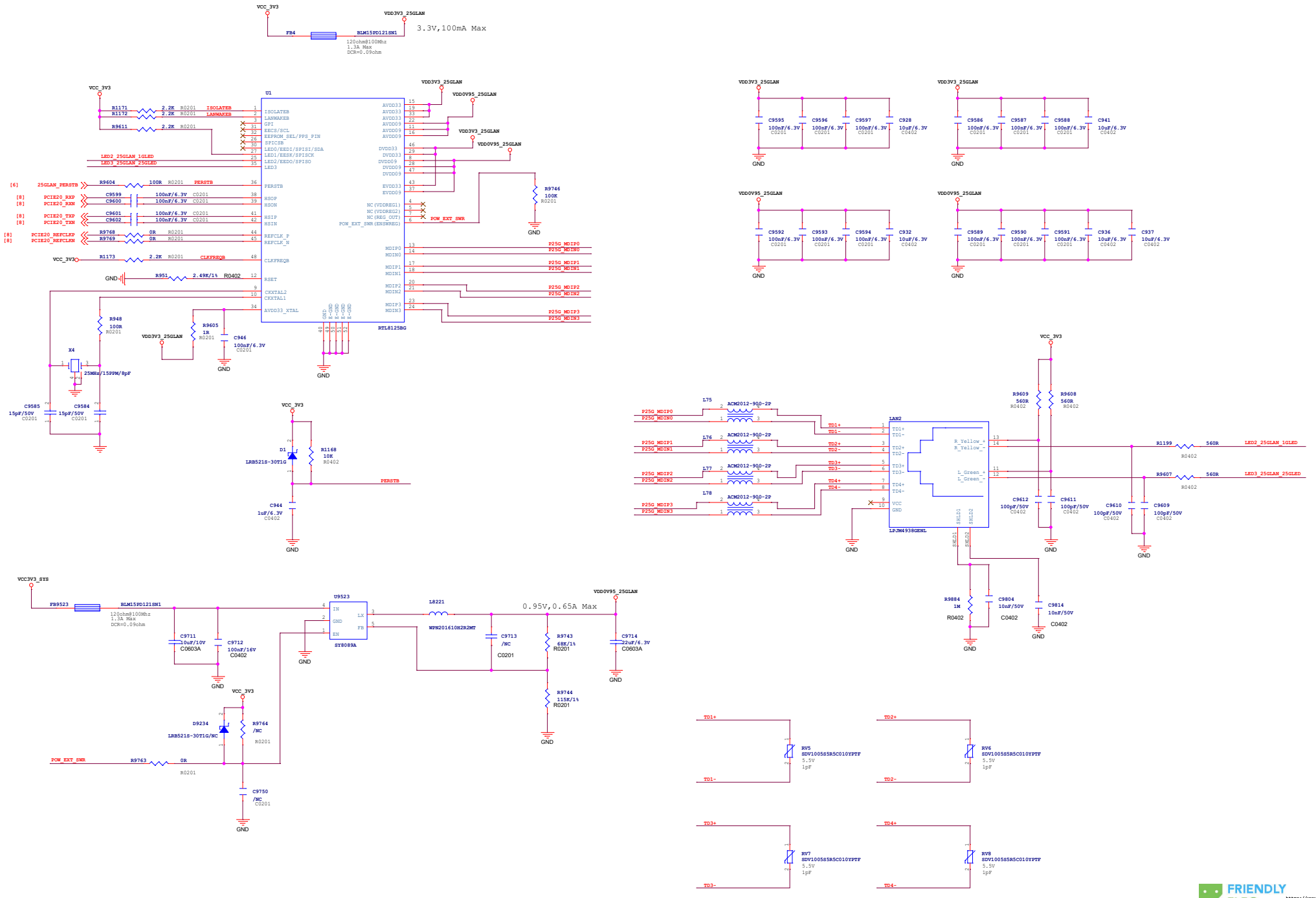
Button



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 19.Debug UART/FAN/LED/Keys
Date: Monday, May 16, 2022	Sheet: 19/ 25

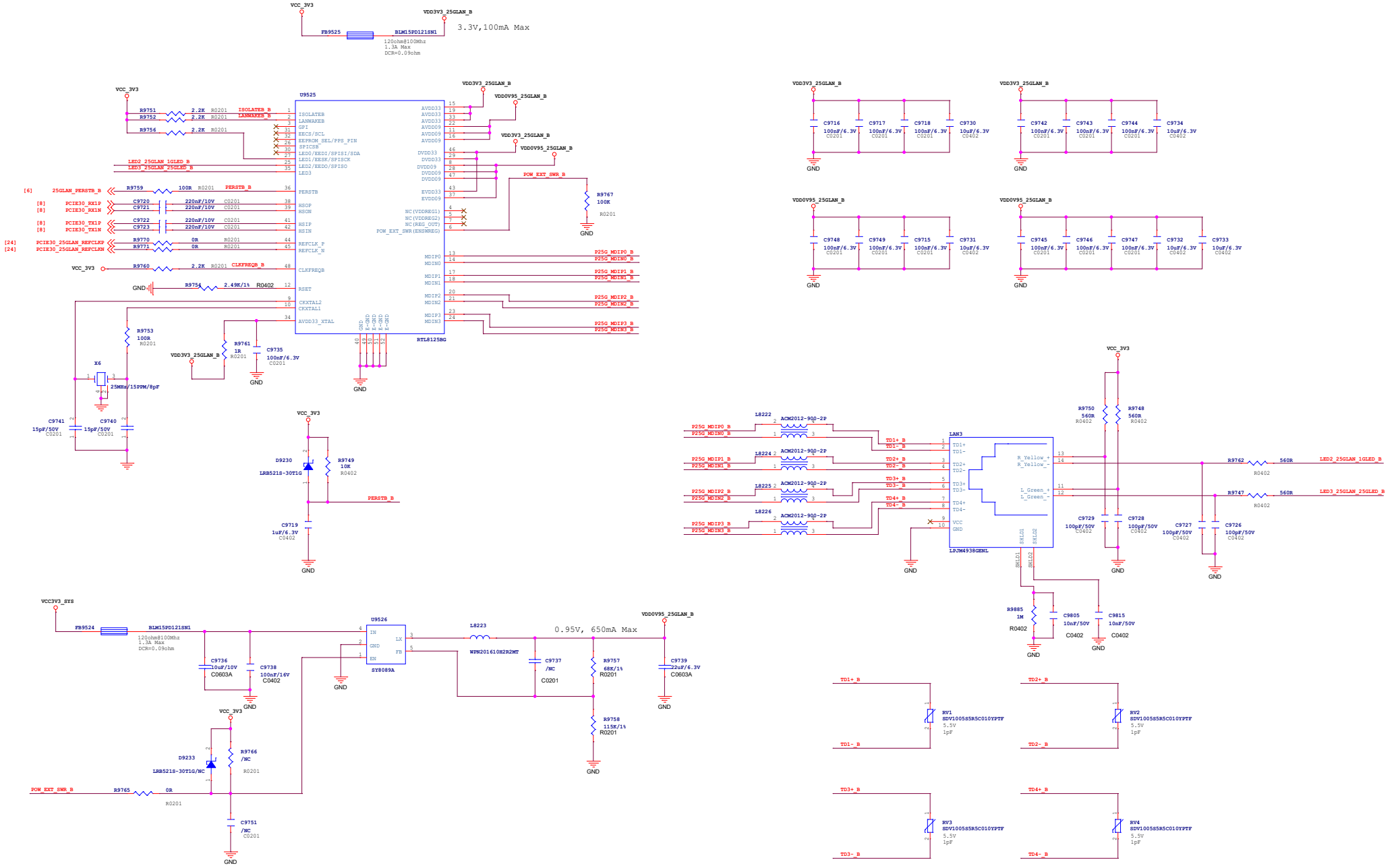
2.5Gbps Ethernet



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S		Rev 2204
Size A2	Page Name 21.Ethernet 2.5G A	
Date: Monday, May 16, 2022		Sheet: 20/ 25

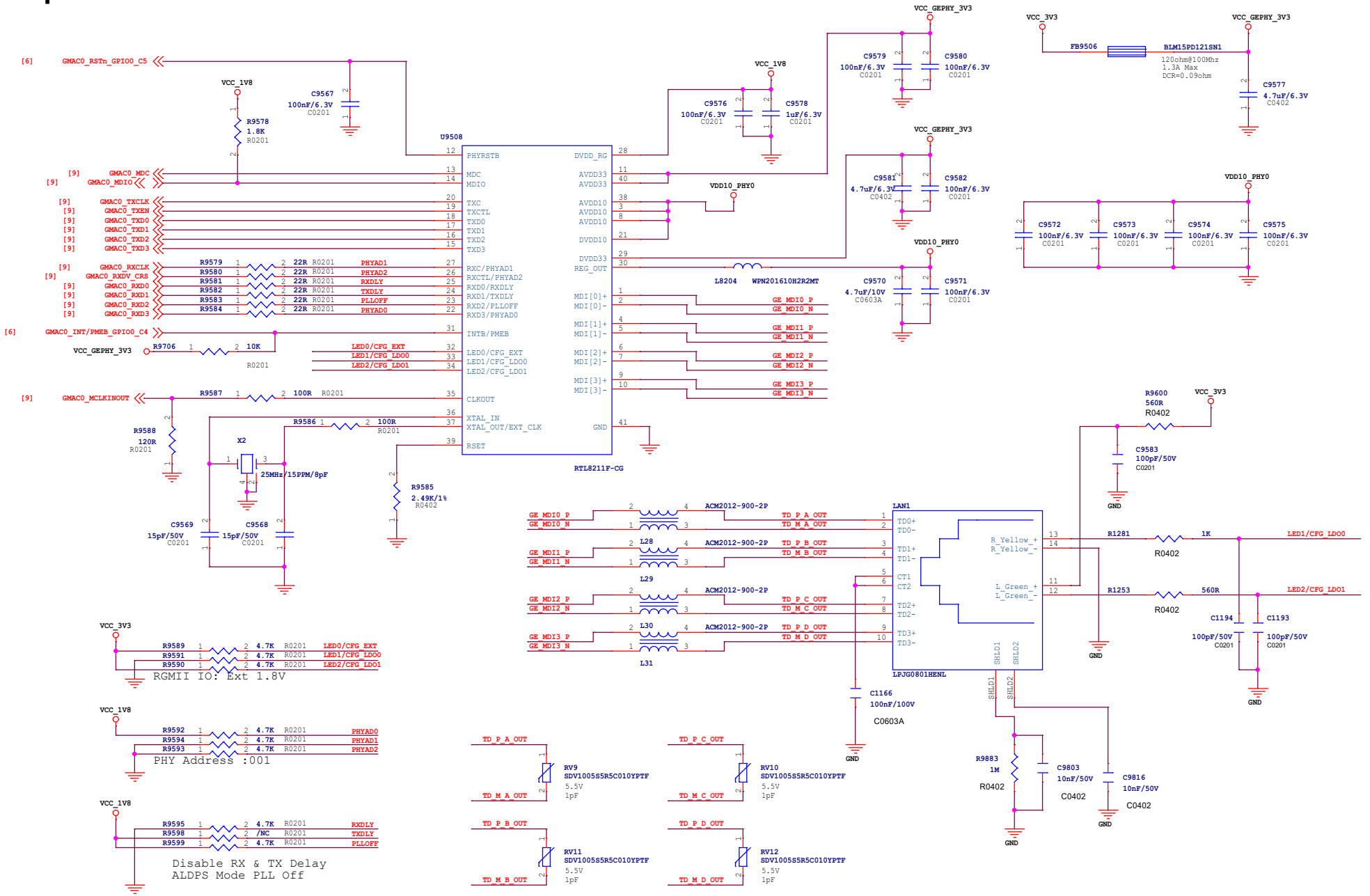
2.5Gbps Ethernet



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

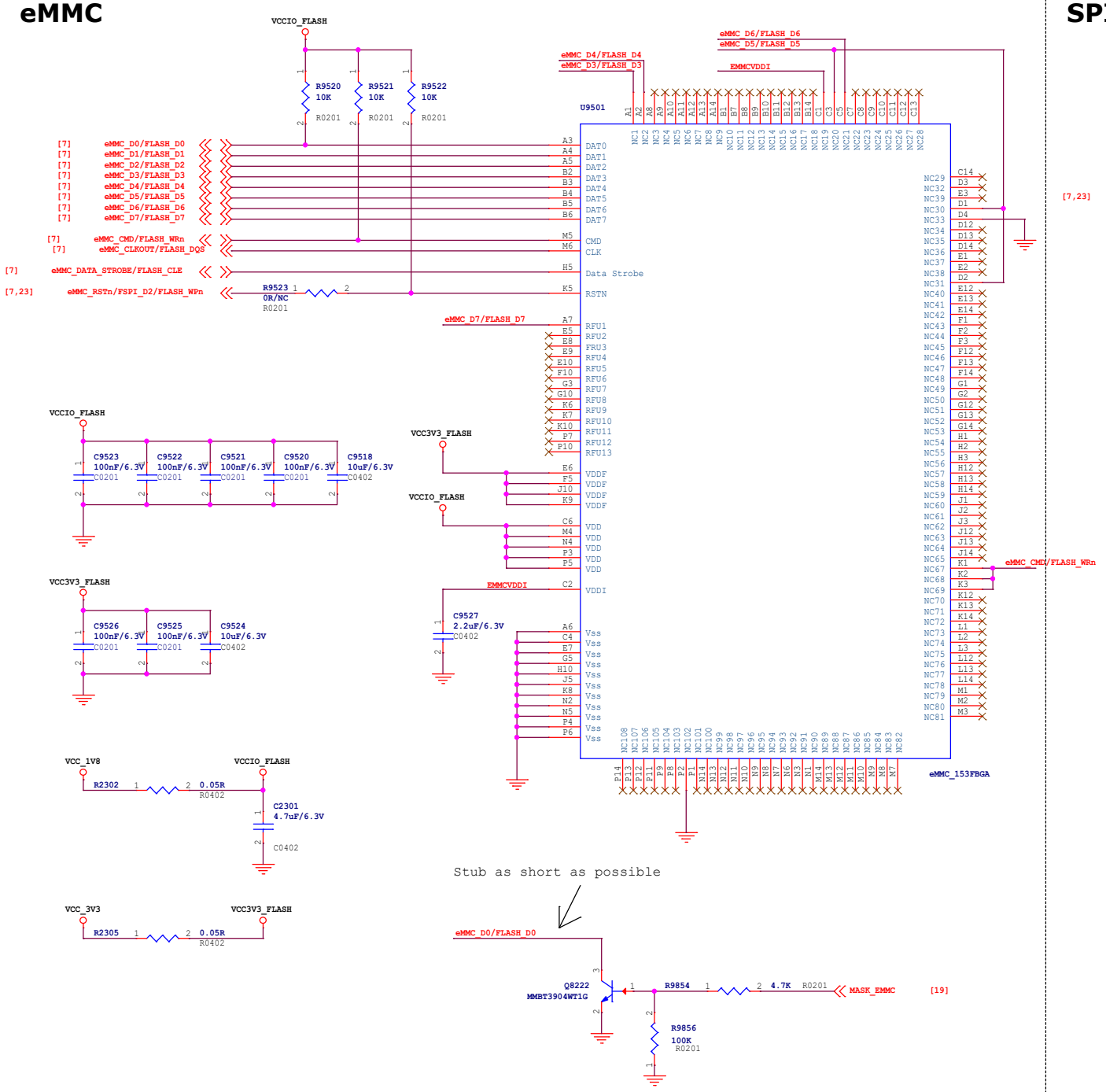
NanoPi R5S		Rev 2204
Size A2	Page Name 22.Ethernet 2.5G B	
Date: Monday, May 16, 2022		Sheet: 21/ 25

1Gbps Ethernet

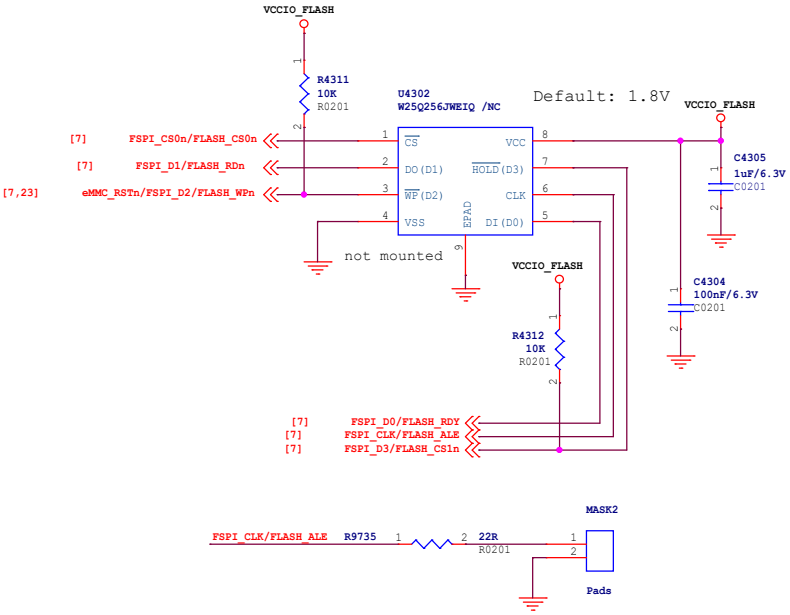


NanoPi R5S	Rev 2204
Size A3	Page Name 23.Ethernet 1G
Date: Monday, May 16, 2022	Sheet: 22/ 25

eMMC



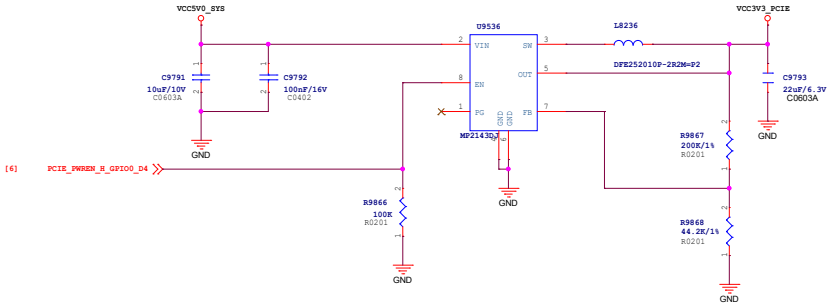
SPI Flash

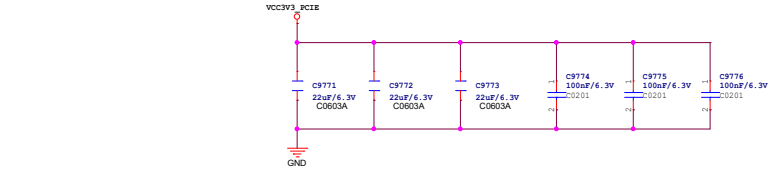


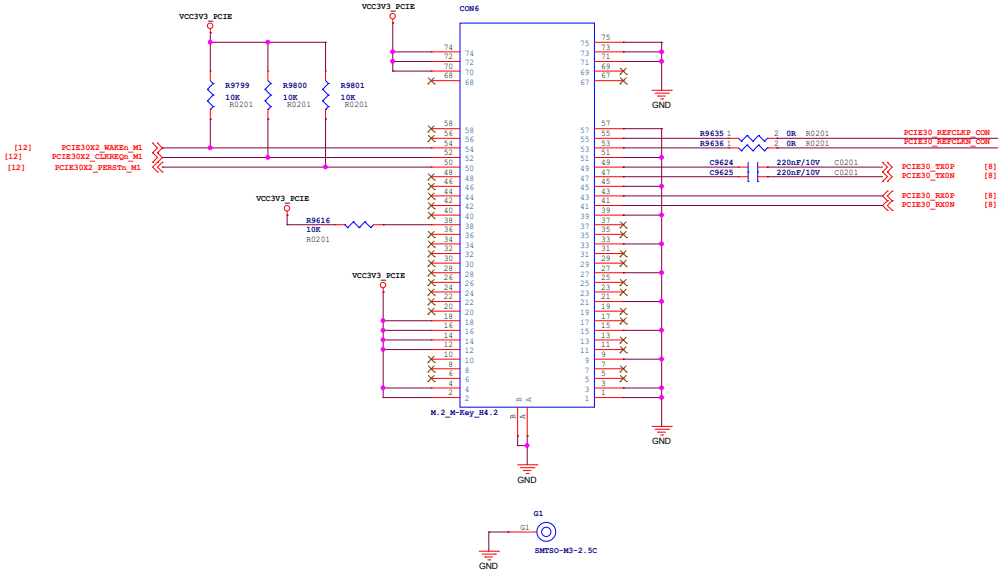
FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 24.eMMC/SPI Flash
Date: Monday, May 16, 2022	Sheet: 23/ 25

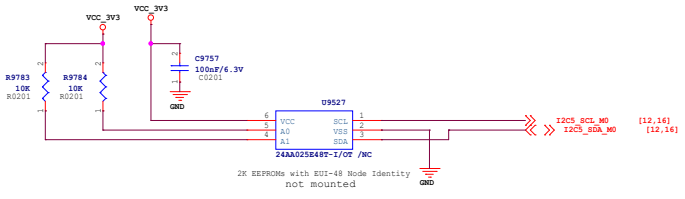
M.2 NVME



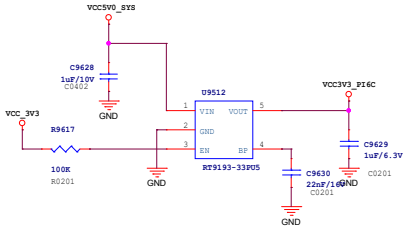


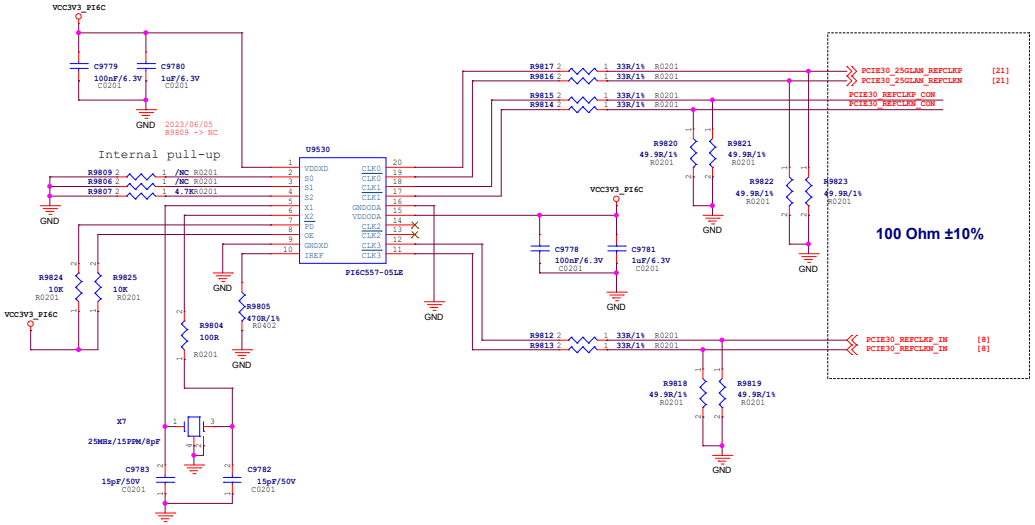


EUI-48 Node Identity



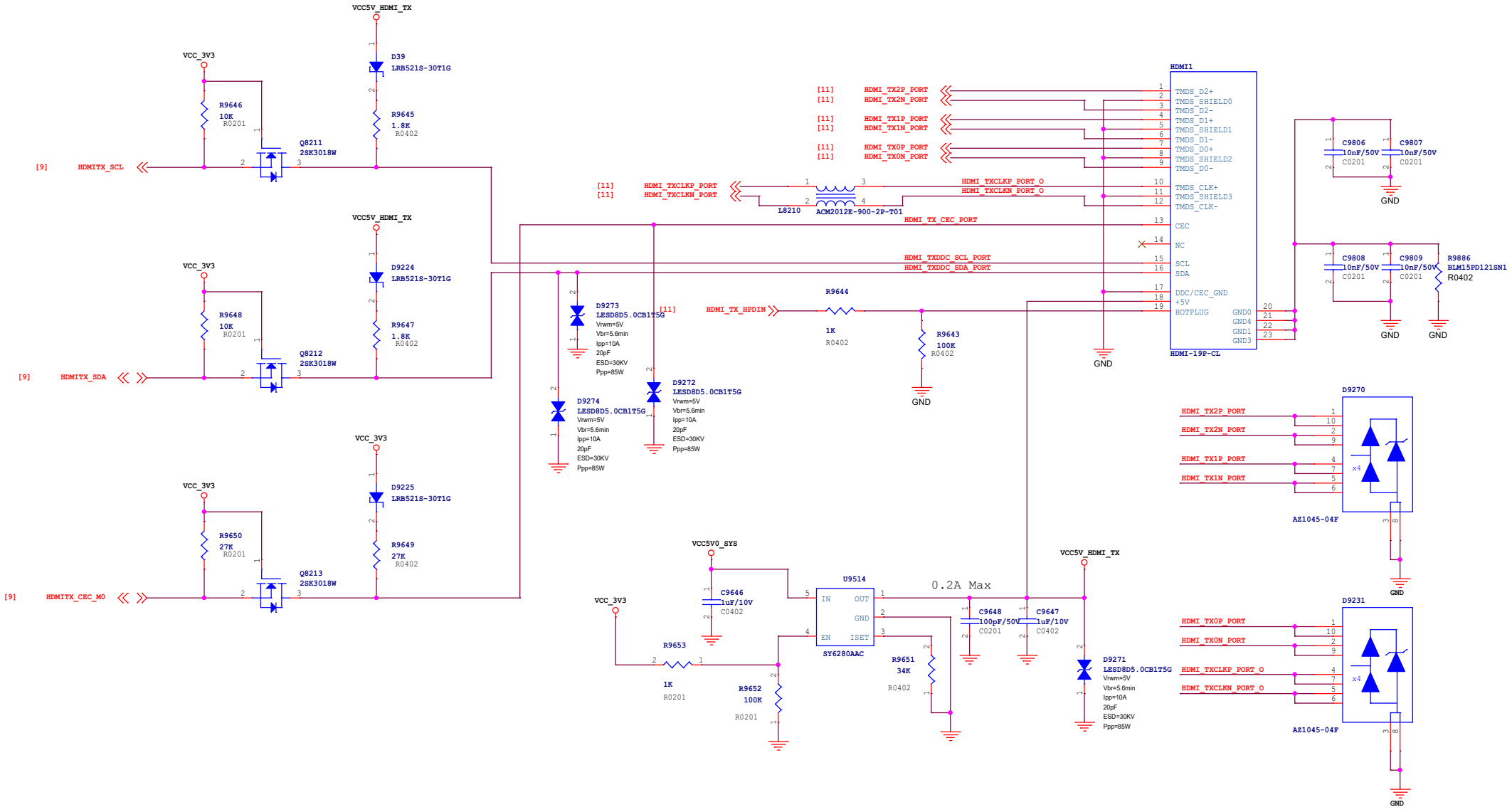
PCIe REFCLK





NanoPi R5S		Rev 2204
Size A2	Page Name 25.M.2 NVME	
Date: Monday, June 05, 2023		Sheet: 24/ 25

HDMI 2.0 TX



FRIENDLY ELEC
https://www.friendlyelec.com/
https://wiki.friendlyelec.com/

NanoPi R5S	Rev 2204
Size A3	Page Name 26.HDMI
Date: Thursday, May 05, 2022	Sheet: 25/ 25