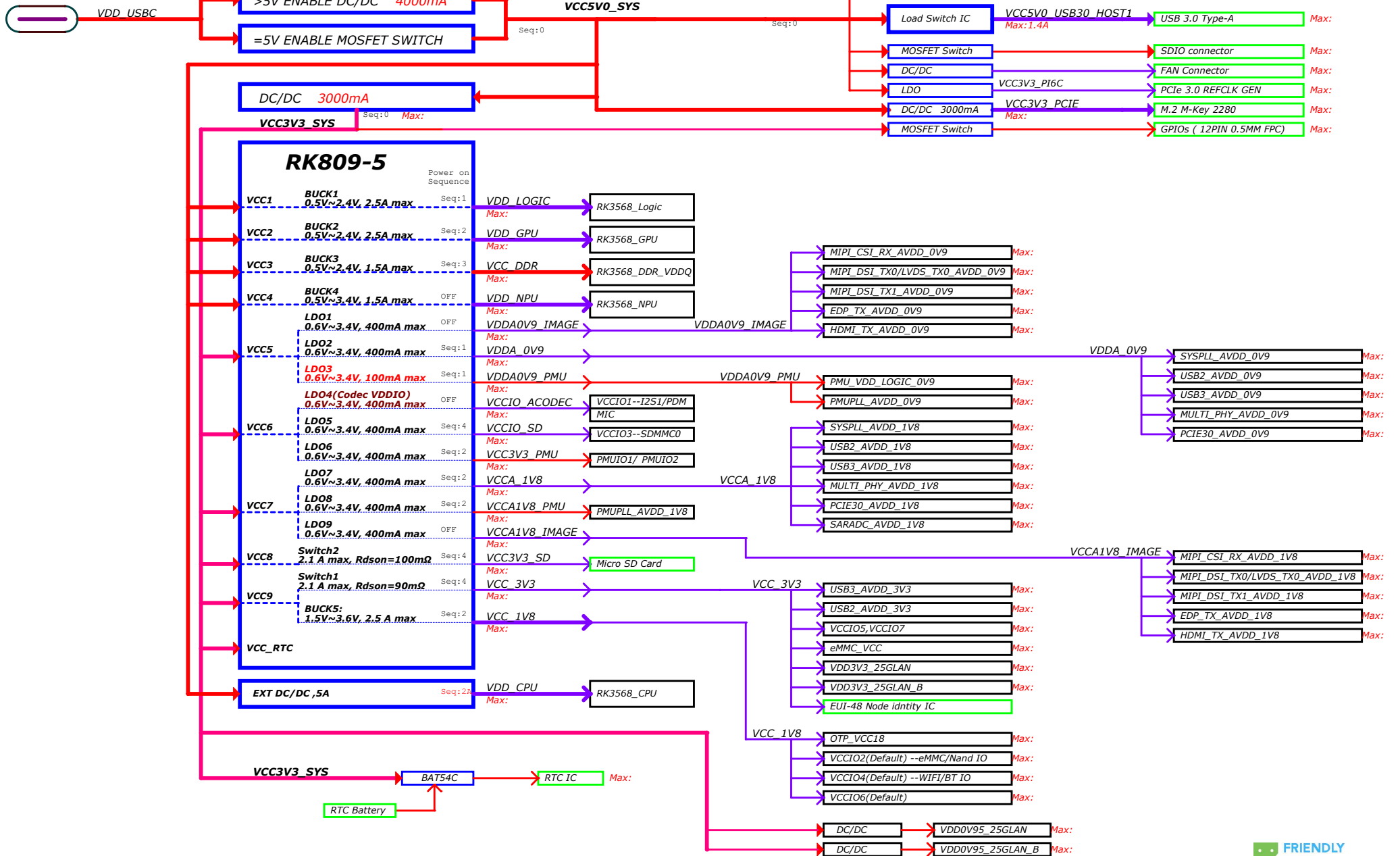
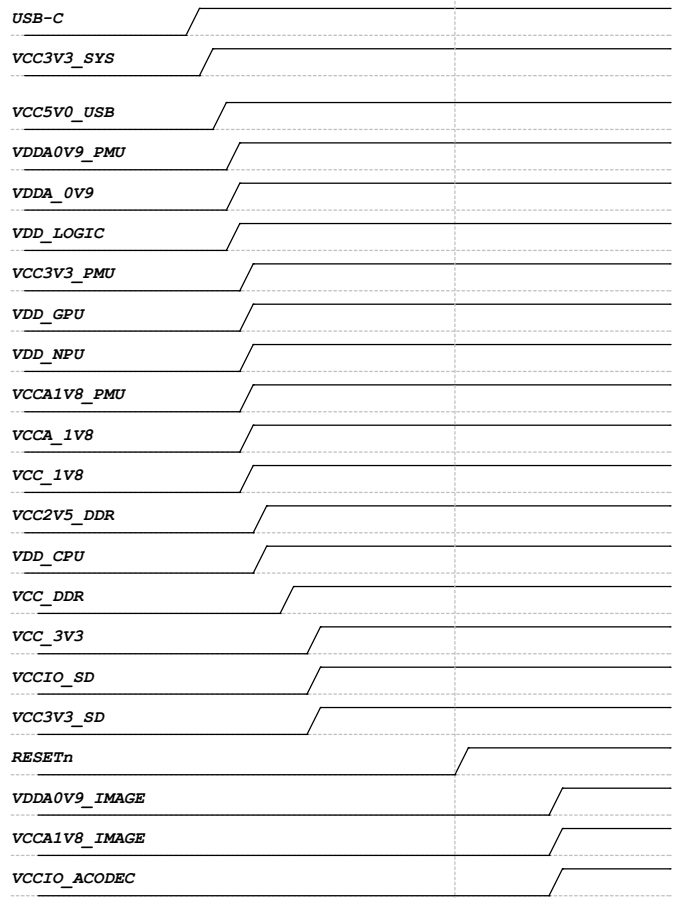


# Power Diagram

USB-C 20W MAX  
(PD 5V/9V/12V)



# Power Sequence



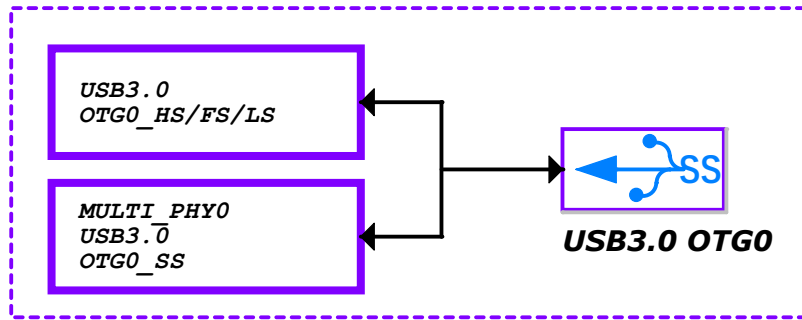
# I2C5, 7bit address  
 - 0x51, HYM8563TS, RTC IC  
 - 0x53, 24AA025E48T, EUI-48 Node Identity

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	100mohm RK809_SW1	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	90mohm RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETEn			Slot:4+5					
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VDD_USBC	EXT BUCK	4.0A	VCC3V3_SYSP	Slot:0	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD

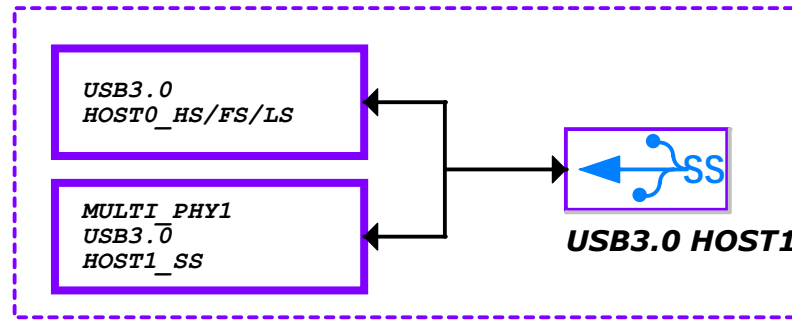
## IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V, FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

## USB3.0 OTG0



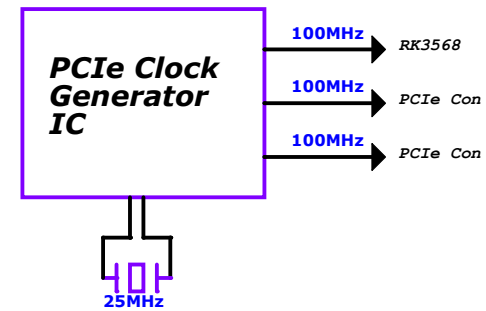
## USB3.0 HOST1



## PCIe3.0 PHY

<b>Option1</b>	<b>PCIe3.0 x2Lane</b>	PCIe30_REFCLK (RC/EP:input)	PCIe30_TX0 PCIe30_RX0 PCIe30_TX1 PCIe30_RX1	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	<b>RC or EP</b>
<b>Option2</b>	<b>PCIe3.0 x1Lane + PCIe3.0 x1Lane</b>	PCIe30_REFCLK (RC:input)	PCIe30_TX0 PCIe30_RX0	PCIe30X2_CLKREQn PCIe30X2_WAKEn PCIe30X2_PERSTn PCIe30X2_BUTTONRSTn	<b>Only RC</b>
			PCIe30_TX1 PCIe30_RX1	PCIe30X1_CLKREQn PCIe30X1_WAKEn PCIe30X1_PERSTn PCIe30X1_BUTTONRSTn	<b>Only RC</b>

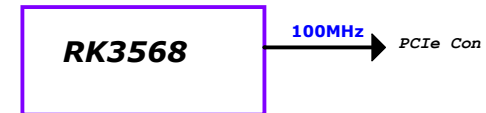
## PCIe REFCLK



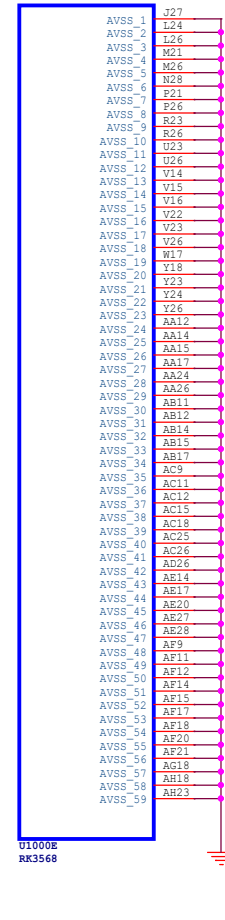
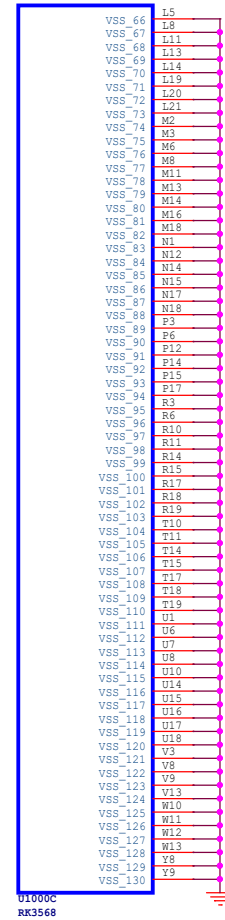
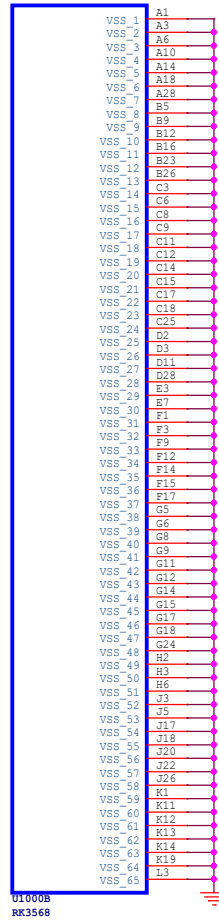
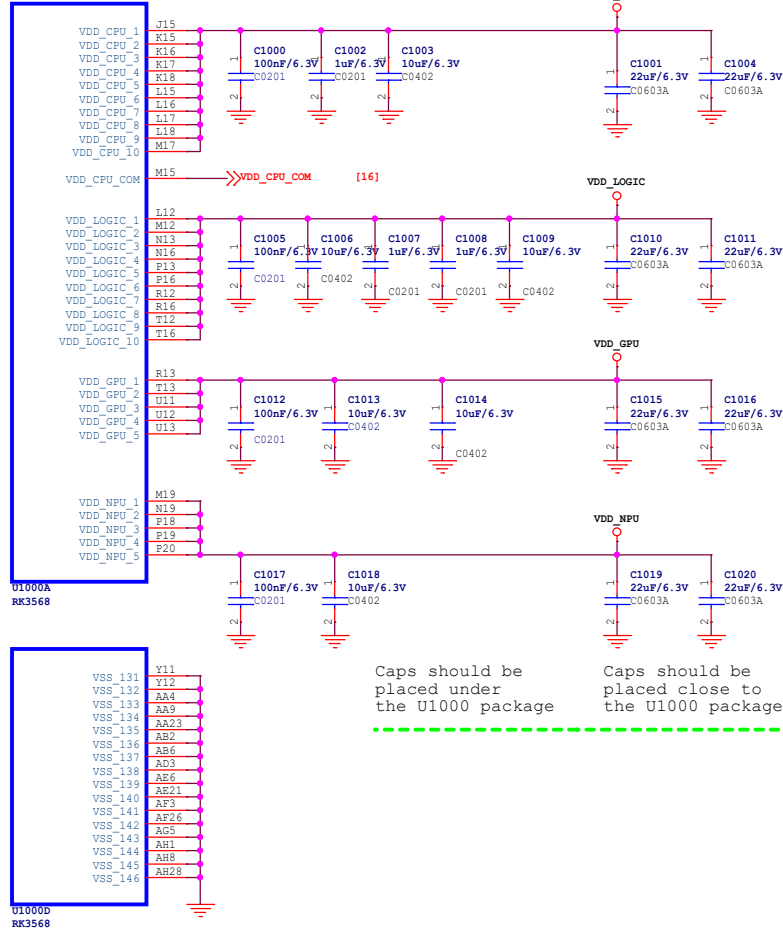
## PCIe2.0 PHY

<b>MULTI_PHY2</b>	<b>PCIe2.0 x1Lane</b>	PCIe20_REFCLK (RC:output)	PCIe20_TX PCIe20_RX	PCIe20_CLKREQn PCIe20_WAKEn PCIe20_PERSTn PCIe20_BUTTONRSTn	<b>Only RC</b>
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## PCIe2.0 REFCLK



# RK3568\_ABCDE (Power&Gnd)

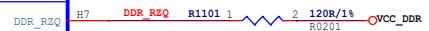


# RK3568\_F (DDR PHY)

	DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3						
[14] LPDDR4 DQ0_A	DDR DQ0 A	F2	DDR DQ0 A / DDR4 DQ0 A	LPDDR4 DQ0 A	DDR3 DQ0	LPDDR3 DQ0	DDR4 A0	LPDDR4 CLKP B	DDR3 A9	---	AC0	B6 AC0	LPDDR4 CLKP_B	[14]
[14] LPDDR4 DQ1_A	DDR DQ1 A	E1	DDR DQ1 A / DDR4 DQ1 A	LPDDR4 DQ1 A	DDR3 DQ1	LPDDR3 DQ1	DDR4 A1	---	---	---	AC1	B1 AC1	LPDDR4 A1_A	[14]
[14] LPDDR4 DQ2_A	DDR DQ2 A	E2	DDR DQ2 A / DDR4 DQ2 A	LPDDR4 DQ2 A	DDR3 DQ2	LPDDR3 DQ2	DDR4 A2	LPDDR4 CKLN B	DDR3 A7	LPDDR3 A6	AC2	F4 AC2	LPDDR4 CKLN_B	[14]
[14] LPDDR4 DQ3_A	DDR DQ3 A	D1	DDR DQ3 A / DDR4 DQ3 A	LPDDR4 DQ3 A	DDR3 DQ3	LPDDR3 DQ3	DDR4 A3	LPDDR4 CKLN A	DDR3 A7	---	AC3	F4 AC3	LPDDR4 CKLN_A	[14]
[14] LPDDR4 DQ4_A	DDR DQ4 A	J1	DDR DQ4 A / DDR4 DQ4 A	LPDDR4 DQ4 A	DDR3 DQ4	LPDDR3 DQ4	DDR4 A4	---	---	---	AC4	D9 AC4	LPDDR4 A4_A	[14]
[14] LPDDR4 DQ5_A	DDR DQ5 A	J2	DDR DQ5 A / DDR4 DQ5 A	LPDDR4 DQ5 A	DDR3 DQ5	LPDDR3 DQ5	DDR4 A5	LPDDR4 A3 B	DDR3 B1	LPDDR3 A3	AC4	D9 AC4	LPDDR4 A3_B	[14]
[14] LPDDR4 DQ6_A	DDR DQ6 A	H1	DDR DQ6 A / DDR4 DQ6 A	LPDDR4 DQ6 A	DDR3 DQ6	LPDDR3 DQ6	DDR4 A6	LPDDR4 A5 B	DDR3 A1	LPDDR3 A2	AC5	D7 AC5	LPDDR4 A5_B	[14]
[14] LPDDR4 DQ7_A	DDR DQ7 A	H4	DDR DQ7 A / DDR4 DQ7 A	LPDDR4 DQ7 A	DDR3 DQ7	LPDDR3 DQ7	DDR4 A7	LPDDR4 A1 B	DDR3 A1	LPDDR3 A1	AC6	A8 AC7	LPDDR4 A1_B	[14]
[14] LPDDR4 DQ0_B	DDR DQ0 B	B10	DDR DQ0 B / DDR4 DQ0 B	LPDDR4 DQ0 B	DDR3 DQ0	LPDDR3 DQ0	DDR4 A8	LPDDR4 ODTO CA B	DDR3 A9	---	AC7	C1 AC8	LPDDR4 ODTO_CA_B	[14]
[14] LPDDR4 DQ1_B	DDR DQ1 B	A9	DDR DQ1 B / DDR4 DQ1 B	LPDDR4 DQ1 B	DDR3 DQ1	LPDDR3 DQ1	DDR4 A9	---	---	---	AC8	A5 AC9	LPDDR4 A5_B	[14]
[14] LPDDR4 DQ2_B	DDR DQ2 B	D12	DDR DQ2 B / DDR4 DQ2 B	LPDDR4 DQ2 B	DDR3 DQ2	LPDDR3 DQ2	DDR4 A10	LPDDR4 CKLN B	DDR3 A6	LPDDR3 A9	AC8	A5 AC9	LPDDR4 CKLN_B	[14]
[14] LPDDR4 DQ3_B	DDR DQ3 B	E2	DDR DQ3 B / DDR4 DQ3 B	LPDDR4 DQ3 B	DDR3 DQ3	LPDDR3 DQ3	DDR4 A11	LPDDR4 CKLN A	DDR3 A6	---	AC9	D6 AC10	LPDDR4 CKLN_A	[14]
[14] LPDDR4 DQ4_B	DDR DQ4 B	A12	DDR DQ4 B / DDR4 DQ4 B	LPDDR4 DQ4 B	DDR3 DQ4	LPDDR3 DQ4	DDR4 A12	---	---	---	AC10	C2 AC11	LPDDR4 A0_A	[14]
[14] LPDDR4 DQ5_B	DDR DQ5 B	D15	DDR DQ5 B / DDR4 DQ5 B	LPDDR4 DQ5 B	DDR3 DQ5	LPDDR3 DQ5	DDR4 A13	LPDDR4 A3 A	DDR3 A2	---	AC11	C4 AC12	LPDDR4 A3_A	[14]
[14] LPDDR4 DQ6_B	DDR DQ6 B	E15	DDR DQ6 B / DDR4 DQ6 B	LPDDR4 DQ6 B	DDR3 DQ6	LPDDR3 DQ6	DDR4 A14	LPDDR4 A5 A	DDR3 A2	---	AC12	B8 AC13	LPDDR4 A0_B	[14]
[14] LPDDR4 DQ7_B	DDR DQ7 B	E14	DDR DQ7 B / DDR4 DQ7 B	LPDDR4 DQ7 B	DDR3 DQ7	LPDDR3 DQ7	DDR4 A15	LPDDR4 A1 A	DDR3 A1	---	AC13	C5 AC14	LPDDR4 A4_A	[14]
[14] LPDDR4 DM0_B	DDR DM0 B	D14	DDR DM0 B / DDR4 DM0 B	LPDDR4 DM0 B	DDR3 DM0	LPDDR3 DM0	DDR4 A16	LPDDR4 A2 A	DDR3 A1	---	AC14	E4 AC15	LPDDR4 A2_A	[14]
[14] LPDDR4 DQ8_B	DDR DQ8 B	B17	DDR DQ8 B / DDR4 DQ8 B	LPDDR4 DQ8 B	DDR3 DQ8	LPDDR3 DQ8	DDR4 A17	LPDDR4 A2 A	DDR3 A1	---	AC15	D5 AC16	LPDDR4 A5_A	[14]
[14] LPDDR4 DQ9_B	DDR DQ9 B	B17	DDR DQ9 B / DDR4 DQ9 B	LPDDR4 DQ9 B	DDR3 DQ9	LPDDR3 DQ9	DDR4 A18	LPDDR4 A5 A	DDR3 A1	---	AC16	E6 AC17	LPDDR4 A5_B	[14]
[14] LPDDR4 DQ10_B	DDR DQ10 B	A17	DDR DQ10 B / DDR4 DQ10 B	LPDDR4 DQ10 B	DDR3 DQ10	LPDDR3 DQ10	DDR4 A19	LPDDR4 CKLN B	DDR3 A1	---	AC17	E11 AC18	LPDDR4 A2_B	[14]
[14] LPDDR4 DQ11_B	DDR DQ11 B	B18	DDR DQ11 B / DDR4 DQ11 B	LPDDR4 DQ11 B	DDR3 DQ11	LPDDR3 DQ11	DDR4 A20	LPDDR4 CKLN A	DDR3 A1	---	AC18	E9 AC19	LPDDR4 A4_B	[14]
[14] LPDDR4 DQ12_B	DDR DQ12 B	B13	DDR DQ12 B / DDR4 DQ12 B	LPDDR4 DQ12 B	DDR3 DQ12	LPDDR3 DQ12	DDR4 A21	---	---	---	AC19	F8		
[14] LPDDR4 DQ13_B	DDR DQ13 B	A13	DDR DQ13 B / DDR4 DQ13 B	LPDDR4 DQ13 B	DDR3 DQ13	LPDDR3 DQ13	DDR4 A22	LPDDR4 ODTO CA A	DDR3 A1	---	AC20	F9		
[14] LPDDR4 DQ14_B	DDR DQ14 B	D17	DDR DQ14 B / DDR4 DQ14 B	LPDDR4 DQ14 B	DDR3 DQ14	LPDDR3 DQ14	DDR4 A23	LPDDR4 ODTO CA A	DDR3 A1	---	AC21	B3 AC22	LPDDR4 CKLN_B	[14]
[14] LPDDR4 DQ15_B	DDR DQ15 B	B14	DDR DQ15 B / DDR4 DQ15 B	LPDDR4 DQ15 B	DDR3 DQ15	LPDDR3 DQ15	DDR4 A24	LPDDR4 CKLN A	DDR3 A1	---	AC22	B3 AC22	LPDDR4 CKLN_A	[14]
[14] LPDDR4 DM1_B	DDR DM1 B	E17	DDR DM1 B / DDR4 DM1 B	LPDDR4 DM1 B	DDR3 DM1	LPDDR3 DM1	DDR4 A25	---	---	---	AC23	B4 AC23	LPDDR4 CLKP_A	[14]
[14] LPDDR4 DQ8_P	DDR DQ8 P	A16	DDR DQ8 P / DDR4 DQ8 P	LPDDR4 DQ8 P	DDR3 DQ8	LPDDR3 DQ8	DDR4 A26	LPDDR4 CLKP B	DDR3 A1	---	AC24	A4 AC24	LPDDR4 CLKP_B	[14]
[14] LPDDR4 DQ9_P	DDR DQ9 P	B17	DDR DQ9 P / DDR4 DQ9 P	LPDDR4 DQ9 P	DDR3 DQ9	LPDDR3 DQ9	DDR4 A27	---	---	---	AC25	A2 AC25	LPDDR4 CS0n_A	[14]
[14] LPDDR4 DQ10_P	DDR DQ10 P	A17	DDR DQ10 P / DDR4 DQ10 P	LPDDR4 DQ10 P	DDR3 DQ10	LPDDR3 DQ10	DDR4 A28	LPDDR4 CS1n A	DDR3 A1	---	AC26	B2 AC26	LPDDR4 CS1n_B	[14]
[14] LPDDR4 DQ11_P	DDR DQ11 P	B18	DDR DQ11 P / DDR4 DQ11 P	LPDDR4 DQ11 P	DDR3 DQ11	LPDDR3 DQ11	DDR4 A29	LPDDR4 CS1n B	DDR3 A1	---	AC27	E8 AC27	LPDDR4 CS0n_B	[14]
[14] LPDDR4 DQ12_P	DDR DQ12 P	B13	DDR DQ12 P / DDR4 DQ12 P	LPDDR4 DQ12 P	DDR3 DQ12	LPDDR3 DQ12	DDR4 A30	---	---	---	AC28	D8 AC28	LPDDR4 CS0n_B	[14]
[14] LPDDR4 DQ13_P	DDR DQ13 P	A13	DDR DQ13 P / DDR4 DQ13 P	LPDDR4 DQ13 P	DDR3 DQ13	LPDDR3 DQ13	DDR4 A31	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ14_P	DDR DQ14 P	D17	DDR DQ14 P / DDR4 DQ14 P	LPDDR4 DQ14 P	DDR3 DQ14	LPDDR3 DQ14	DDR4 A32	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ15_P	DDR DQ15 P	B14	DDR DQ15 P / DDR4 DQ15 P	LPDDR4 DQ15 P	DDR3 DQ15	LPDDR3 DQ15	DDR4 A33	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ8_N	DDR DQ8 N	M4	DDR DQ8 N / DDR4 DQ8 N	LPDDR4 DQ8 N	DDR3 DQ8	LPDDR3 DQ8	DDR4 A34	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ9_N	DDR DQ9 N	M5	DDR DQ9 N / DDR4 DQ9 N	LPDDR4 DQ9 N	DDR3 DQ9	LPDDR3 DQ9	DDR4 A35	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ10_N	DDR DQ10 N	R5	DDR DQ10 N / DDR4 DQ10 N	LPDDR4 DQ10 N	DDR3 DQ10	LPDDR3 DQ10	DDR4 A36	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ11_N	DDR DQ11 N	M7	DDR DQ11 N / DDR4 DQ11 N	LPDDR4 DQ11 N	DDR3 DQ11	LPDDR3 DQ11	DDR4 A37	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ12_N	DDR DQ12 N	E7	DDR DQ12 N / DDR4 DQ12 N	LPDDR4 DQ12 N	DDR3 DQ12	LPDDR3 DQ12	DDR4 A38	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ13_N	DDR DQ13 N	R4	DDR DQ13 N / DDR4 DQ13 N	LPDDR4 DQ13 N	DDR3 DQ13	LPDDR3 DQ13	DDR4 A39	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ14_N	DDR DQ14 N	E4	DDR DQ14 N / DDR4 DQ14 N	LPDDR4 DQ14 N	DDR3 DQ14	LPDDR3 DQ14	DDR4 A40	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ15_N	DDR DQ15 N	R4	DDR DQ15 N / DDR4 DQ15 N	LPDDR4 DQ15 N	DDR3 DQ15	LPDDR3 DQ15	DDR4 A41	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DM0_P	DDR DM0 P	P5	DDR DM0 P / DDR4 DM0 P	LPDDR4 DM0 P	DDR3 DM0	LPDDR3 DM0	DDR4 A42	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DM0_N	DDR DM0 N	M4	DDR DM0 N / DDR4 DM0 N	LPDDR4 DM0 N	DDR3 DM0	LPDDR3 DM0	DDR4 A43	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ8_P	DDR DQ8 P	E2	DDR DQ8 P / DDR4 DQ8 P	LPDDR4 DQ8 P	DDR3 DQ8	LPDDR3 DQ8	DDR4 A44	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]
[14] LPDDR4 DQ9_P	DDR DQ9 P	E1	DDR DQ9 P / DDR4 DQ9 P	LPDDR4 DQ9 P	DDR3 DQ9	LPDDR3 DQ9	DDR4 A45	---	---	---	AC29	F11 AC29	LPDDR4 RESETn	[14]

Note: Sequences can not be swap

Note: Except DDR3, other DQ sequences can not be swap

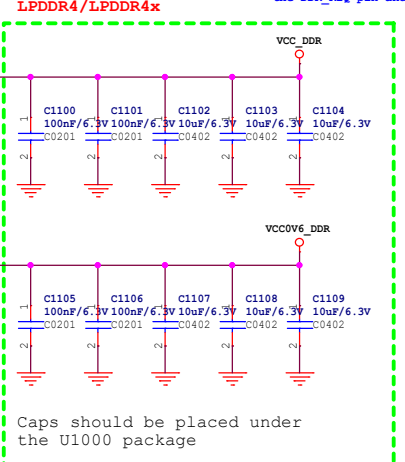


For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR\_RQ pin and VSS pin



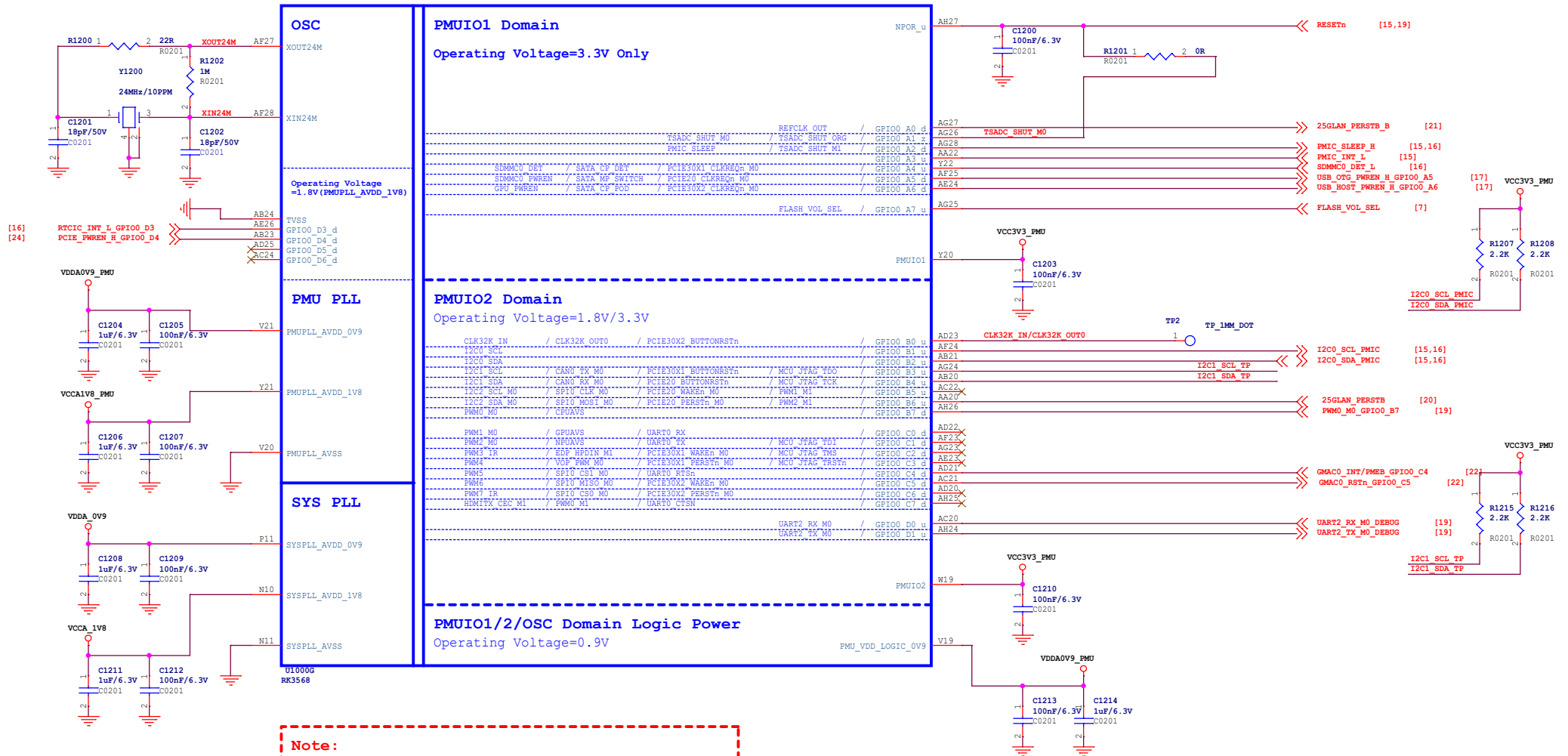
For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR\_RQ pin and DDRPHY\_VDDQ pin

DDR3L = 1.35V	DDRPHY_VDDQ_1	H9
DDR3 = 1.5V	DDRPHY_VDDQ_2	H12
DDR4 = 1.2V	DDRPHY_VDDQ_3	H14
LPDDR3 = 1.2V	DDRPHY_VDDQ_4	H15
LPDDR4 = 1.1V	DDRPHY_VDDQ_5	L9
LPDDR4x = 1.1V	DDRPHY_VDDQ_6	L8
	DDRPHY_VDDQ_7	M9
	DDRPHY_VDDQ_8	M9
	DDRPHY_VDDQ_9	J11
	DDRPHY_VDDQ_10	J12
	DDRPHY_VDDQ_11	J14
	DDRPHY_VDDQ_12	J10
	DDRPHY_VDDQ_13	L10
	DDRPHY_VDDQ_14	M10
	DDRPHY_VDDQ_15	M10
	DDRPHY_VDDQ_16	M10



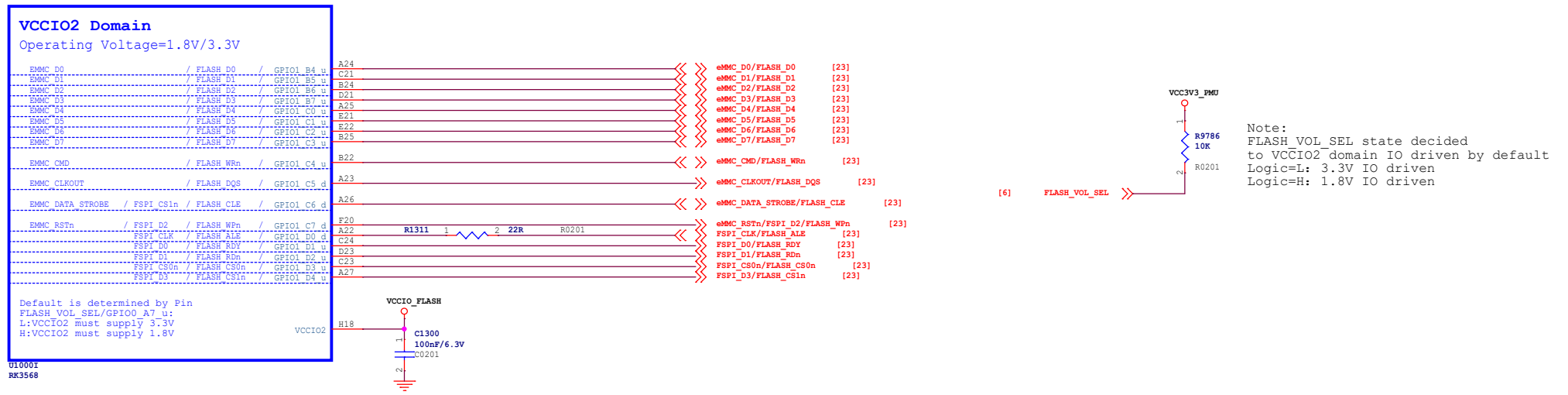
Caps should be placed under the U1000 package

# RK3568\_G (OSC/PLL/PMUIO1/2)

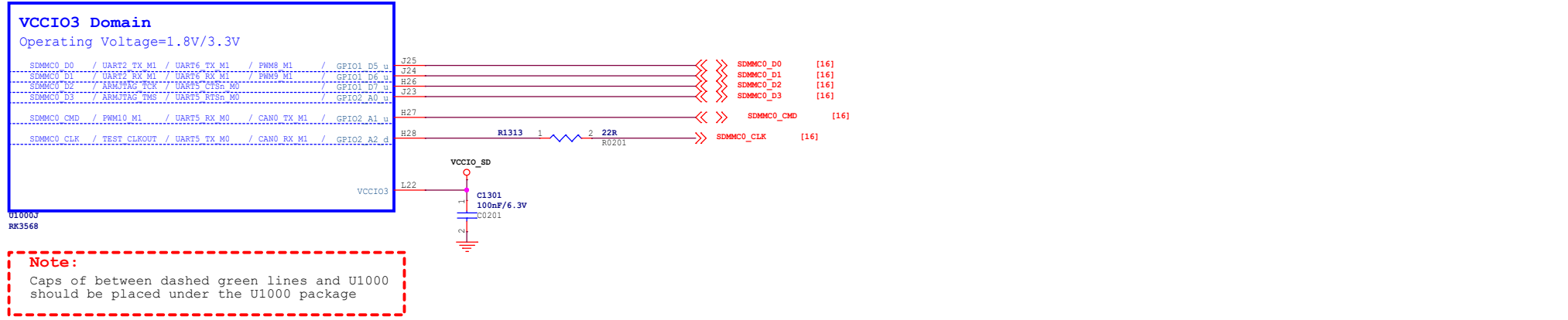


**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

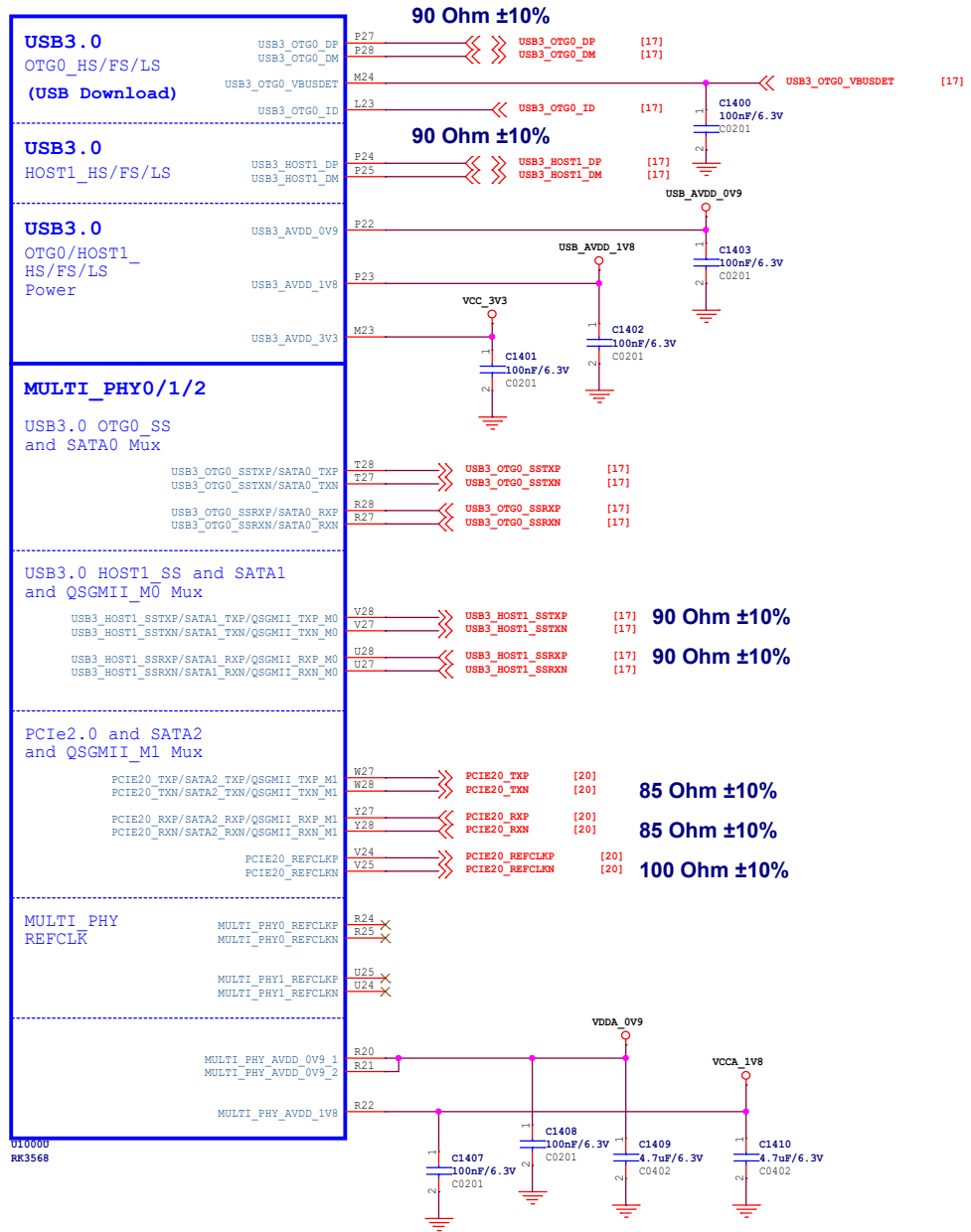
# RK3568\_I (VCCIO2 Domain)



# RK3568\_J (VCCIO3 Domain)

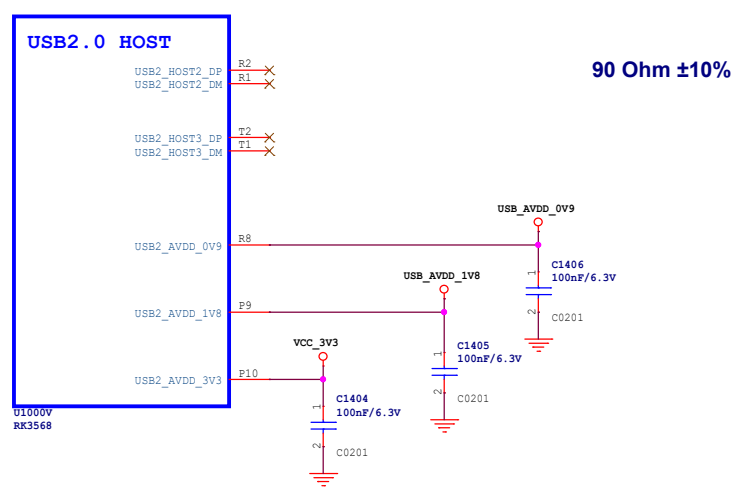


# RK3568\_U (USB3.0/SATA/QSGMII/PCIE2.0 x1)

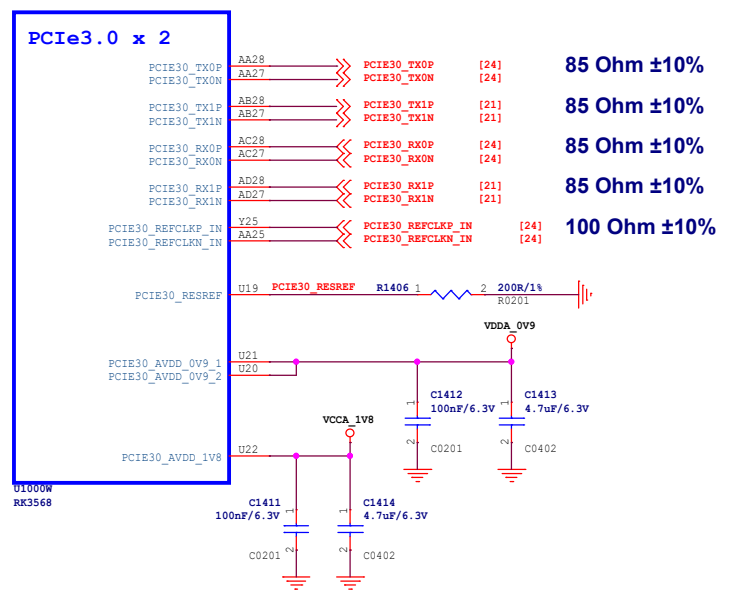


**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

# RK3568\_V (USB2.0 HOST)



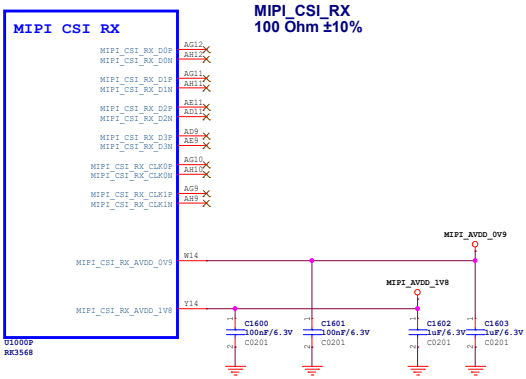
# RK3568\_W (PCIE3.0 x2)





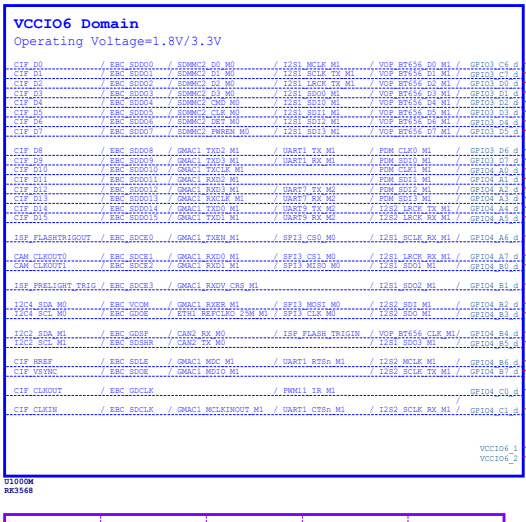


# RK3568\_P(MIPI\_CSI\_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

# RK3568\_M(VCCIO6 Domain)

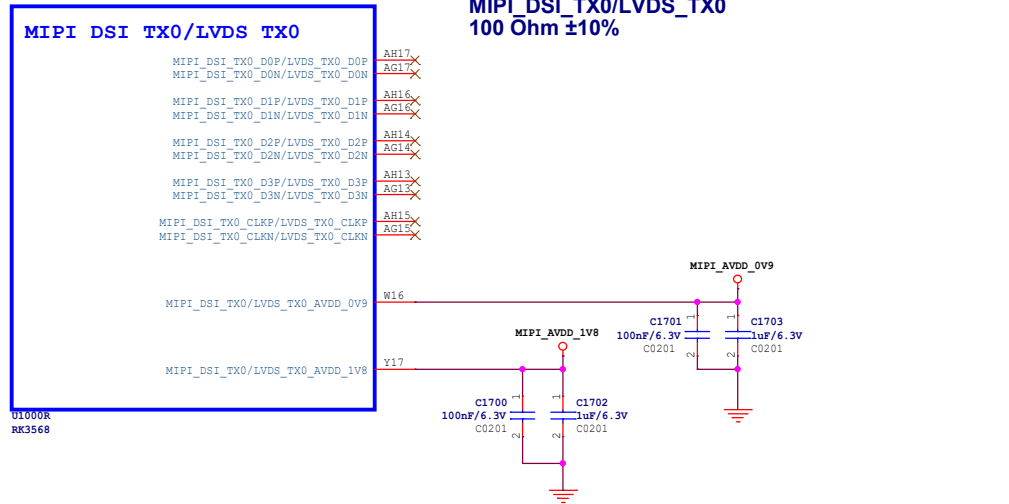


Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

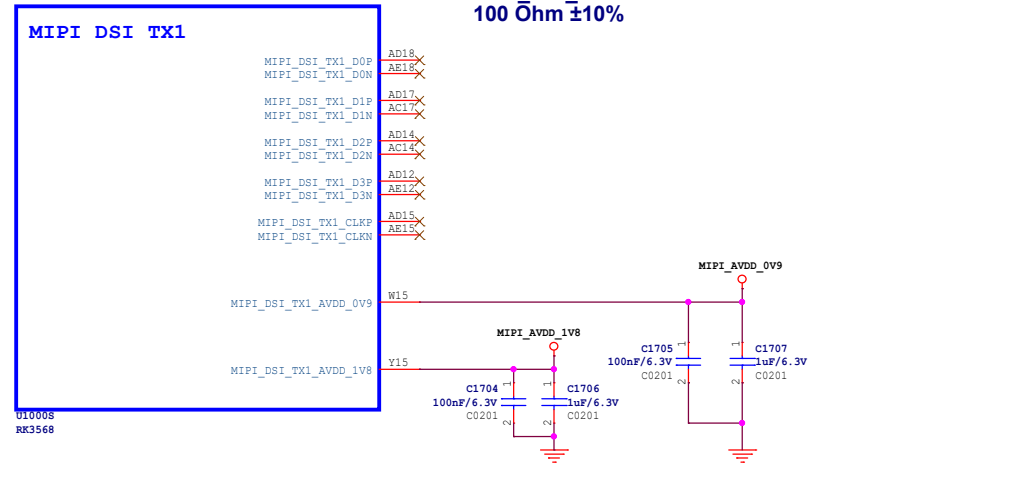
Support BF601 YCbCr 422 8bit input  
Support BF656 YCbCr 422 8bit input  
Support RAW 8/10/12bit input  
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling  
Support 2/4 mixed BF656/BT1120 YCbCr 422 8bit input

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

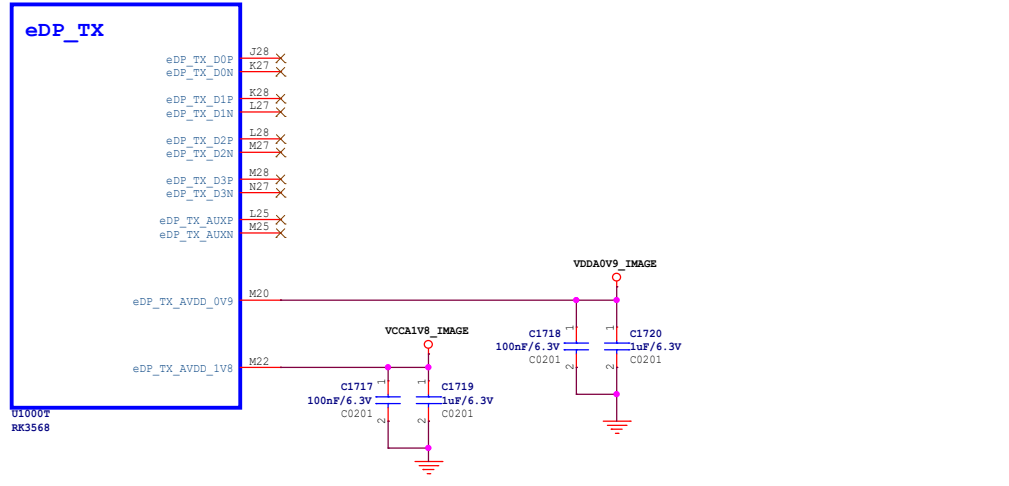
# RK3568\_R (MIPI\_DSI\_TX0/LVDS\_TX0)



# RK3568\_S (MIPI\_DSI\_TX1)

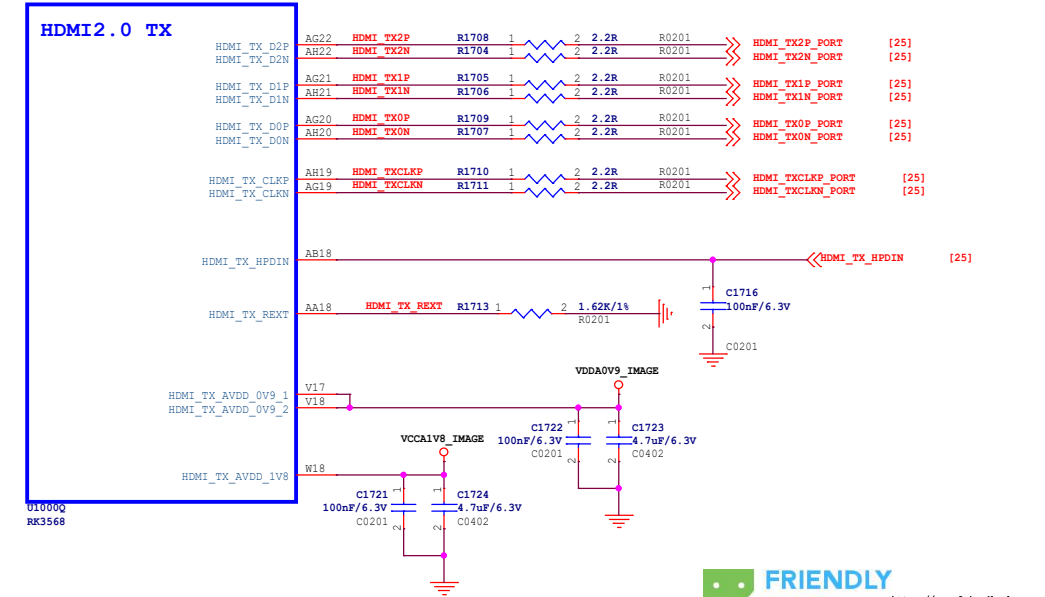


# RK3568\_T (eDP TX)



**Note:**  
 Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package

# RK3568\_Q (HDMI2.0 TX)



**HDMI TMSD trace**  
 100 Ohm ±10%

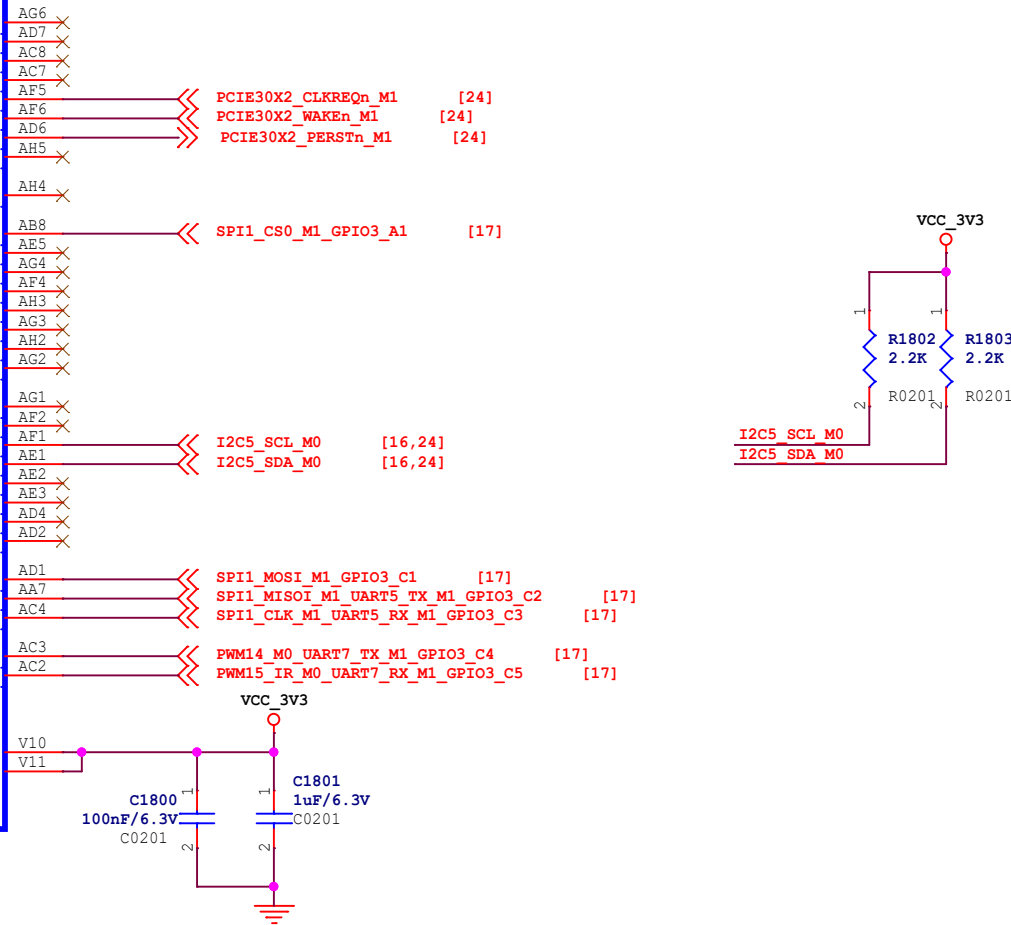
# RK3568\_L (VCCIO5 Domain)

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREOn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREOn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREOn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERStn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERStn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0	/ SDMMC2 DET M1	/ GPIO3 A7 d	
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0	/ SDMMC2 PWREN M1	/ GPIO3 B0 d	
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERStn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

VCCIO5\_1  
VCCIO5\_2



U1000L  
RK3568

### Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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<https://wiki.friendlyelec.com/>

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Size A4	Page Name 12.RK3568_VO Interface_2	
Date: Thursday, May 05, 2022	Sheet: 12/ 25	

# RK3568\_H (VCCIO1 Domain)

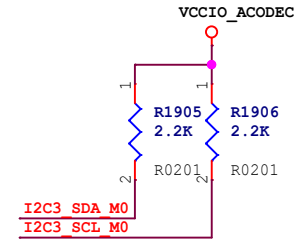
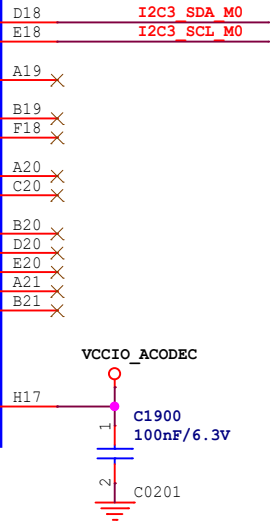
## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

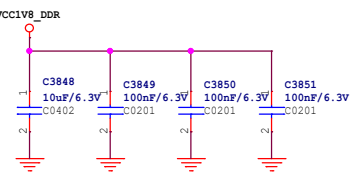
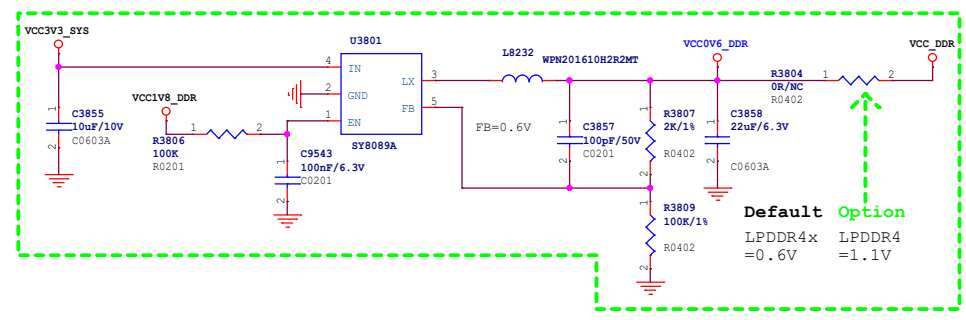
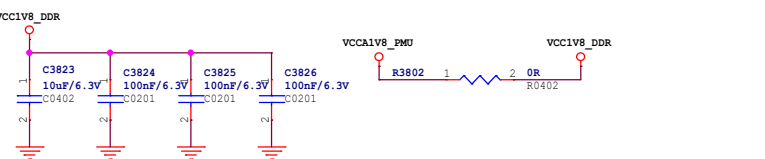
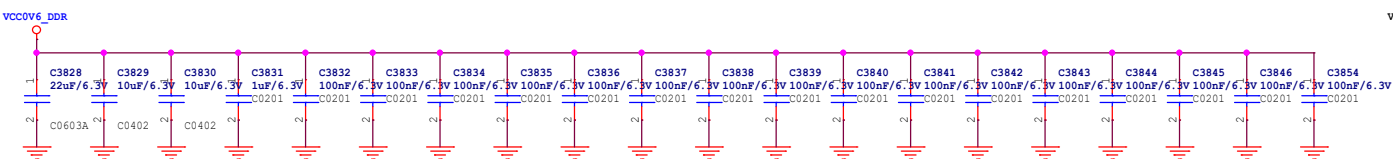
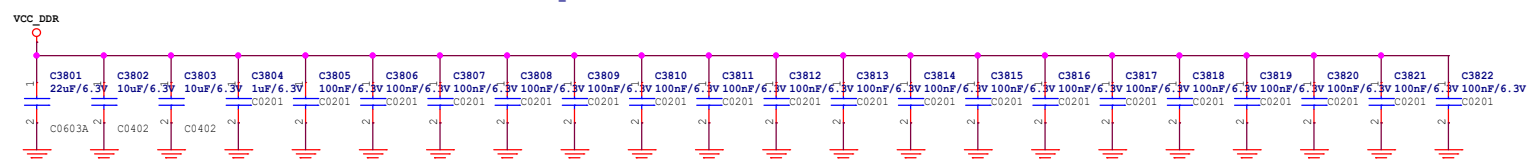
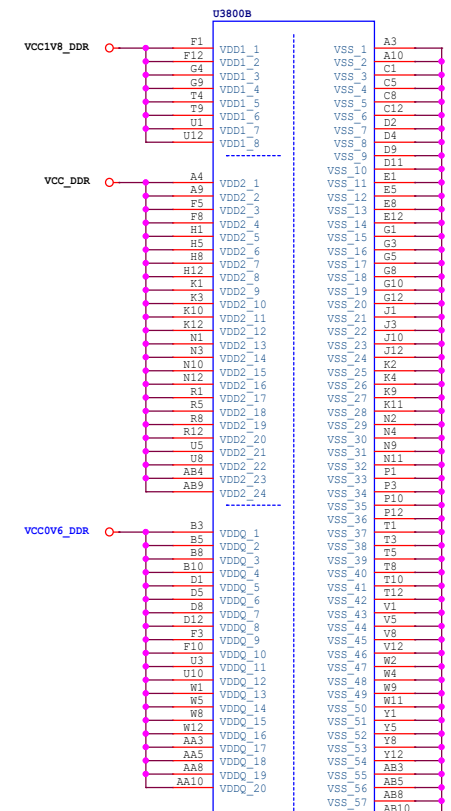
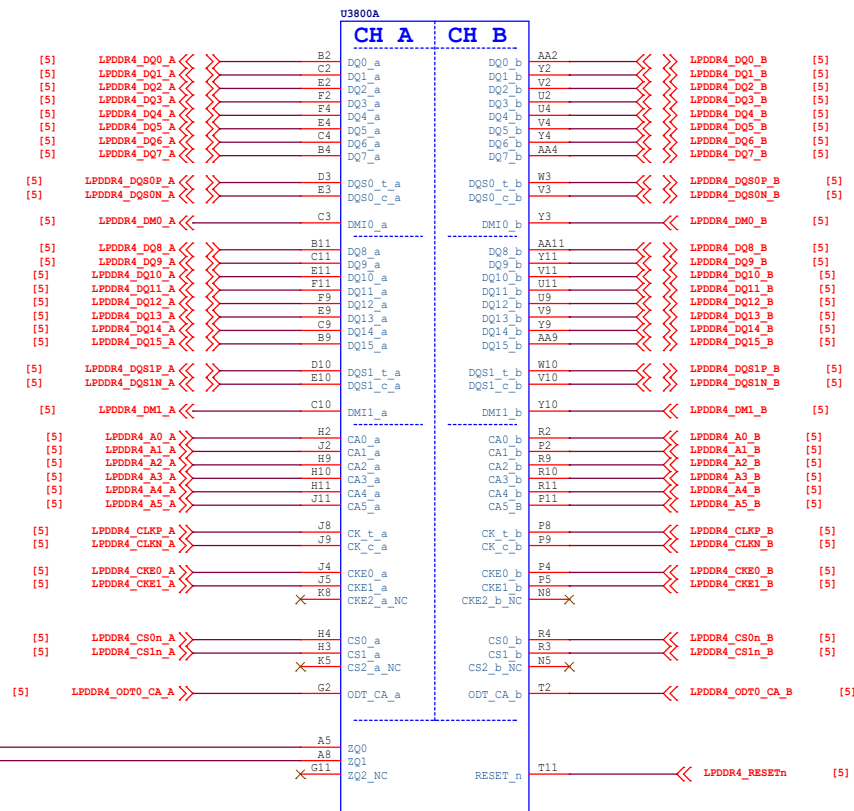
I2C3 SDA M0	/ UART3 RX M0	/ CAN1 RX M0	/ AUDIOPWM LOUT P	/ ACODEC ADC DATA	/ GPIO1 A0 u	D18	I2C3 SDA M0
I2C3 SCL M0	/ UART3 TX M0	/ CAN1 TX M0	/ AUDIOPWM LOUT N	/ ACODEC ADC CLK	/ GPIO1 A1 u	E18	I2C3 SCL M0
I2S1 MCLK M0	/ UART3 RTSn M0	/ SCR CLK	/ PCIE30X1 PERSTn M2		/ GPIO1 A2 d	A19	X
I2S1 SCLK TX M0	/ UART3 CTSn M0	/ SCR IO	/ PCIE30X1 WAKEn M2	/ ACODEC DAC CLK	/ GPIO1 A3 d	B19	X
I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0	/ SPDIF TX M0		/ GPIO1 A4 d	F18	X
I2S1 LRCK TX M0	/ UART4 RTSn M0	/ SCR RST	/ PCIE30X1 CLKREOn M2	/ ACODEC DAC SYNC	/ GPIO1 A5 d	A20	X
I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0	/ AUDIOPWM ROUT P		/ GPIO1 A6 d	C20	X
I2S1 SDO0 M0	/ UART4 CTSn M0	/ SCR DET	/ AUDIOPWM ROUT N	/ ACODEC DAC DATAL	/ GPIO1 A7 d	B20	X
I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0	/ PCIE20 CLKREOn M2	/ ACODEC DAC DATAR	/ GPIO1 B0 d	D20	X
I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0	/ PCIE20 WAKEn M2	/ ACODEC ADC SYNC	/ GPIO1 B1 d	E20	X
I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0	/ PCIE20 PERSTn M2		/ GPIO1 B2 d	A21	X
	/ I2S1 SDI0 M0	/ PDM SDI0 M0			/ GPIO1 B3 d	B21	X

U1000H  
RK3568

VCCIO1



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package



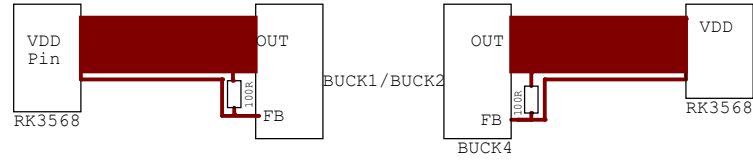
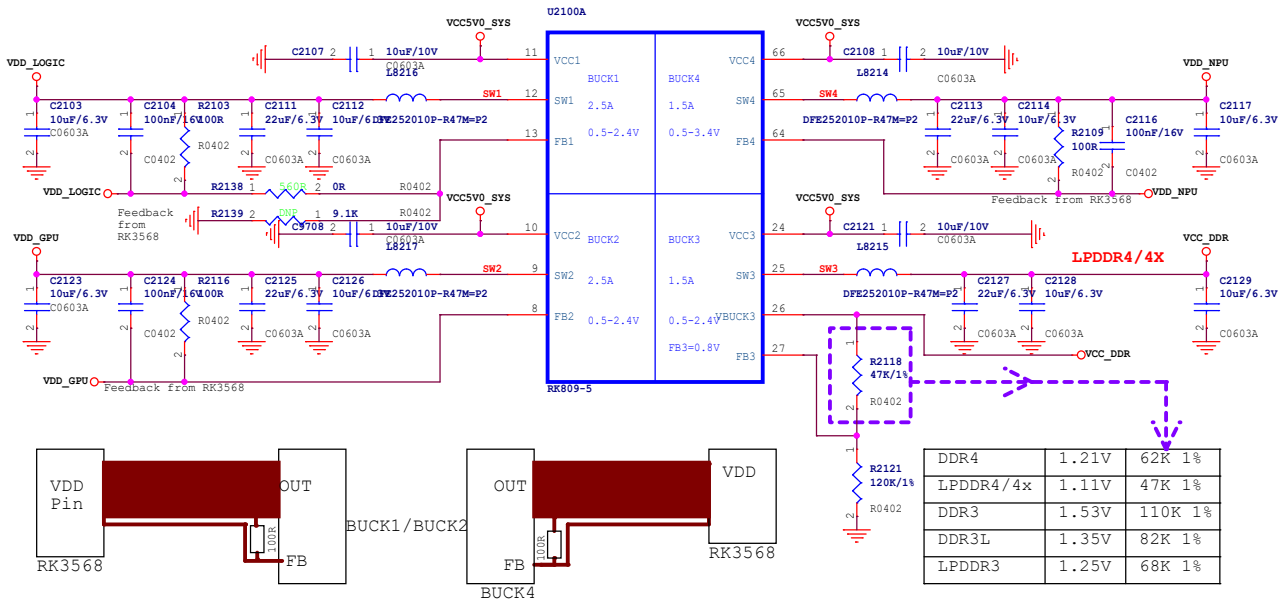
Default LPDDR4x = 0.6V  
Option LPDDR4 = 1.1V

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<https://wiki.friendlyelec.com/>

**NanoPi R5S** Rev 2204

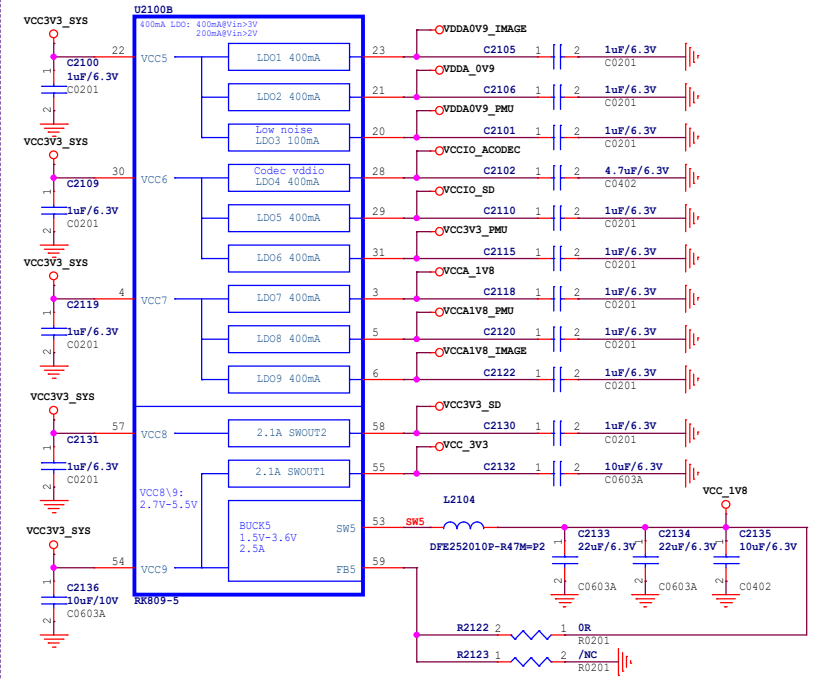
Size	Page Name
A3	14.DRAM-LPDDR4X_1X32bit_200P
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# PMIC RK809 DCDC

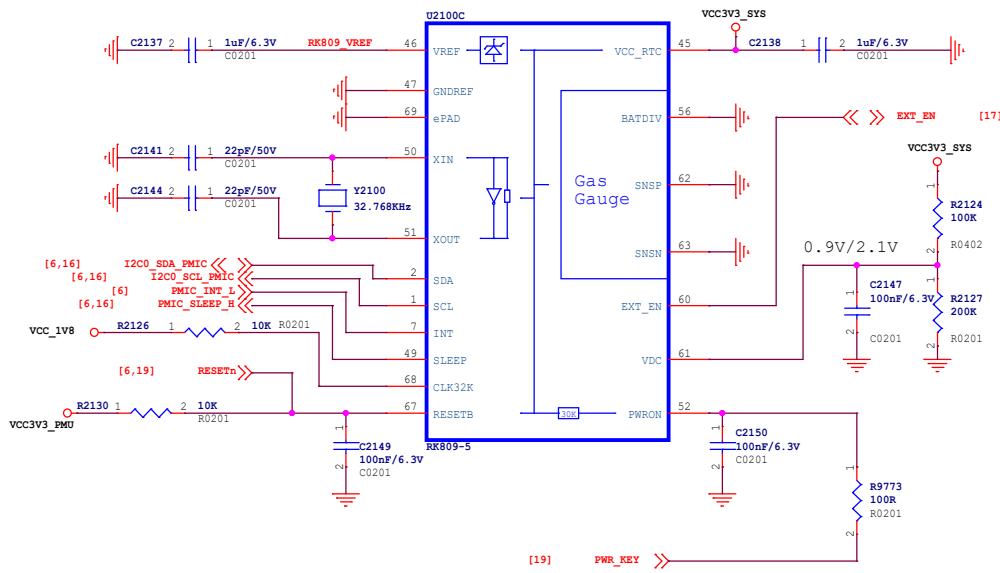


DDR4	1.21V	62K	1%
LPDDR4/4x	1.11V	47K	1%
DDR3	1.53V	110K	1%
DDR3L	1.35V	82K	1%
LPDDR3	1.25V	68K	1%

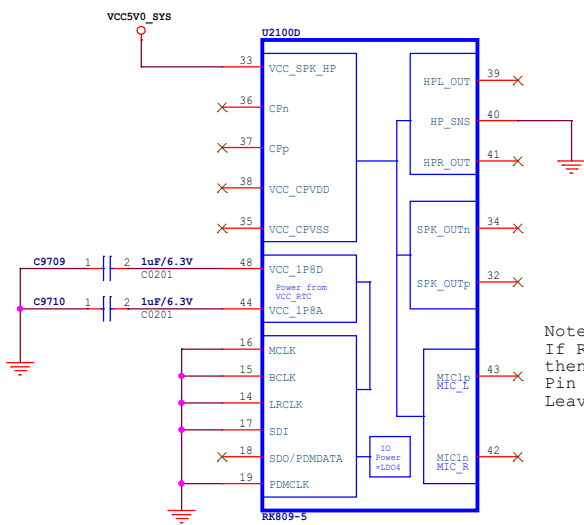
# PMIC RK809 LDO



# PMIC RK809 Management

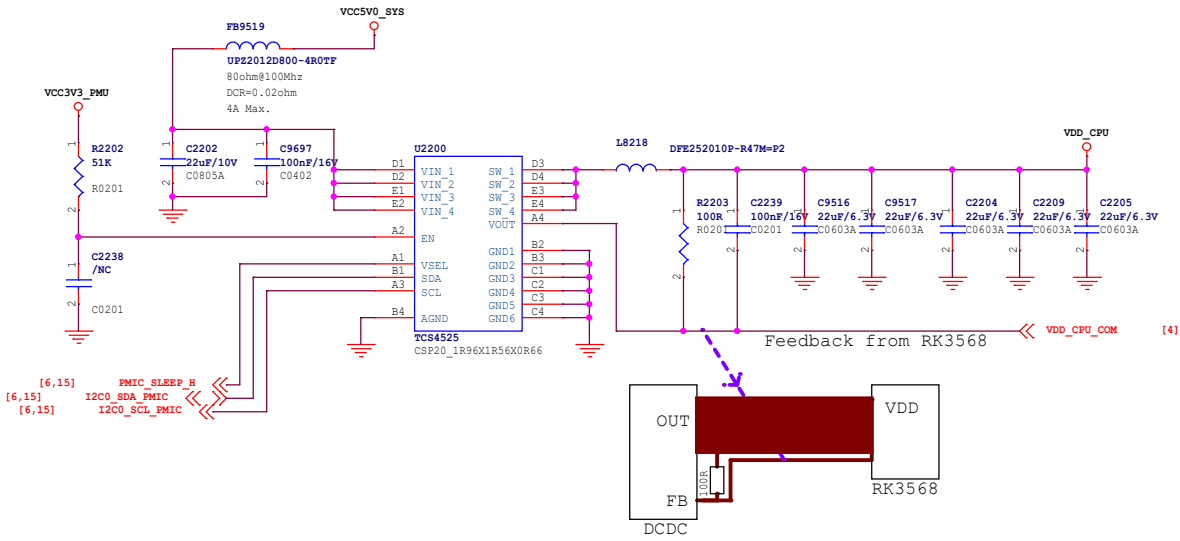


# PMIC RK809 CODEC

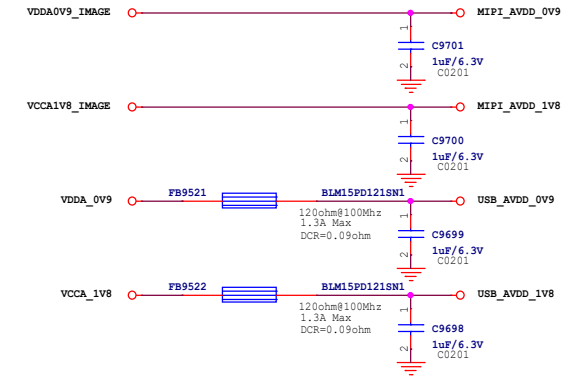


Note:  
If RK809-5 codec is not used,  
then Pin 14,15,16,17,19,40 Tie VSS  
Pin 18,36,37,38,35,39,41,34,32,43,42  
Leave floating

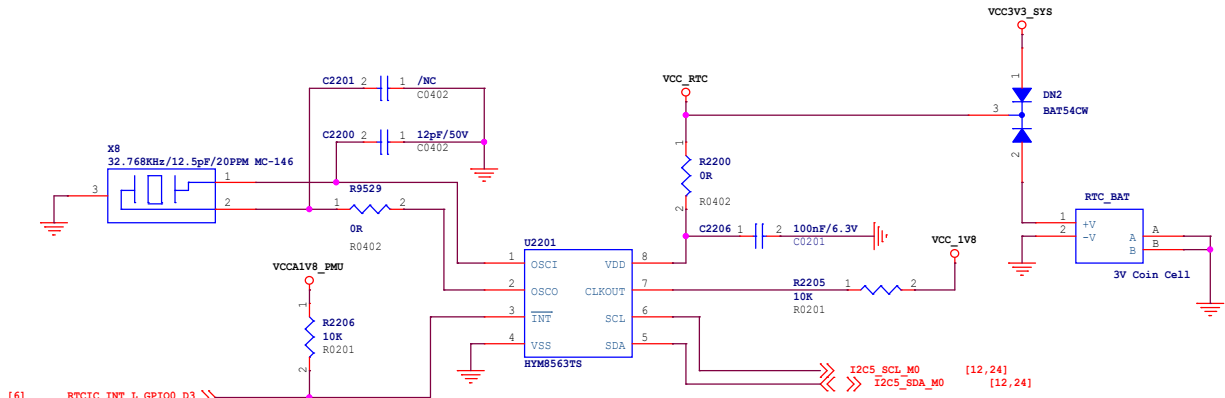
# VDD\_CPU



# VDD\_USB, VDD\_MIPI

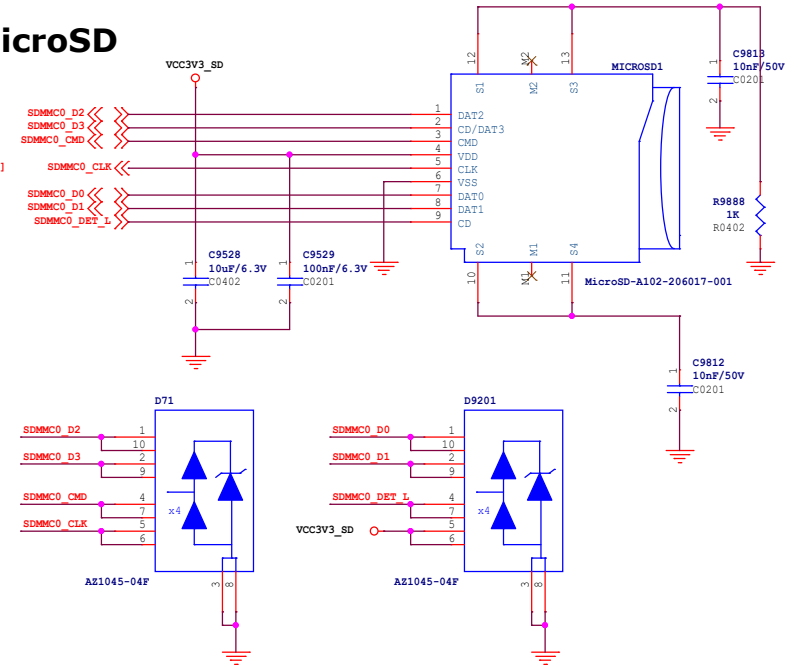


# RTC



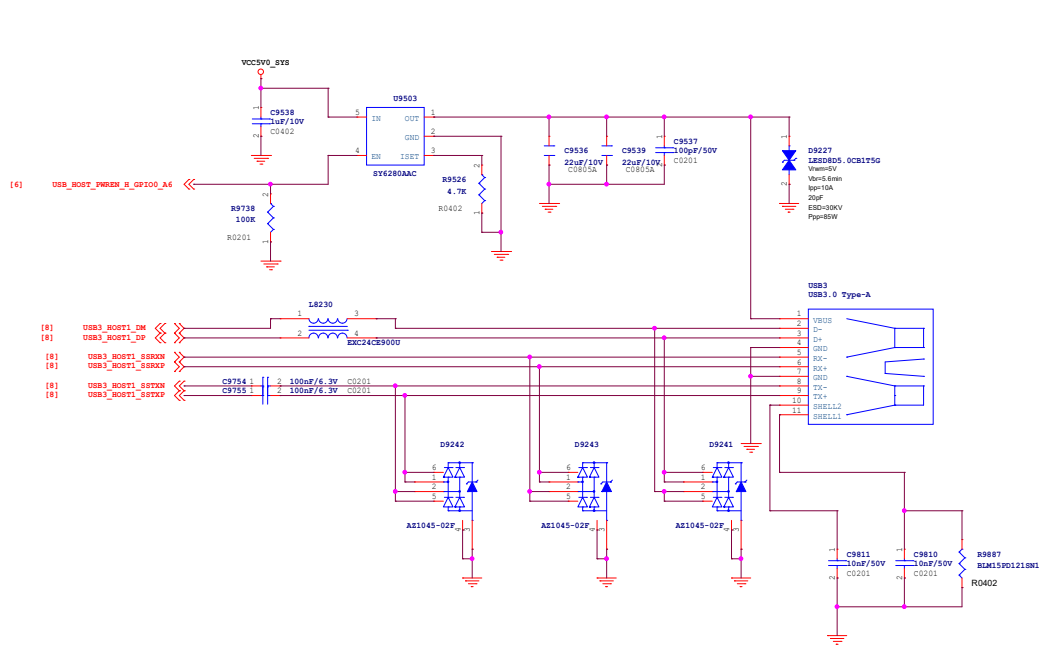
Address: Read A3H, Write A2H  
7bit address: 0x51

# microSD

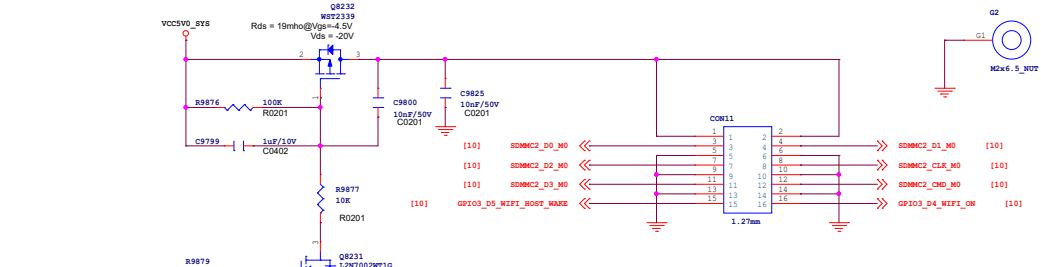




## USB 3.0

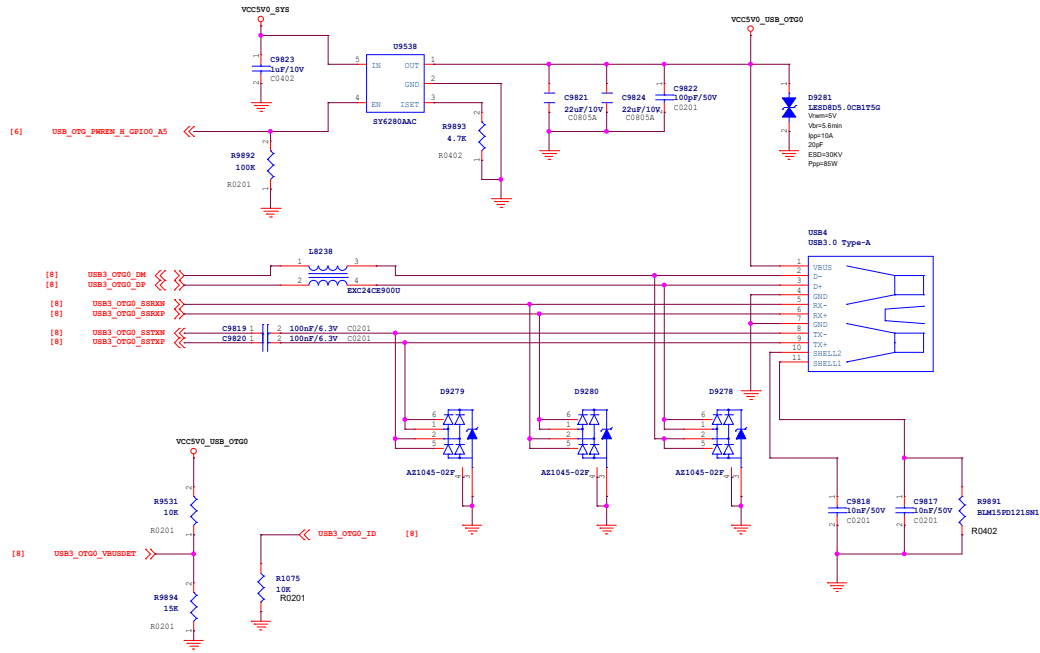


## SDIO/I2S

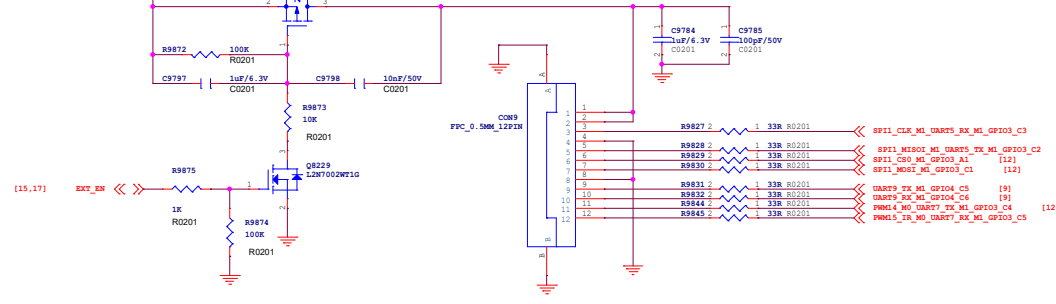


Pin#	GPIO	SD/MMC/SDIO	I2S	POWER	Description
1				VCC5V0_SYS	5V power output
2				VCC5V0_SYS	5V power output
3	GPIO3_C6	SDMMC2_D0_M0	I2S1_MCLK_M1		1.8V level
4	GPIO3_C7	SDMMC2_D1_M0	I2S1_SCLK_TX_M1		1.8V level
5				GND	
6				GND	
7	GPIO3_D0	SDMMC2_D2_M0	I2S1_LRCK_TX_M1		1.8V level
8	GPIO3_D3	SDMMC2_CLK_M0	I2S1_SD1_M1		1.8V level
9				GND	
10				GND	
11	GPIO3_D1	SDMMC2_D3_M0	I2S1_SDO0_M1		1.8V level
12	GPIO3_D2	SDMMC2_CMD_M0	I2S1_SDIO_M1		1.8V level
13				GND	
14				GND	
15	GPIO3_D5	SDMMC2_PWREN_M0	I2S1_SD13_M1		1.8V level
16	GPIO3_D4	SDMMC2_DET_M0	I2S1_SD12_M1		1.8V level

## USB 3.0/ADB/MASK

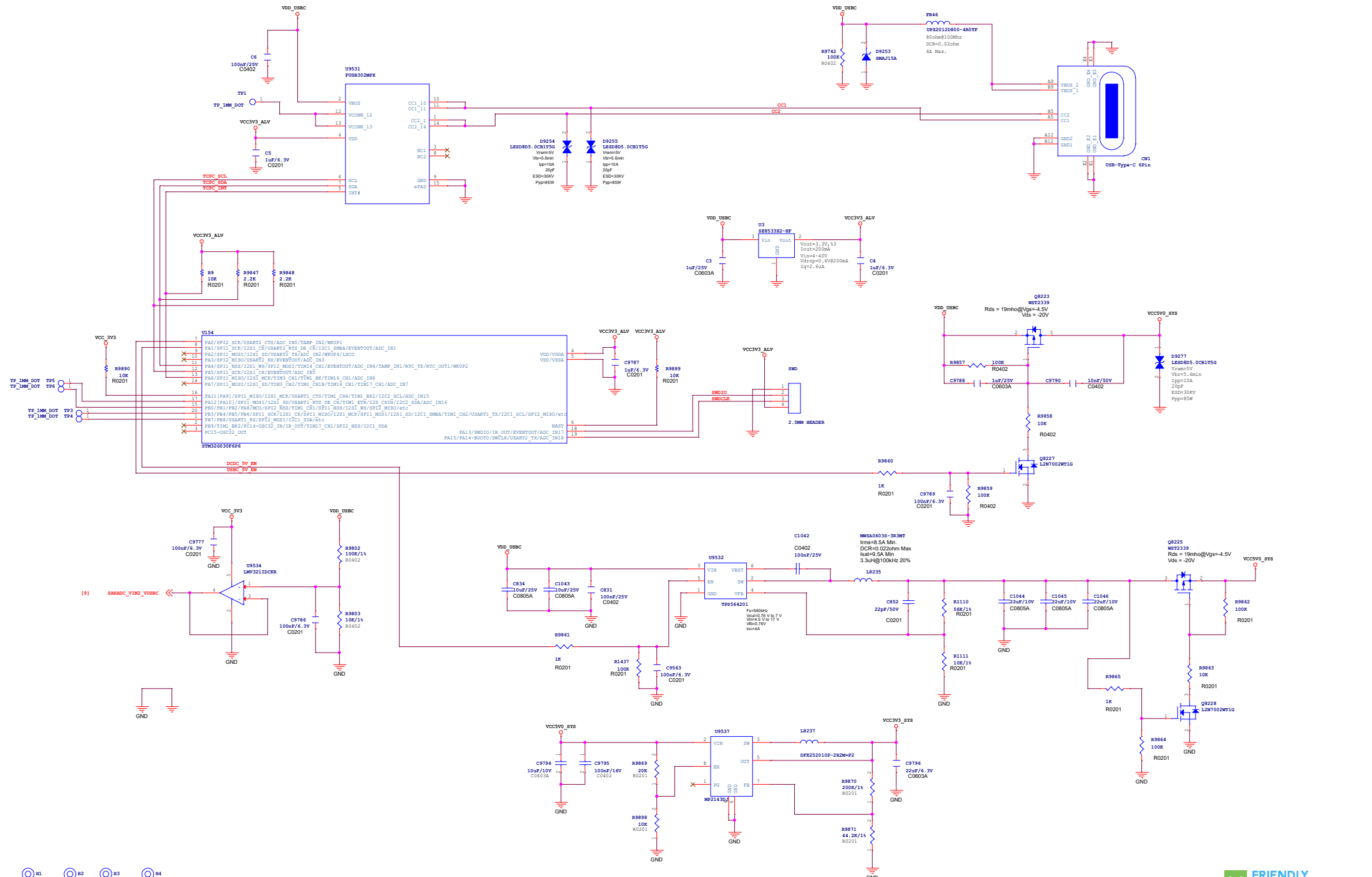


## GPIO

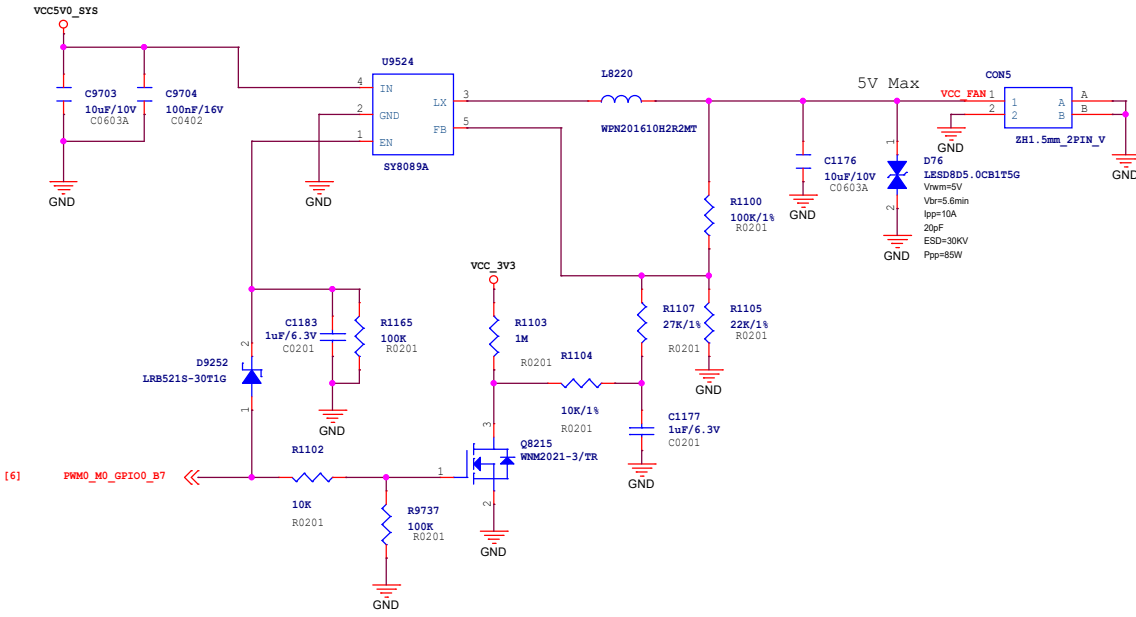


Pin#	GPIO	SPI	UART	PWM	POWER	Description
1					VCC3V3_SYS	3.3V power output
2					VCC3V3_SYS	3.3V power output
3	GPIO3_C3	SPI1_CLK_M1	UART5_RX_M1		3.3V level	
4					GND	
5	GPIO3_C2	SPI1_MISO_M1	UART5_TX_M1		3.3V level	
6	GPIO3_A1	SPI1_CS0_M1			3.3V level	
7	GPIO3_C1	SPI1_MOSI_M1			3.3V level	
8					GND	
9	GPIO4_C5		UART9_TX_M1	PWM12_M1	3.3V level	
10	GPIO4_C6		UART9_RX_M1	PWM13_M1	3.3V level	
11	GPIO3_C4		UART7_TX_M1	PWM14_M0	3.3V level	
12	GPIO3_C5		UART7_RX_M1	PWM15_IR_M0	3.3V level	

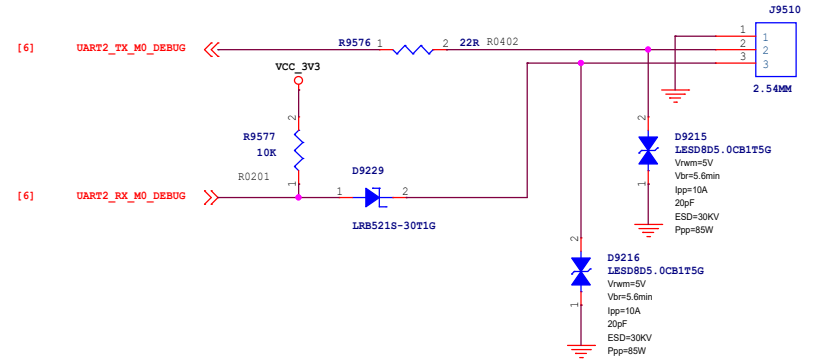
# USB PD



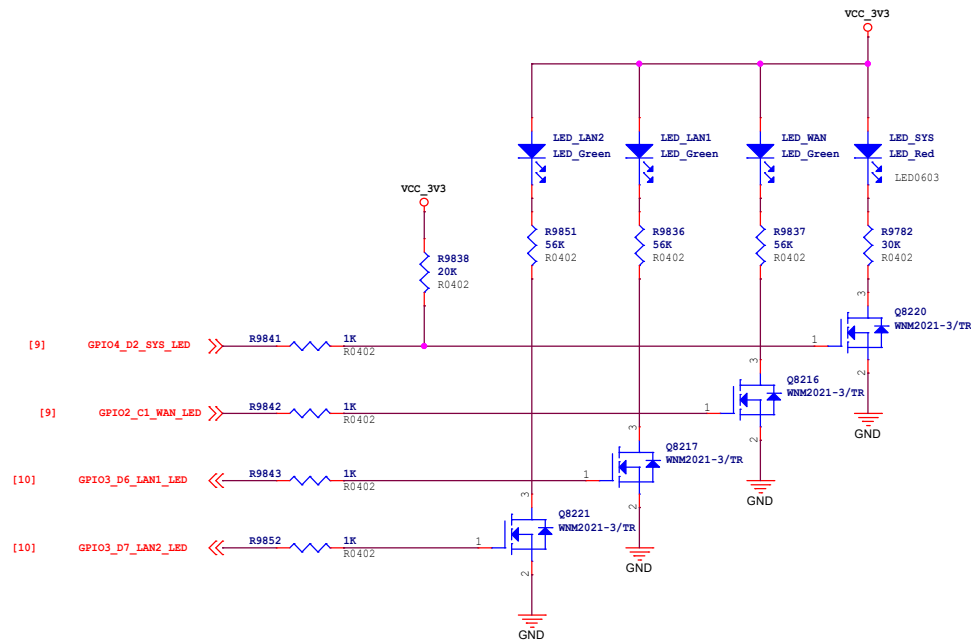
# Cooling Fan



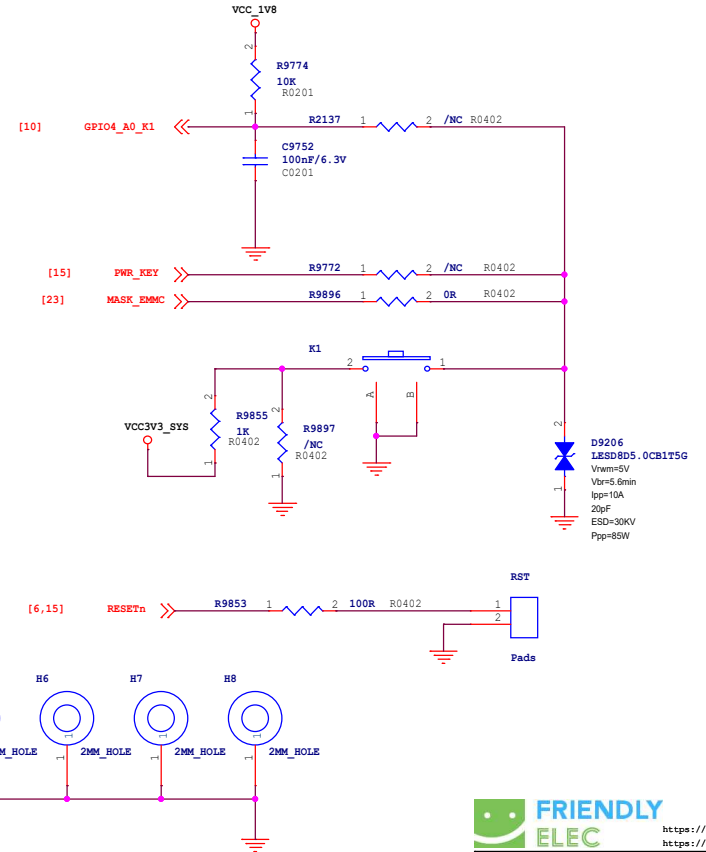
# Debug UART



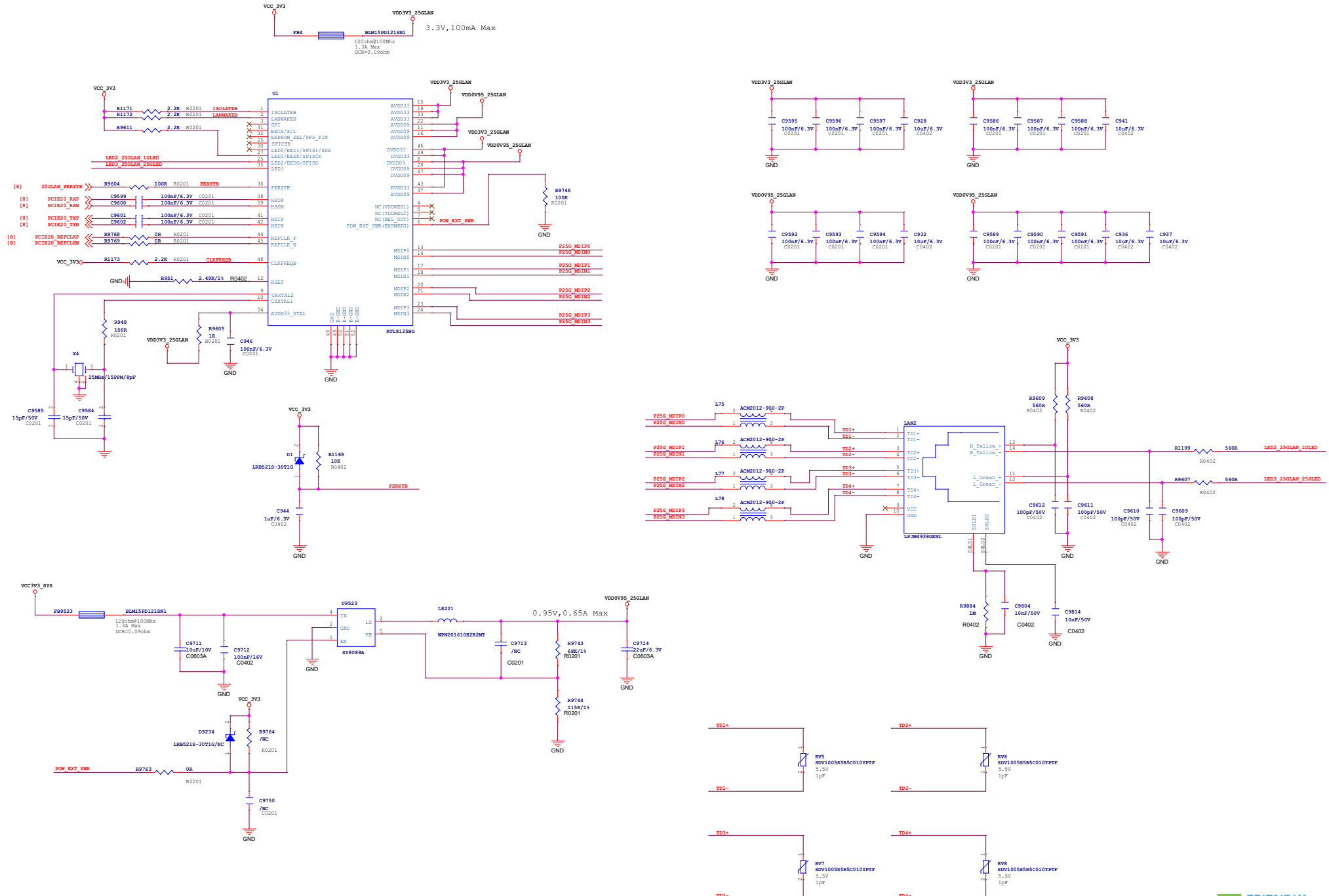
# LED



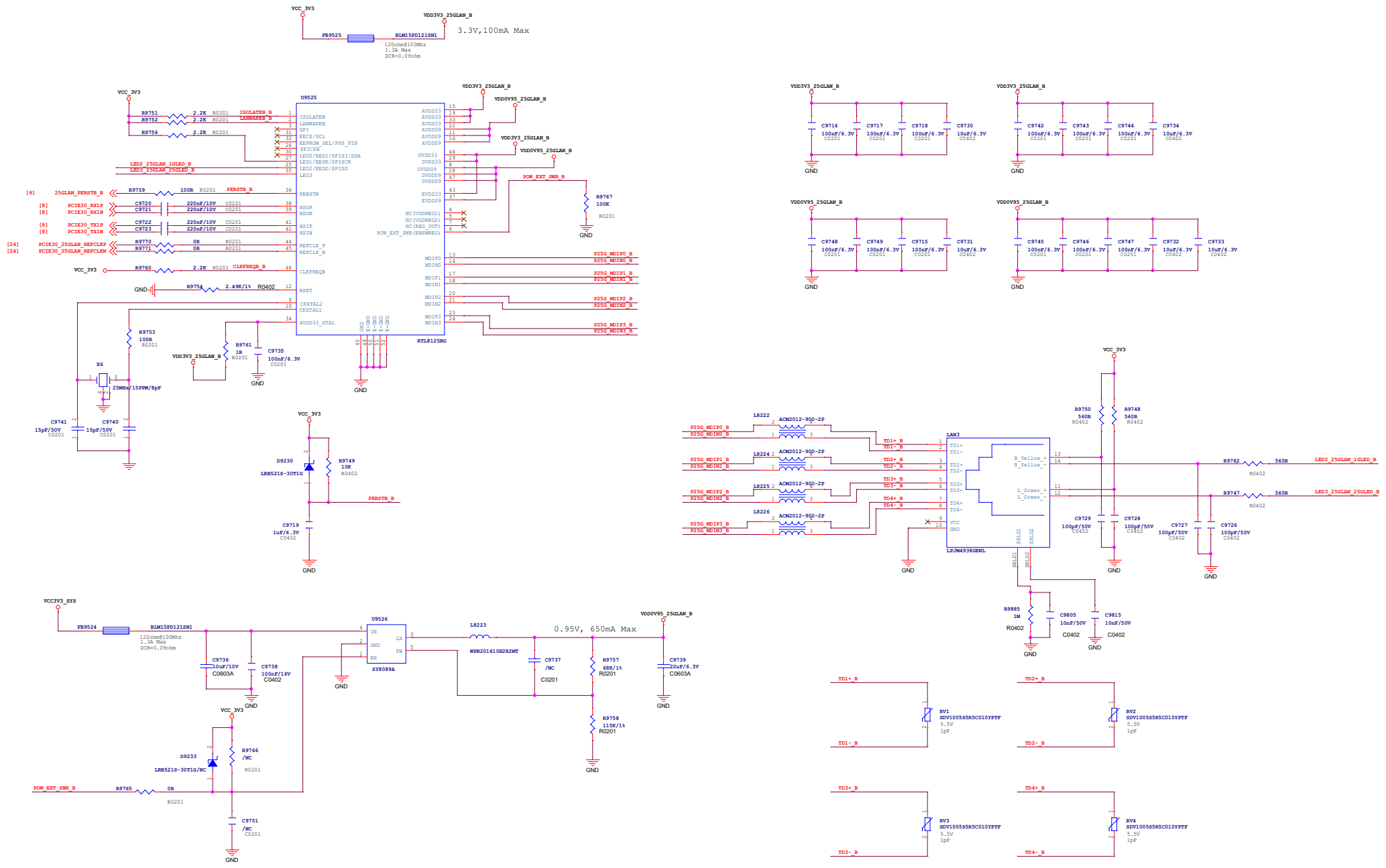
# Button



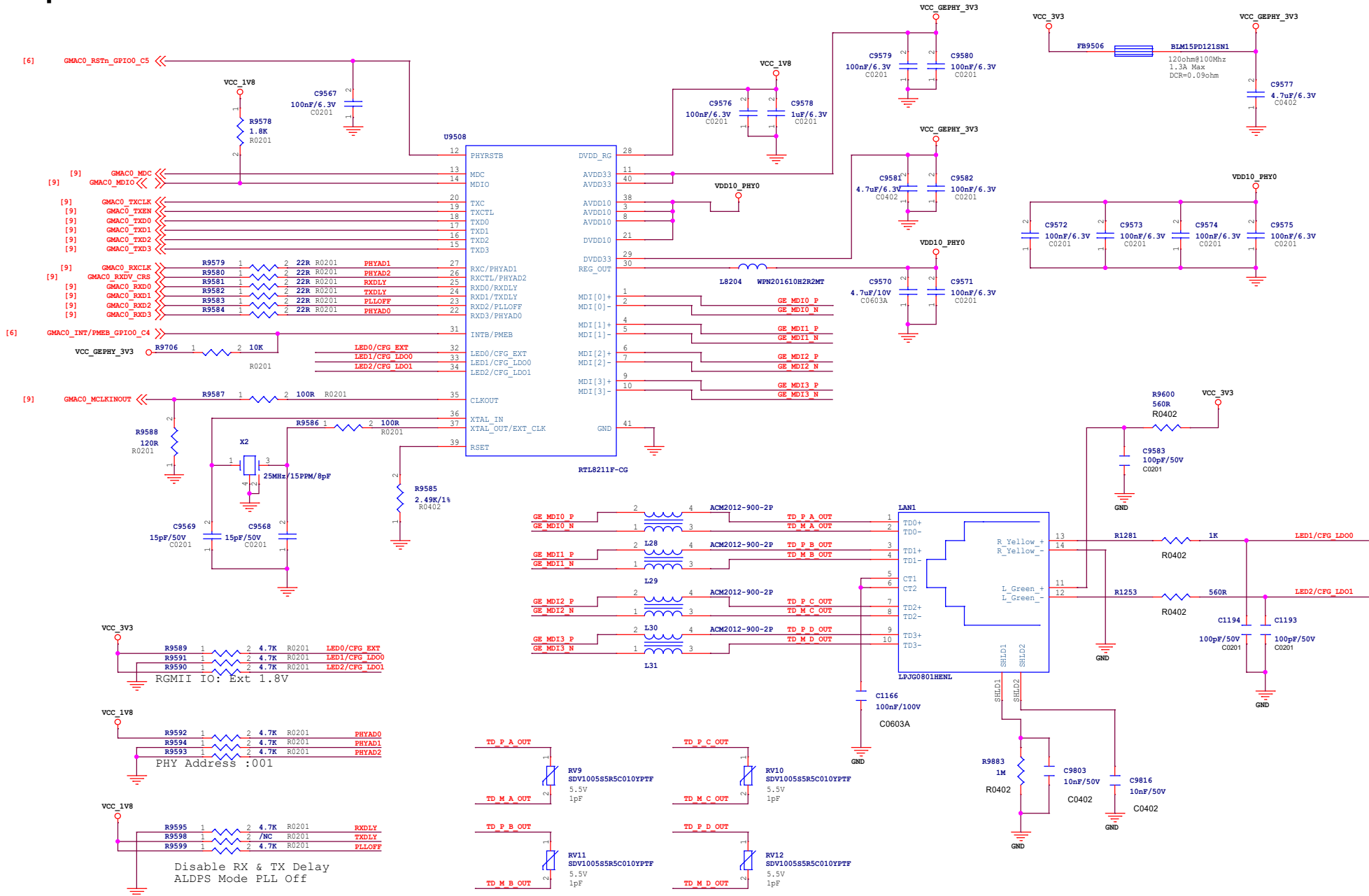
# 2.5Gbps Ethernet



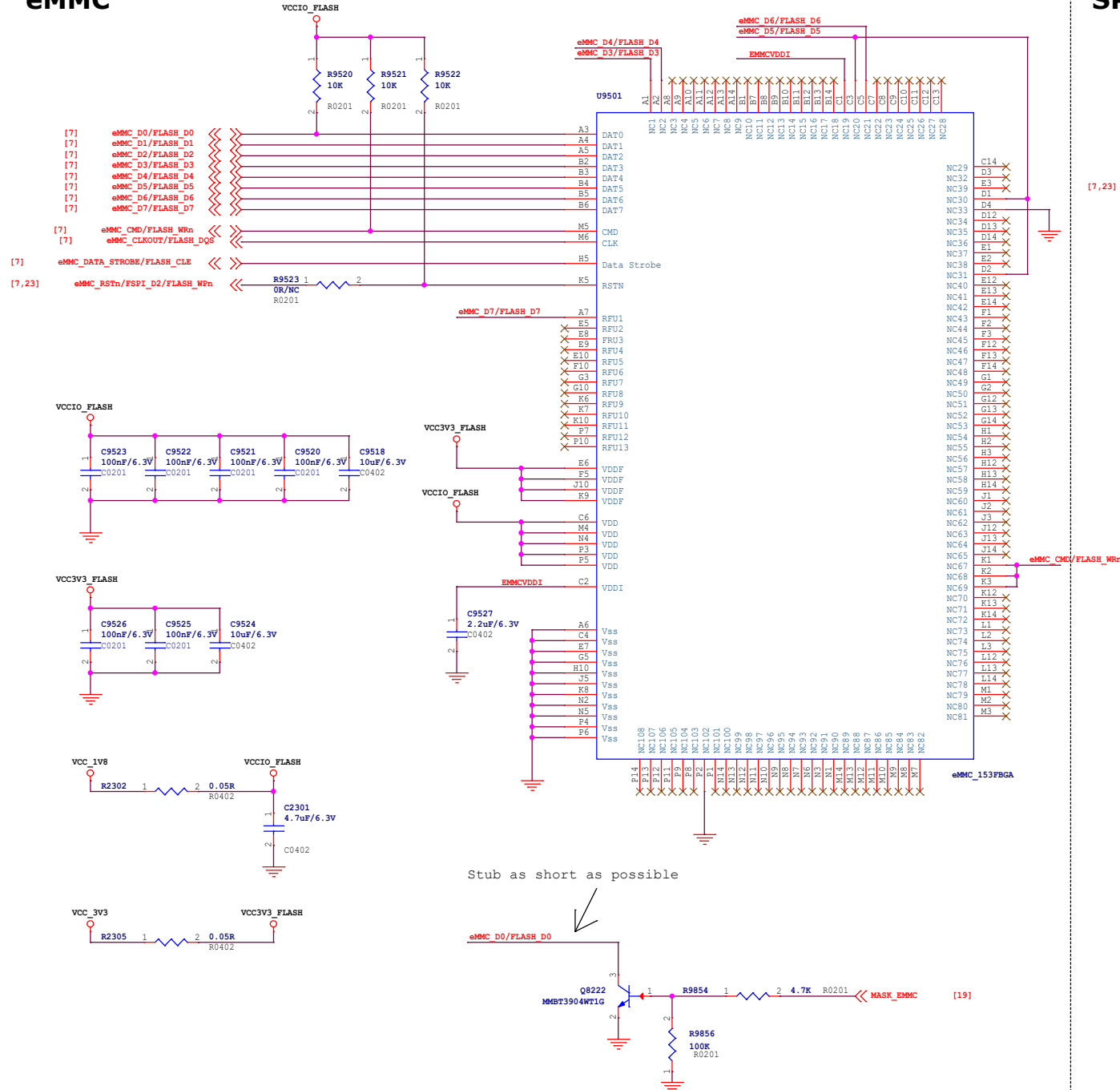
# 2.5Gbps Ethernet



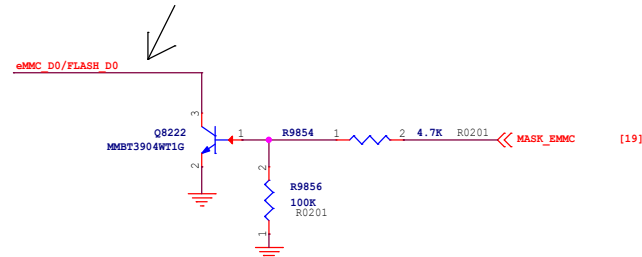
# 1Gbps Ethernet



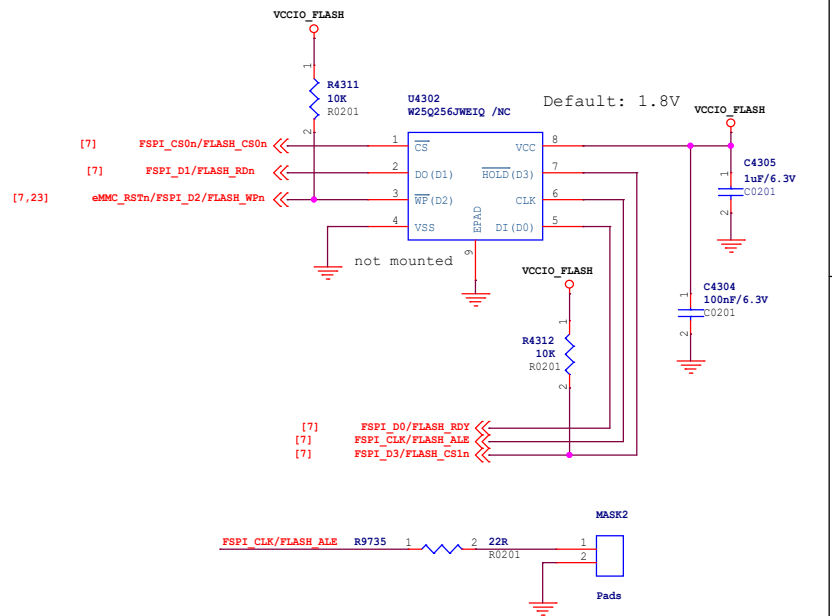
# eMMC



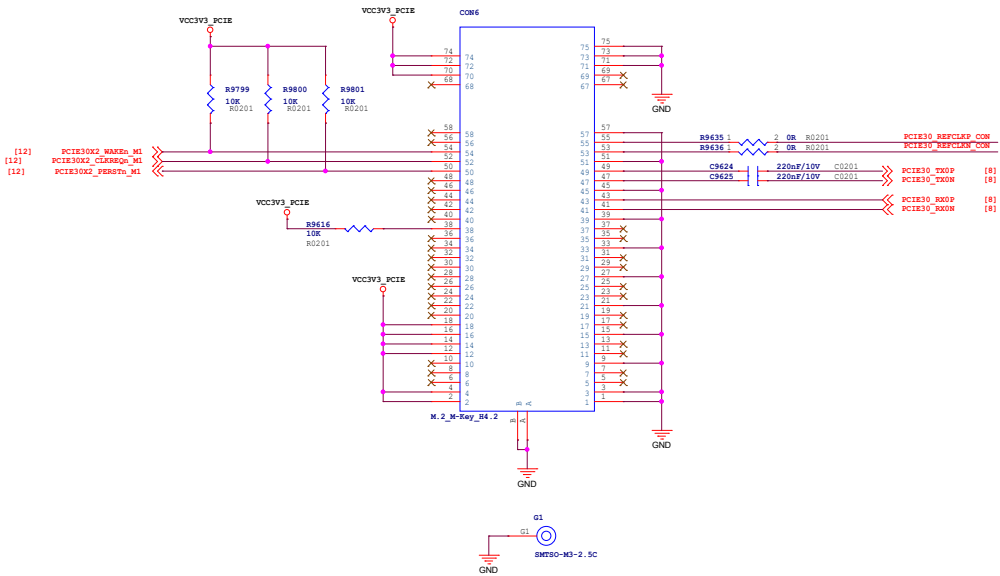
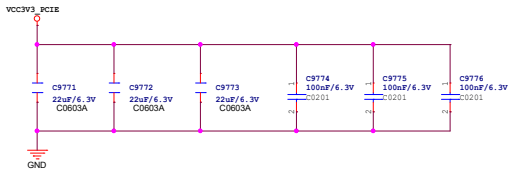
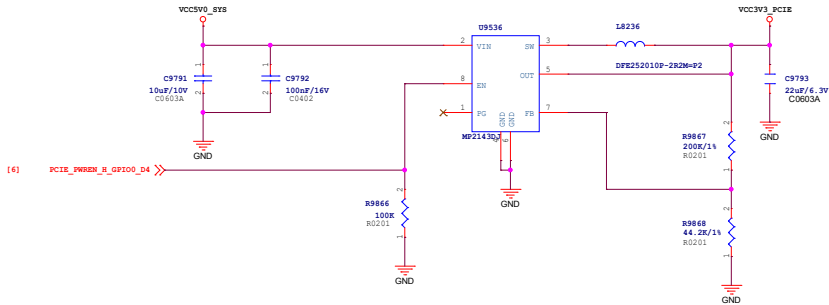
Stub as short as possible



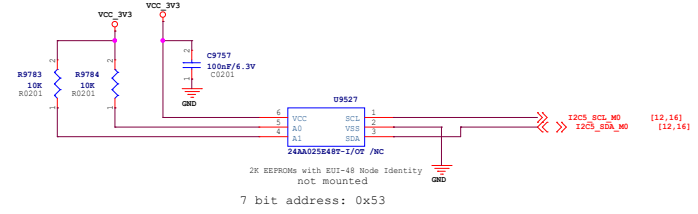
# SPI Flash



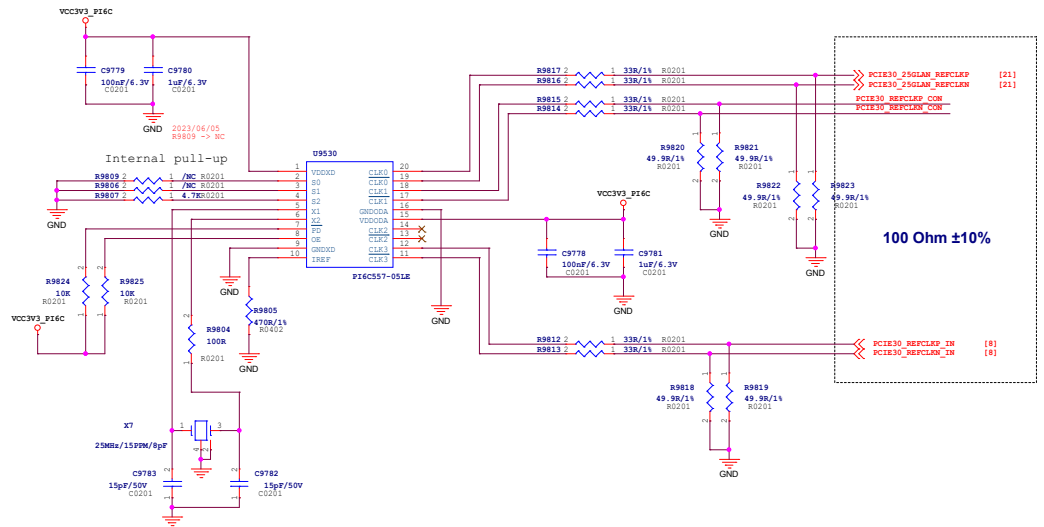
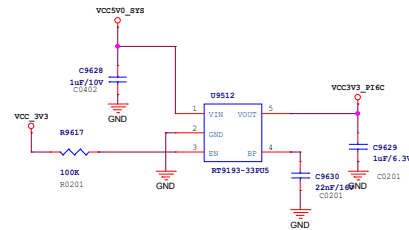
# M.2 NVME



# EUI-48 Node Identity



# PCIe REFCLK





# HDMI 2.0 TX

