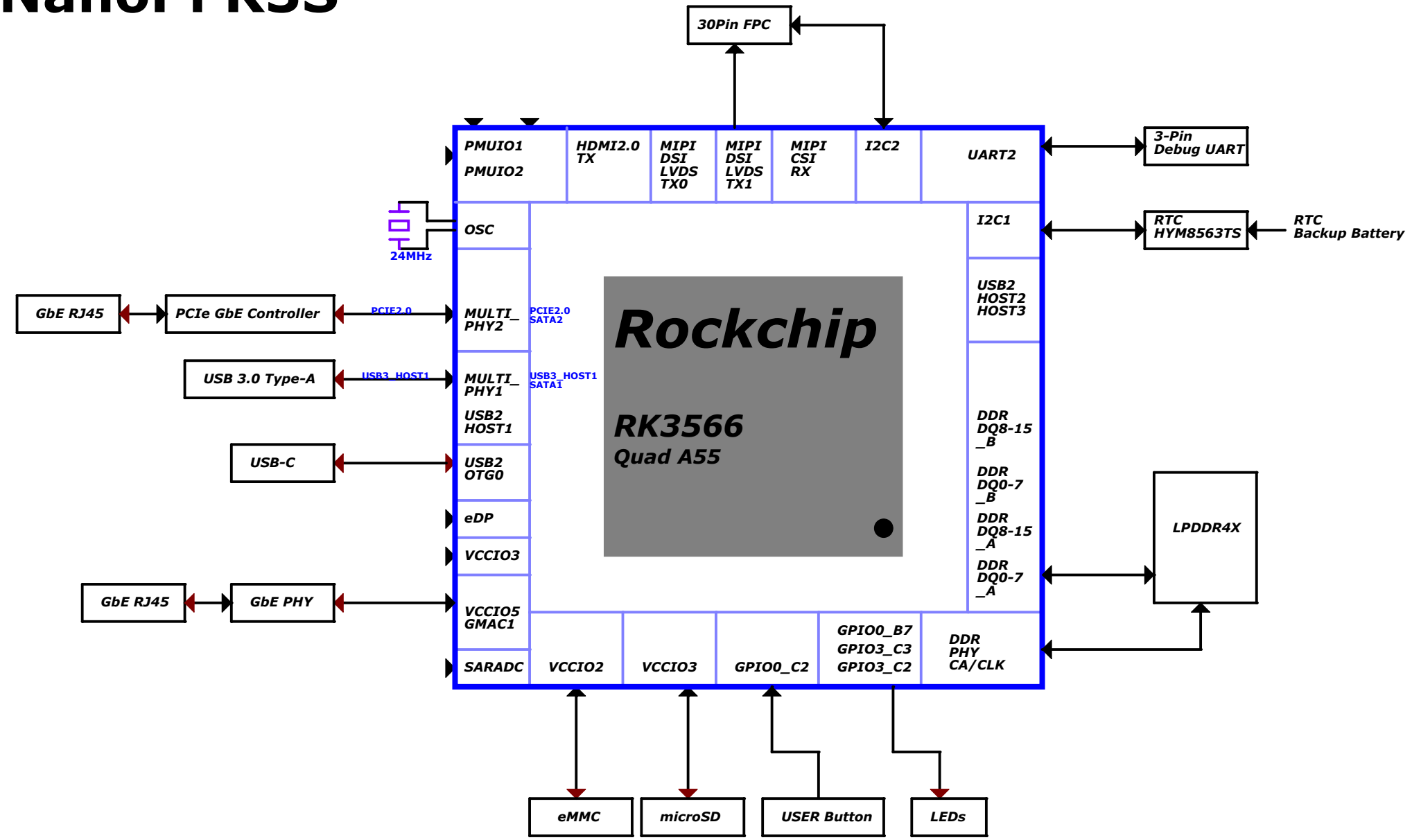
NanoPi R3S



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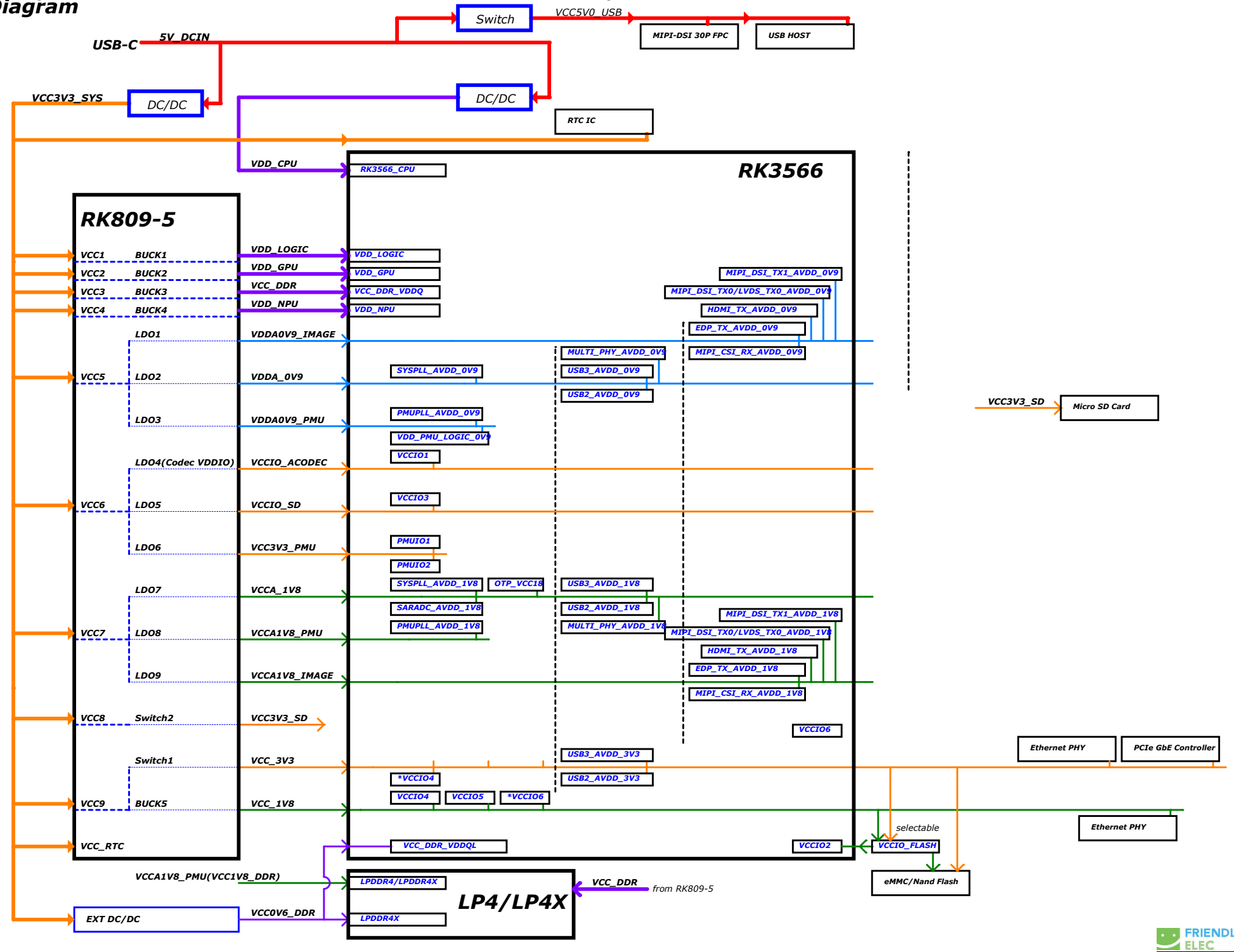
Power Diagram



NanoPi R3S	Rev 2406
Size A2	Page Name 02.Power_Diagram
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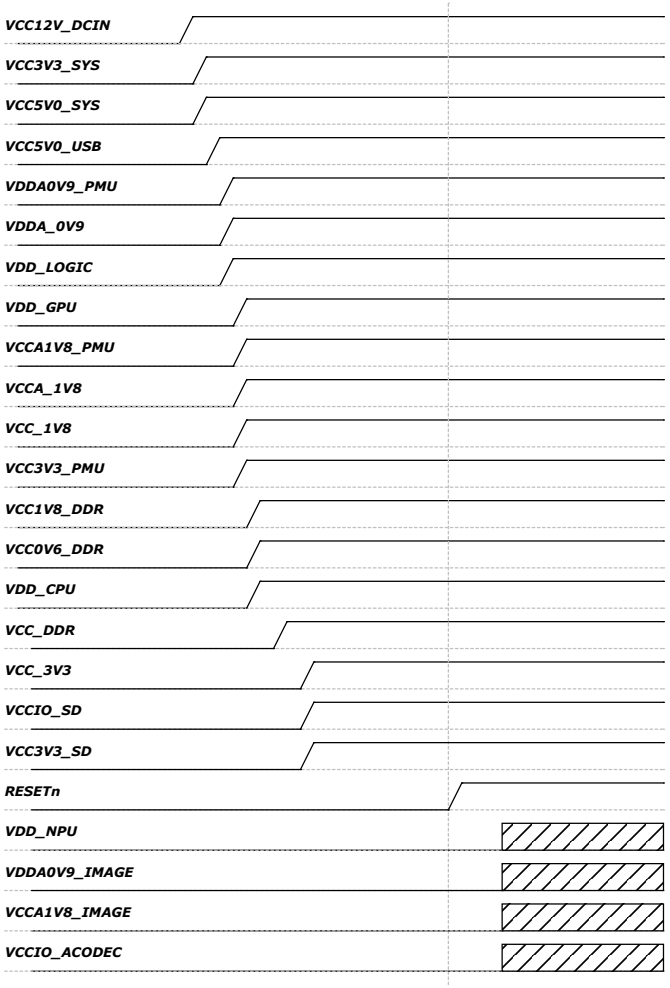
Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	--/0.9V	OFF	OFF
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	--/0.9V	OFF	OFF
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	--/3.3V	OFF	OFF
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	--/1.8V	OFF	OFF
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK809_RESETn			Slot:4+5			
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	ON
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

IO Power Domain Map

Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	3.3V as default, dts config should follow the HW design
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	VCC_1V8 as default, VCC_3V3 optional
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	VCC1V8_DVP as default, VCC_1V8 optional
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

!!! Attention 注意

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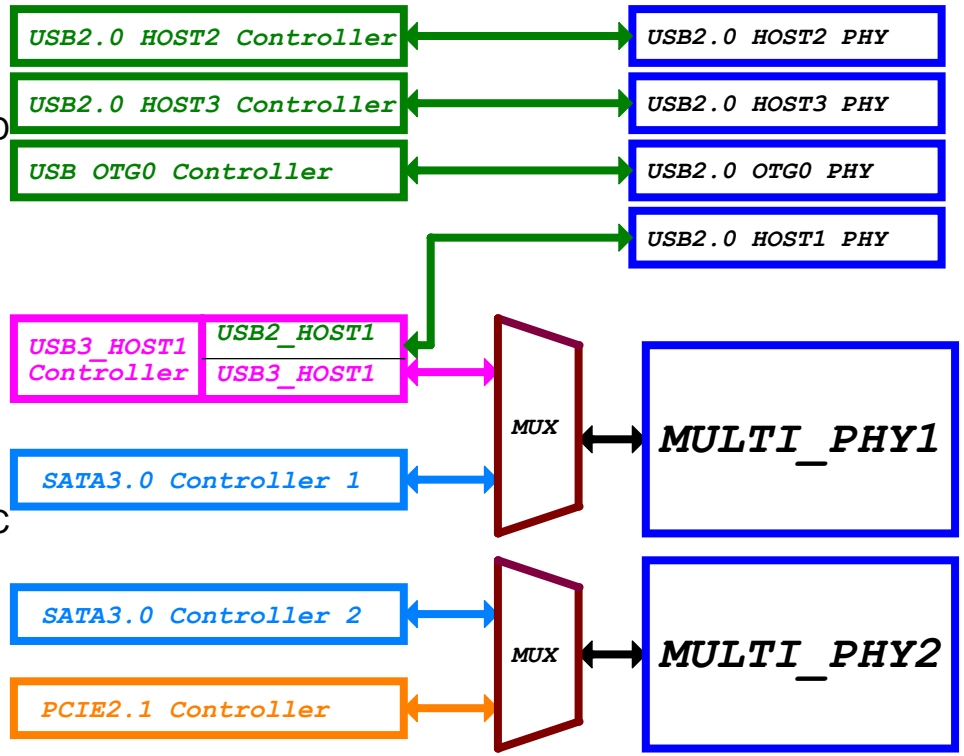
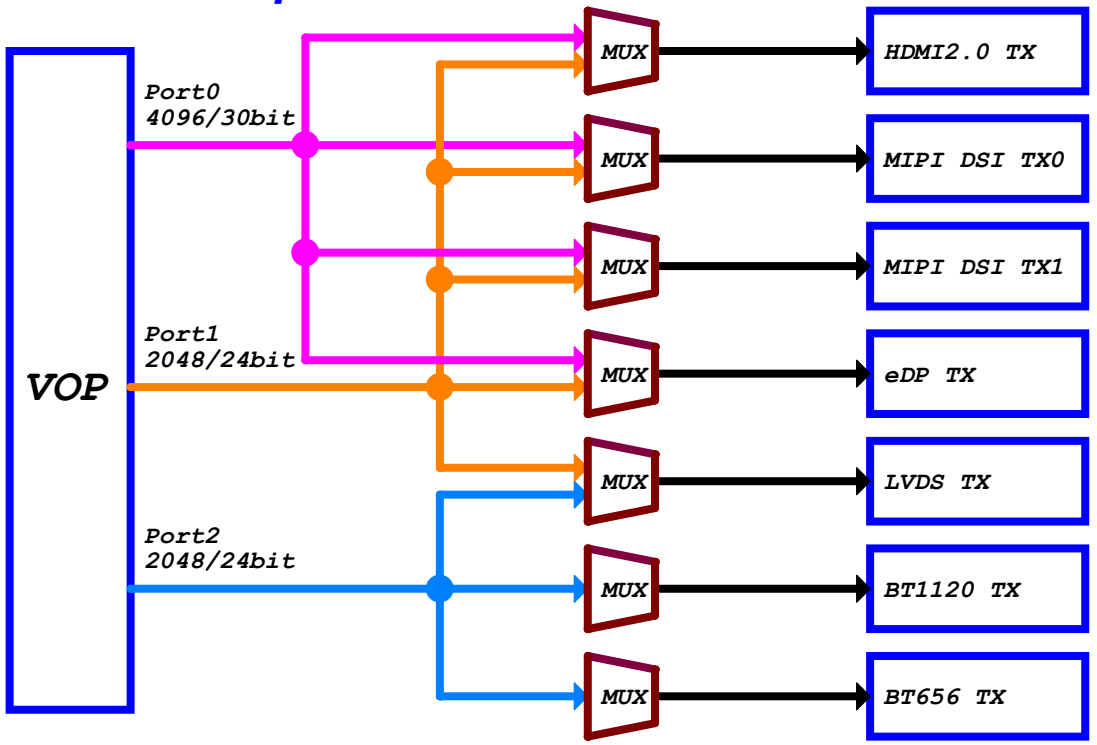
MULTI_PHY1/2 Path Map

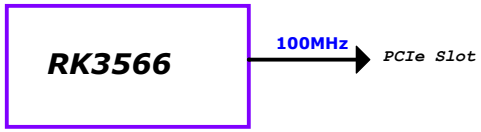


VOP Path Map



RK3566 support max to 2 output display ports! !

PCIe2.1 REFCLK-RC Mode



PCIe2.1 PHY

MULTI_ PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

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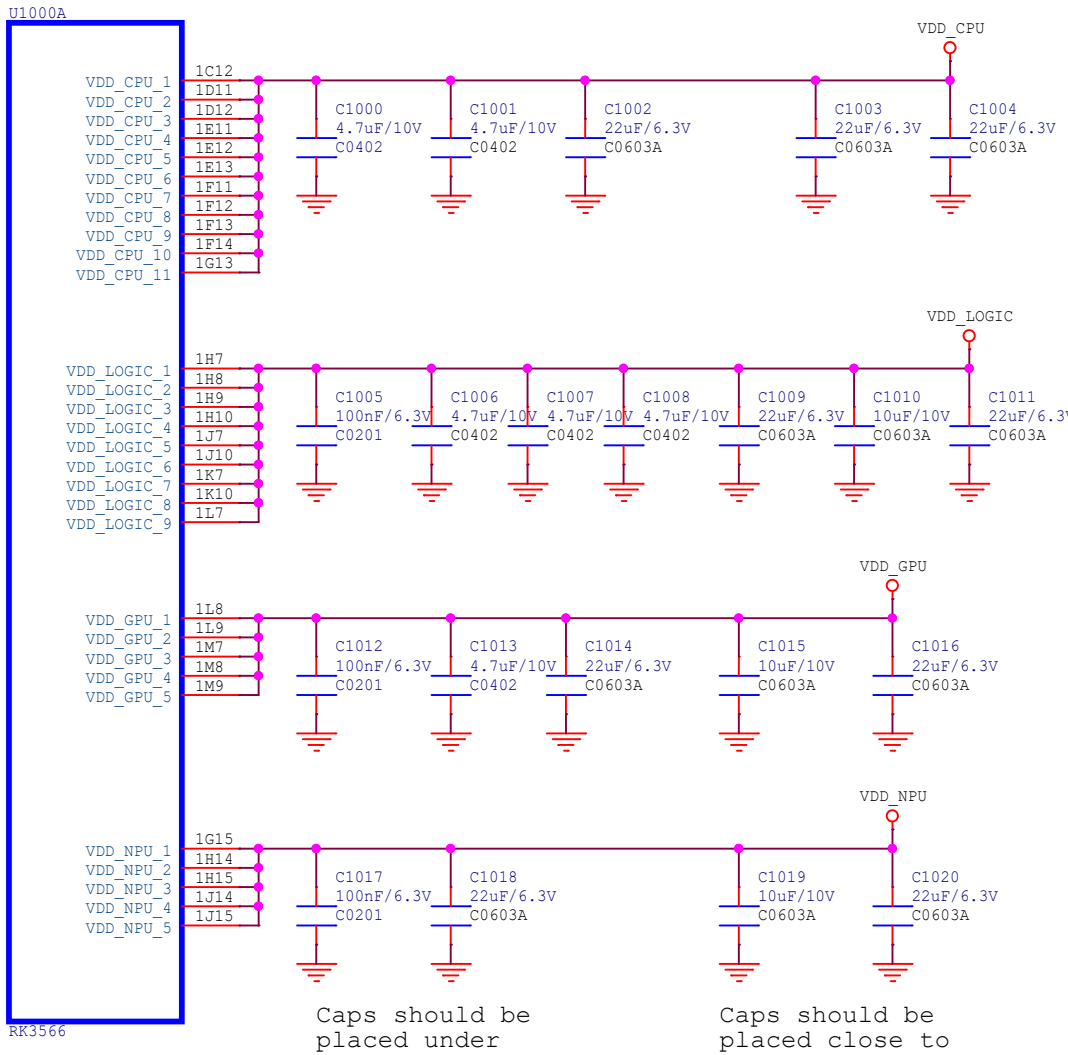
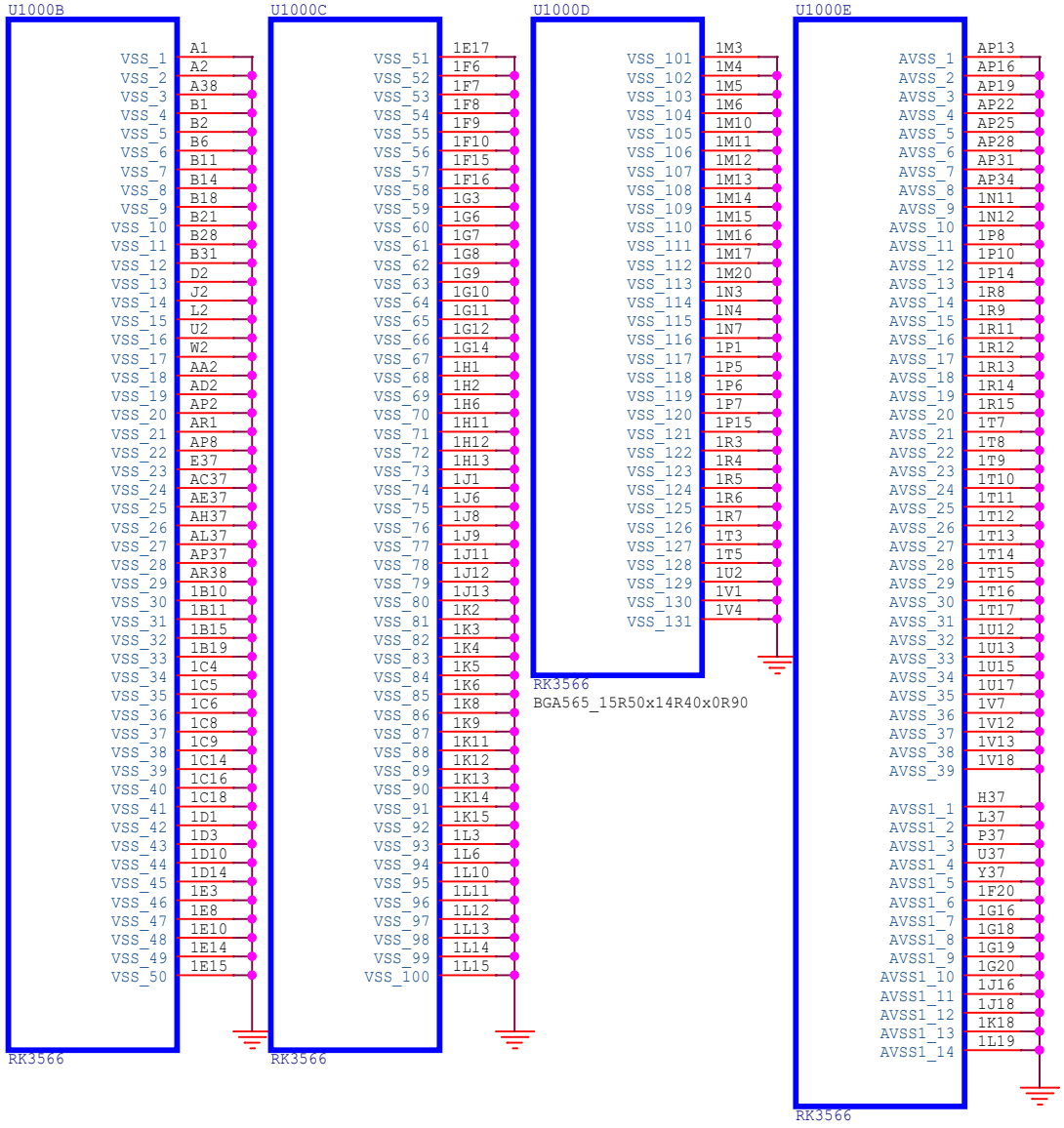
RK3566_ABCDE

(Power&GND)



Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package



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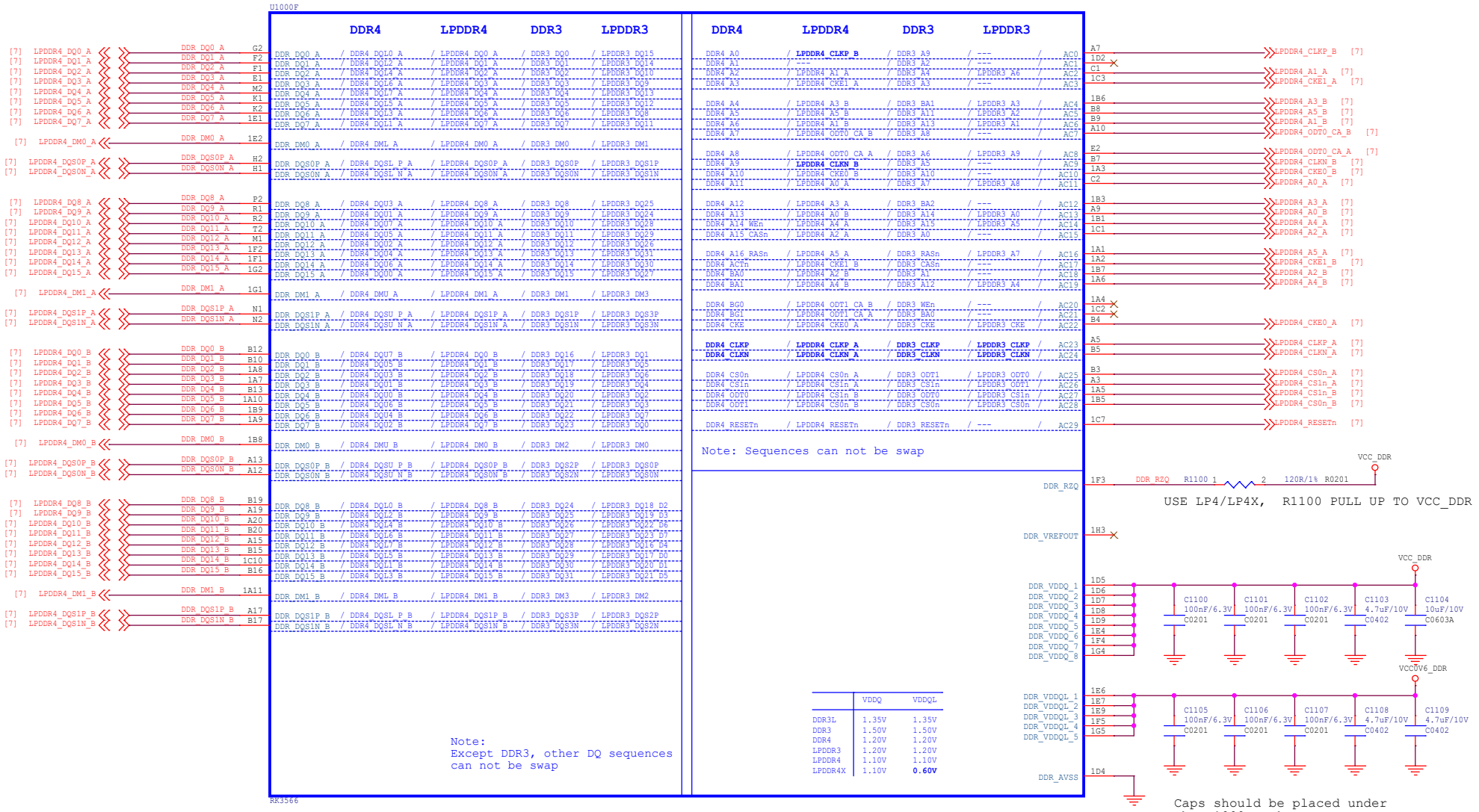
RK3566_F(DDR PHY)



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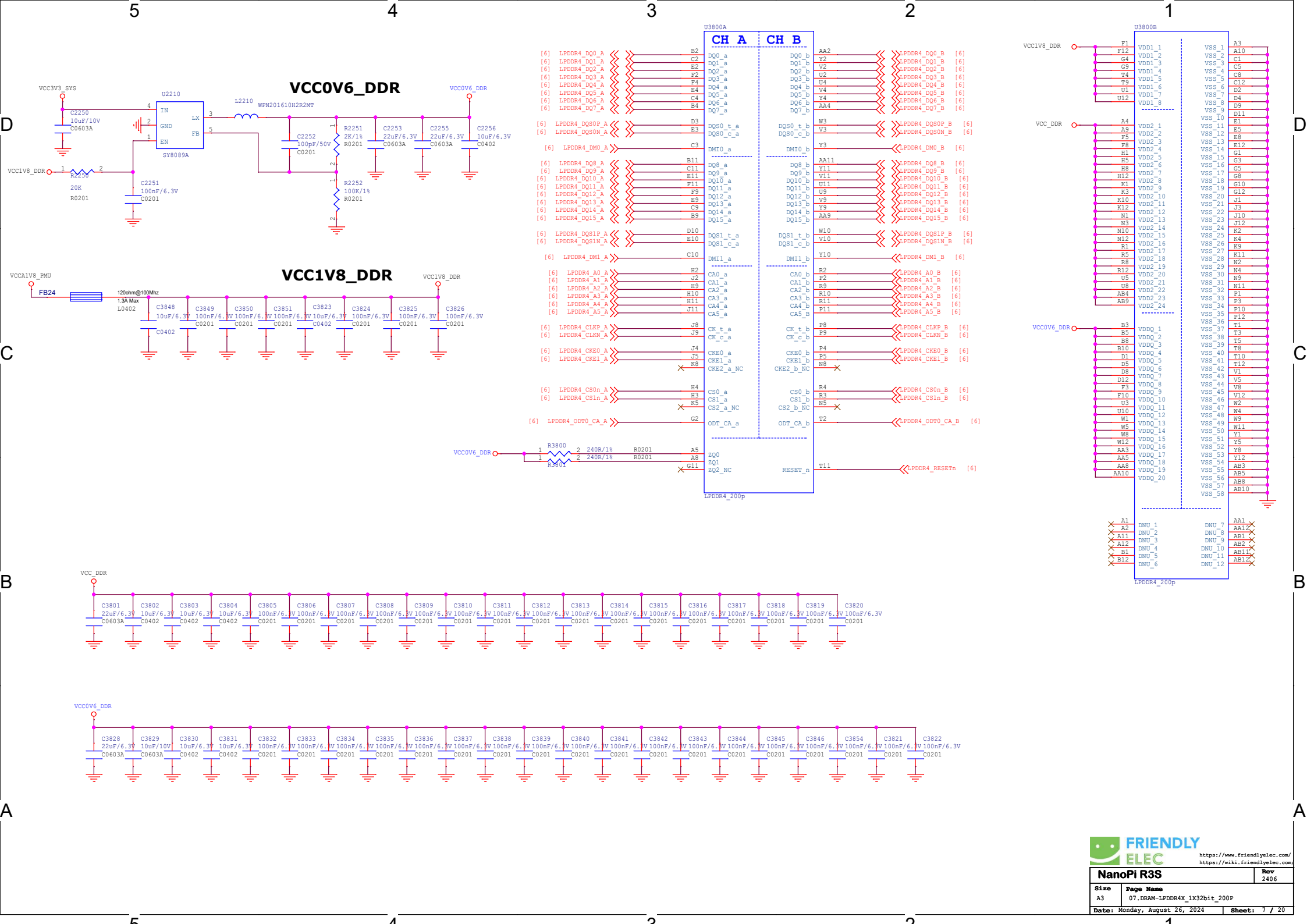

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RK3566_G(OSC/PLL/PMUIO1/2)

FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

FLASH_VOL_SEL R3808 1 2 2.2K R0201 VCC3V3_PMU

Adjust the load capacitor
according to the crystal spec.

U1000G

OSC
XOUT24M
XIN24M

PMU PLL
PMUPLL_AVDD_0V9
PMUPLL_AVDD_1V8
PMUPLL_AVSS

SYS PLL
SYSPLL_AVDD_0V9
SYSPLL_AVDD_1V8
SYSPLL_AVSS

RK3566

PMUIO1 Domain
Operating Voltage=3.3V Only

Operating Voltage =1.8V Only (PMUPLL_AVDD_1V8)

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

PMUIO1/2/OSC Domain Logic Power
Operating Voltage=0.9V

R1200 22R R0201 XOUT24M AD38
X11 24MHz/10PPM/8pF
R1201 1M R0201
XIN24M AD37
C1201 15pF/50V C0201
C1202 15pF/50V C0201
1M18 TVSS
[15] RTCIC_INT_L_GPIO0_D3 1N19 GPIO0_D3_d
1M19 GPIO0_D4_d
1N20 GPIO0_D5_d
1P20 GPIO0_D6_d
DO NOT USE

VDDA0V9_PMU
C1204 1uF/10V C0402
C1205 100nF/6.3V C0201
1P17 PMUPLL_AVDD_0V9
VCCA1V8_PMU
C1206 1uF/10V C0402
C1207 100nF/6.3V C0201
1N18 PMUPLL_AVDD_1V8
1N17 PMUPLL_AVSS
VDDA_0V9
C1208 1uF/10V C0402
C1209 100nF/6.3V C0201
1H5 SYSPLL_AVDD_0V9
VCCA_1V8
C1211 1uF/10V C0402
C1212 100nF/6.3V C0201
1H4 SYSPLL_AVDD_1V8
1J5 SYSPLL_AVSS

Caps should be placed close to the U1000 package
Caps should be placed under the U1000 package

nPOR_u AG38
C1200 100nF/6.3V C0201
Caps should be placed under the U1000 package
RESETn [14,20]

REFCLK_OUT / GPIO0_A0_d
TSADC_SHUT_M0 / TSADC_SHUT_ORG / GPIO0_A1_d
PMIC_SLEEP / TSADC_SHUT_M1 / GPIO0_A2_d
GPIO0_A3_u
SDMMC0_DET / SATA_CP_DET / GPIO0_A4_u
SDMMC0_PWREN / SATA_MP_SWITCH / PCIE20_CLKREQn_M0 / GPIO0_A5_d
GPU_PWREN / SATA_CP_POD / GPIO0_A6_d
FLASH_VOL_SEL / GPIO0_A7_u

1P18 1R20 TSADC_SHUT_M0 R1202 1 0R 2 R0201
1P19 PMIC_SLEEP_H [14,15]
1R19 PMIC_INT_L [14]
AF37 SDMMC0_DET_L [17]
AG37
AJ38 USB_HOST_PWREN_H_GPIO0_A6 [20]
AF38 FLASH_VOL_SEL

VCC3V3_PMU
R1203 2.2K R0201
R1204 2.2K R0201
I2C0_SCL_PMIC
I2C0_SDA_PMIC

PMUIO1
1P16 C1203 100nF/6.3V C0201

CLK32K_IN / CLK32K_OUT0 / GPIO0_B0_u
I2C0_SCL / GPIO0_B1_u
I2C0_SDA / GPIO0_B2_u
I2C1_SCL / MCU_JTAG_TDO / GPIO0_B3_u
I2C1_SDA / PCIE2U_BUTTONRSTn / MCU_JTAG_TCK / GPIO0_B4_u
PWM1_M1 / I2C2_SCL_M0 / SPI0_CLK_M0 / PCIE2U_WAKEn_M0 / GPIO0_B5_u
PWM2_M1 / I2C2_SDA_M0 / SPI0_MOSI_M0 / PCIE2U_PERSTn_M0 / GPIO0_B6_u
PWM0_M0 / CPUAVS / GPIO0_B7_d
PWM1_M0 / GPUAVS / UART0_RX / GPIO0_C0_d
PWM2_M0 / NPUAVS / UART0_TX / MCU_JTAG_TDI / GPIO0_C1_d
PWM3_IR / EDP_HPDIN_M1 / MCU_JTAG_TMS / GPIO0_C2_d
PWM4 / VOP_PWM_M0 / MCU_JTAG_TRSTn / GPIO0_C3_d
PWM5 / SPI0_CS1_M0 / UART0_RTSn / GPIO0_C4_d
PWM6 / SPI0_MISO_M0 / GPIO0_C5_d
PWM7_IR / SPI0_CS0_M0 / GPIO0_C6_d
PWM0_M1 / HDMITX_CEC_M1 / UART0_CTSn / GPIO0_C7_d
UART2_RX_M0 / GPIO0_D0_u
UART2_TX_M0 / GPIO0_D1_u

1T20 AJ37 I2C0_SCL_PMIC [14,15]
AK38 I2C0_SDA_PMIC [14,15]
AK37 I2C1_SCL [15]
AM38 I2C1_SDA [15]
1U20 I2C2_SCL_M0 [20]
1R16 I2C2_SDA_M0 [20]
1R17 GPIO0_B7_LED_SYS [20]

VCC3V3_PMU
R3819 2.2K R0201
R3820 2.2K R0201
I2C1_SCL
I2C1_SDA

1T19 1R18 AM37 GPIO0_C2_K1 [20]
AN38 PWM4_LCD_BL [20]
AN37 GPIO0_C4_LCD_RST [20]
1U19 GPIO0_C5_TP_RST [20]
1T18 GPIO0_C6_TP_INT [20]
1V20

1V19 UART2_RX_M0_DEBUG [15]
1U18 UART2_TX_M0_DEBUG [15]

VCC3V3_PMU
R3881 2.2K R0201
R3882 2.2K R0201
I2C2_SCL_M0
I2C2_SDA_M0

PMUIO2
1N15 C1210 100nF/6.3V C0201
Caps should be placed under the U1000 package

PMU_VDD_LOGIC_0V9
1N16 C1213 100nF/6.3V C0201
VDDA0V9_PMU C1214 1uF/10V C0402
Caps should be placed close to the U1000 package

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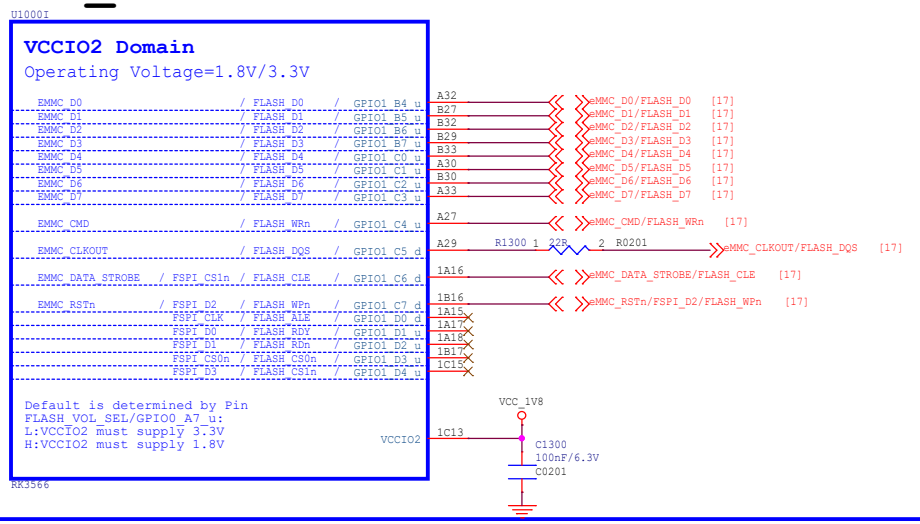
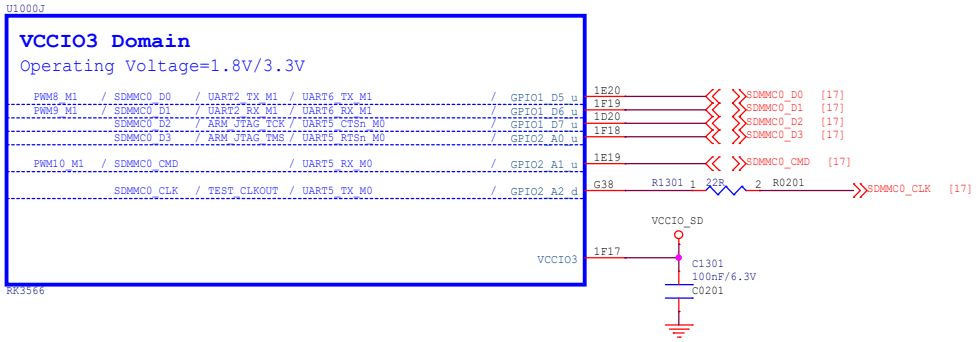
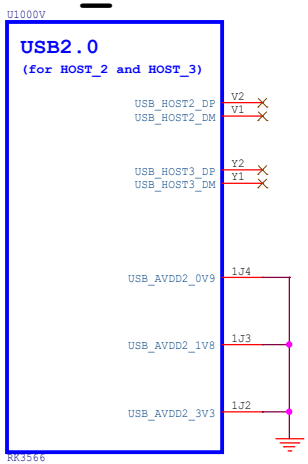
RK3566_I(VCCIO2 Domain)



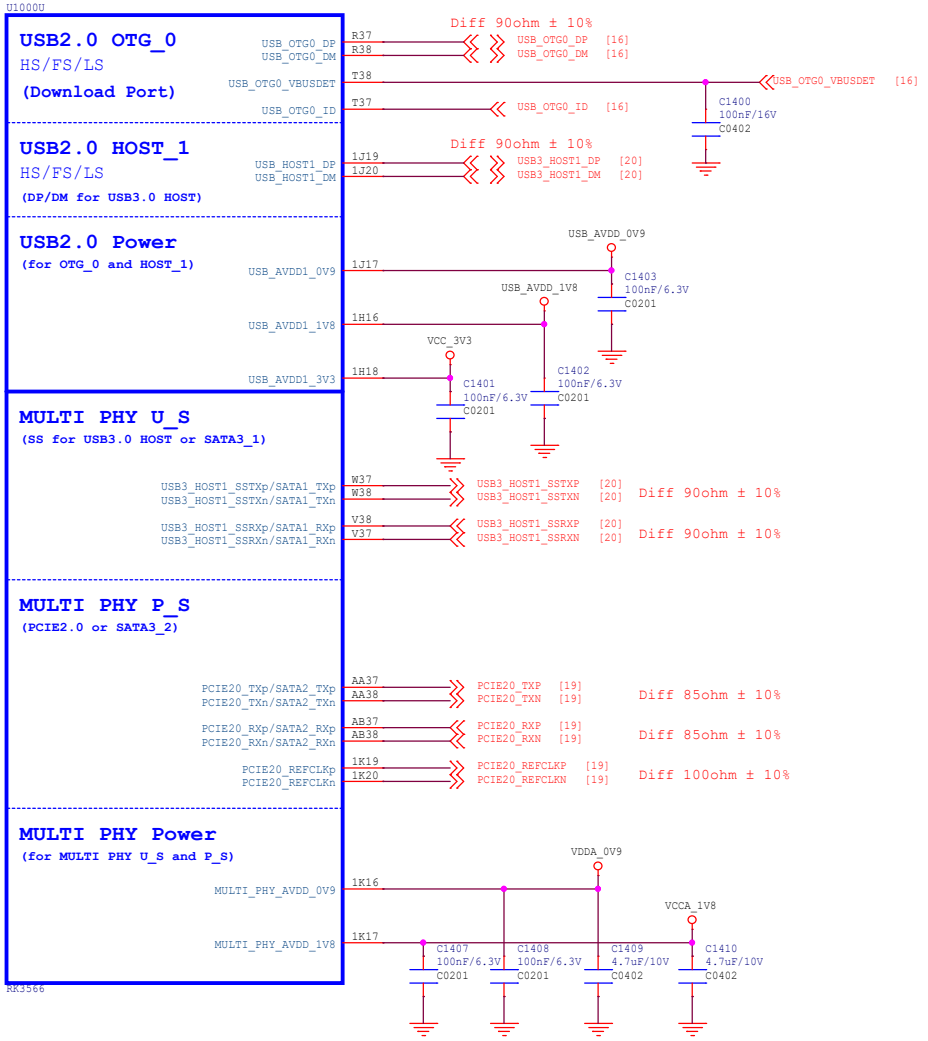
RK3566_J(VCCIO3 Domain)



RK3566_V(USB2.0 HOST)



RK3566_U(USB3.0/PCIe2.0x1/SATA)



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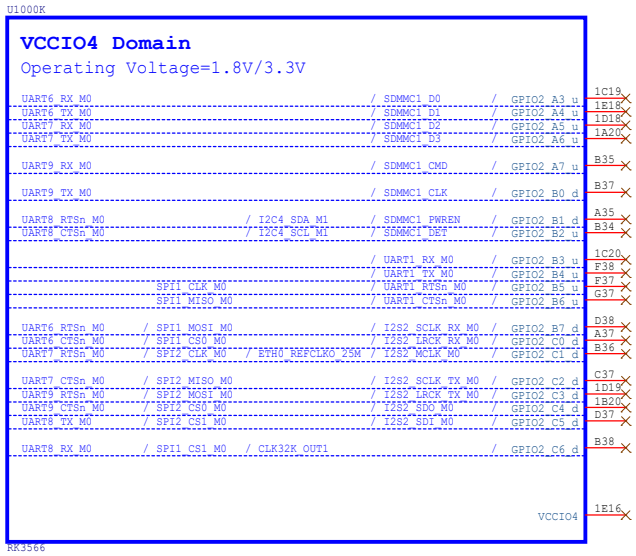
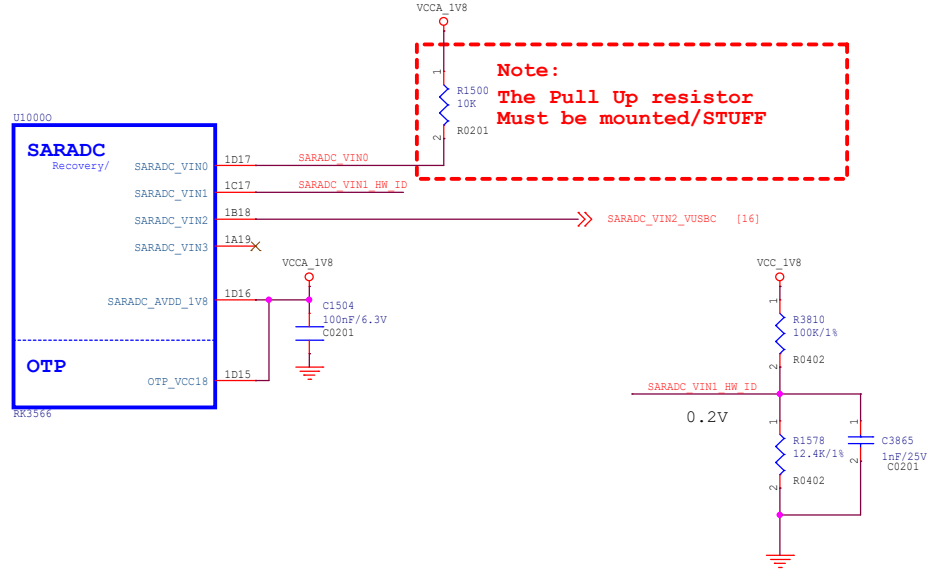
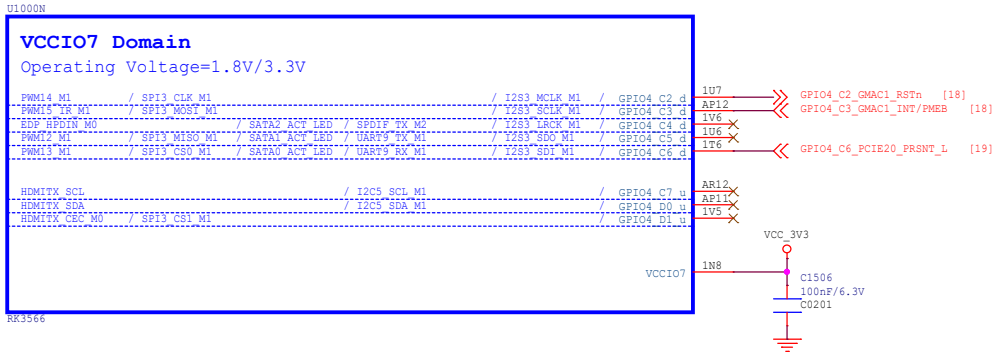
RK3566_K(VCCIO4 Domain)



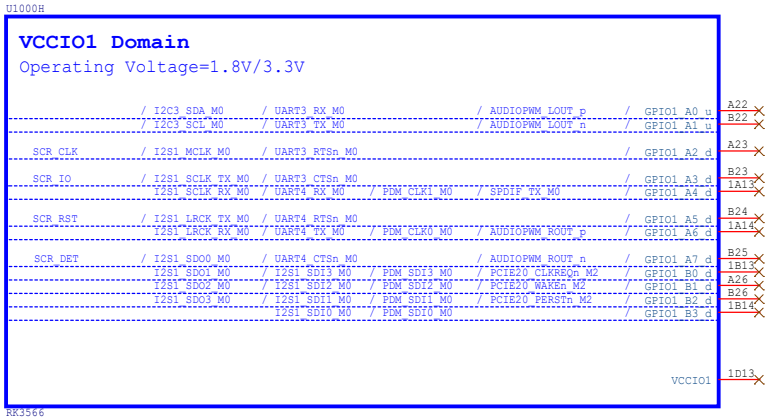
RK3566_O(SARADC/OTP)



RK3566_N(VCCIO7 Domain)



RK3566_H(VCCIO1 Domain)



软件dts的电压配置严格与硬件设计保持一致!
Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

VCCIO_ACODEC = 3.3V as default

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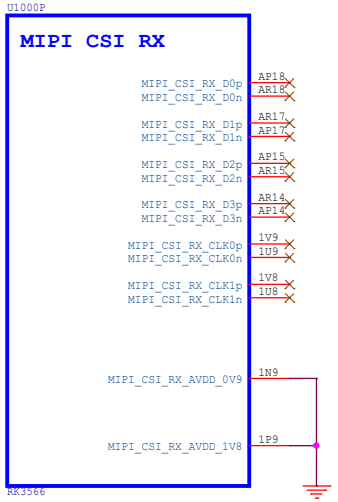
RK3566_P(MIPI_CSI_RX)



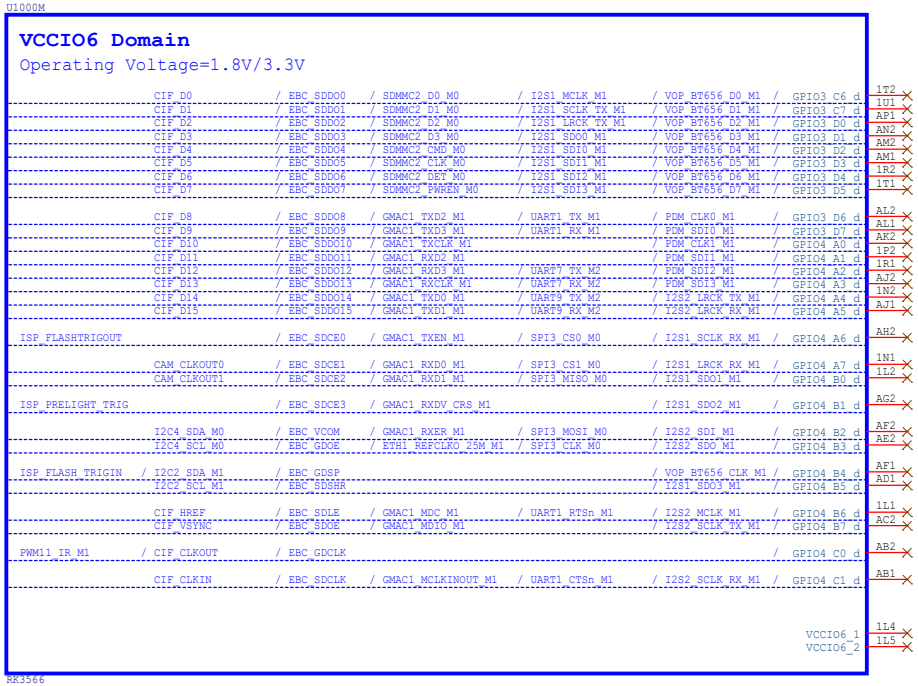
Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Usage of CIF Interface				
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

RK3566_M(VCCIO6 Domain)



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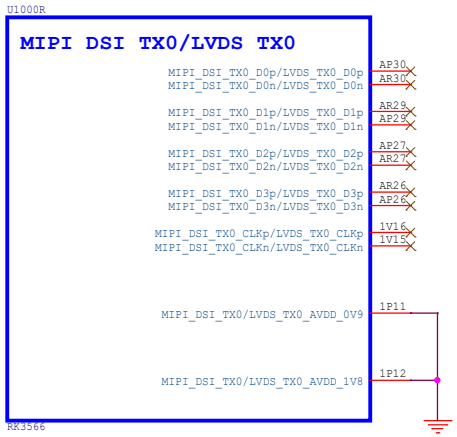
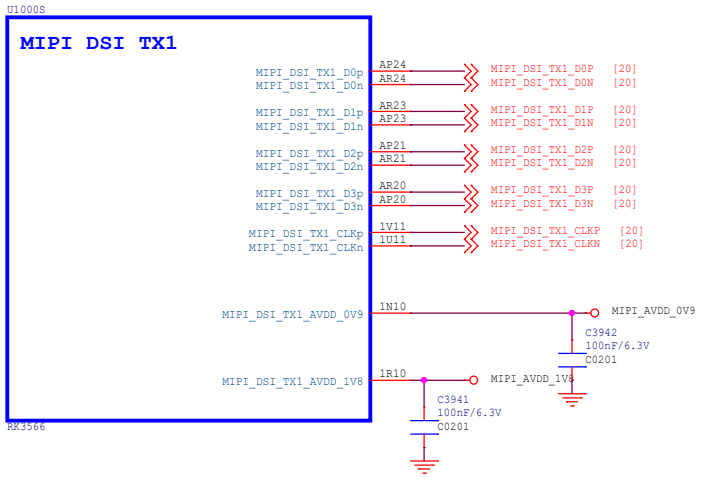
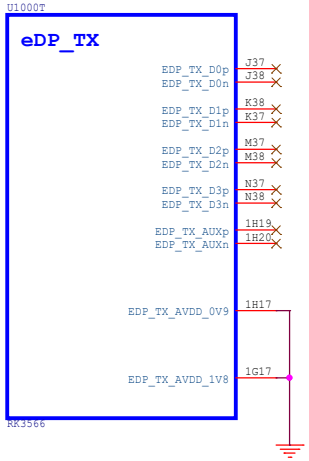
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



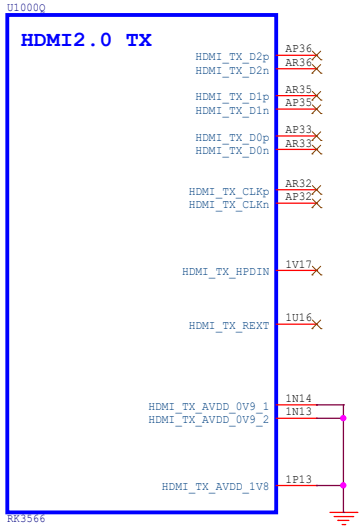
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



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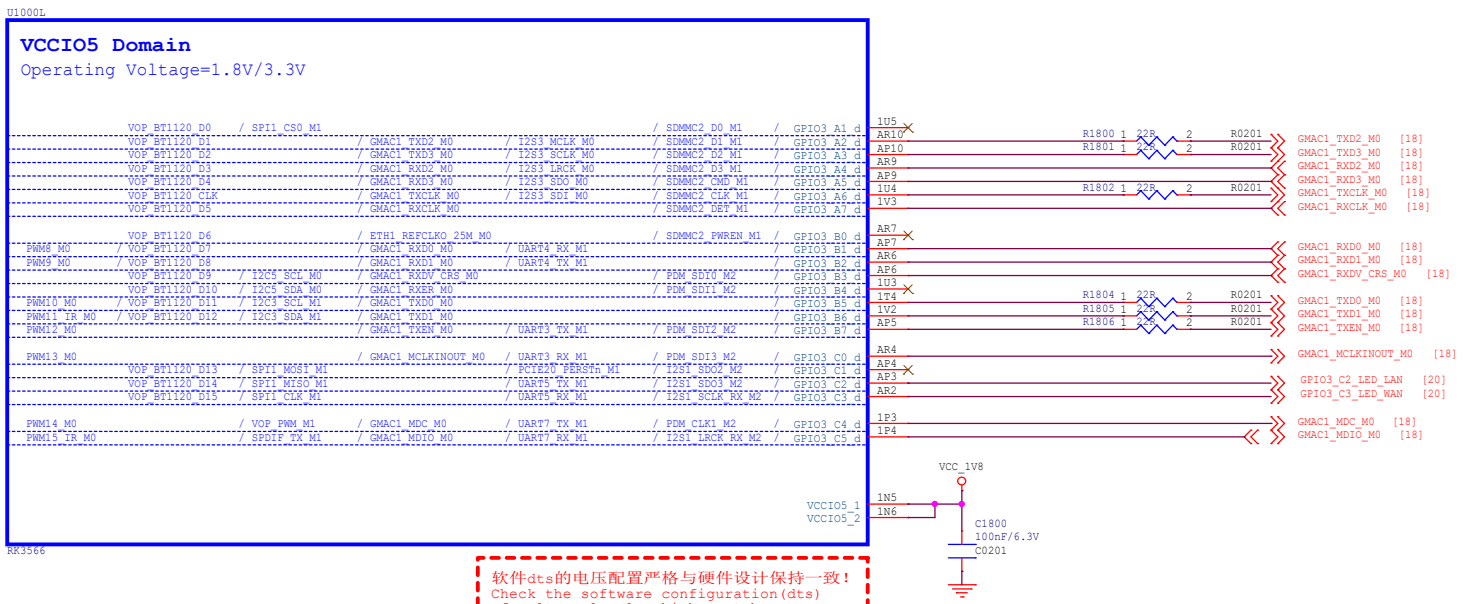
RK3566_L(VCCIO5 Domain)



软件dts的电压配置严格与硬件设计保持一致！
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------>	PHYx_TXD0	GMACx_TXD0	------>	PHYx_TXD0
GMACx_TXD1	------>	PHYx_TXD1	GMACx_TXD1	------>	PHYx_TXD1
GMACx_TXD2	------>	PHYx_TXD2			
GMACx_TXD3	------>	PHYx_TXD3			
GMACx_TXEN	------>	PHYx_TXEN	GMACx_TXEN	------>	PHYx_TXEN
GMACx_TXCLK	------>	PHYx_TXCLK			
GMACx_RXD0	<------	PHYx_RXD0	GMACx_RXD0	<------	PHYx_RXD0
GMACx_RXD1	<------	PHYx_RXD1	GMACx_RXD1	<------	PHYx_RXD1
GMACx_RXD2	<------	PHYx_RXD2			
GMACx_RXD3	<------	PHYx_RXD3			
GMACx_RXDV	<------	PHYx_RXDV	GMACx_RXDV	<------	PHYx_CRS_DV
GMACx_RXCLK	<------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<------	PHYx_RXER
GMACx_MDC	------>	PHYx_MDC	GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<------>	PHYx_MDIO	GMACx_MDIO	<------>	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx_XTALIN			
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125 (Option)	GMACx_MCLKINOUT	------>	PHYx_XTALIN/REFCLK
GPIO	------>	PHYx_RSTn	GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB	GPIO	<------	PHYx_INT/PMEB

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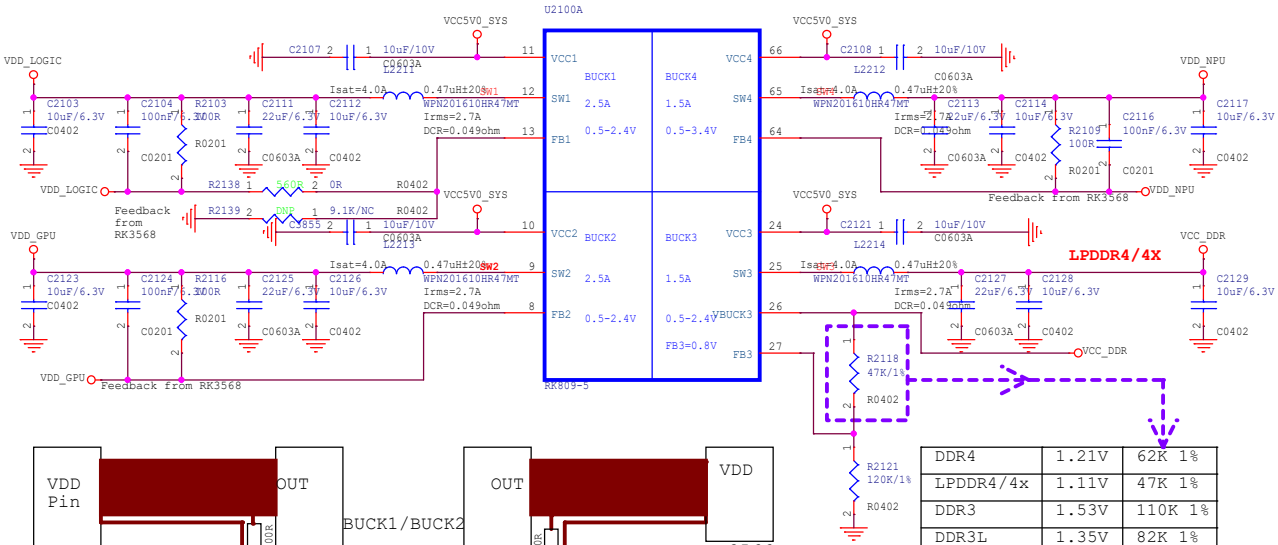
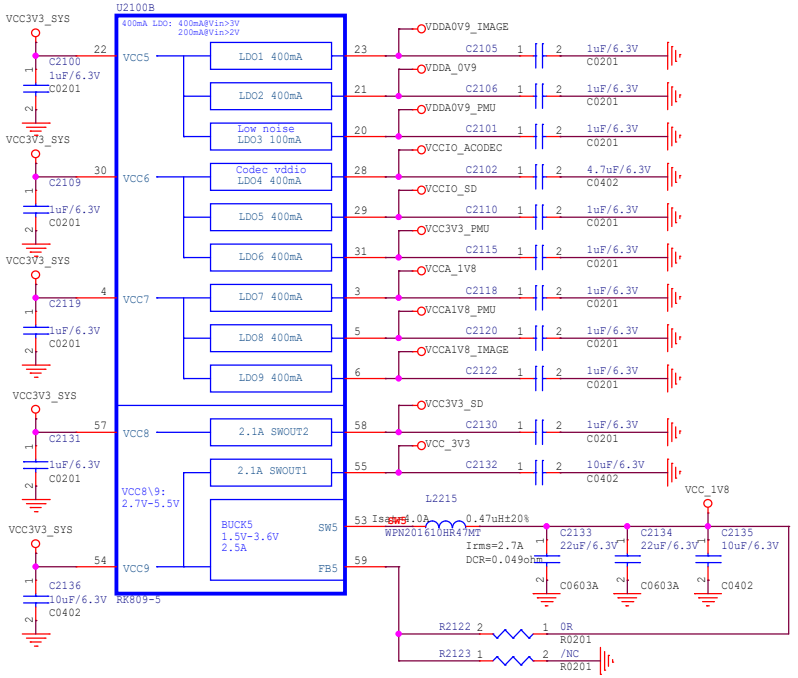
PMIC RK809 DCDC

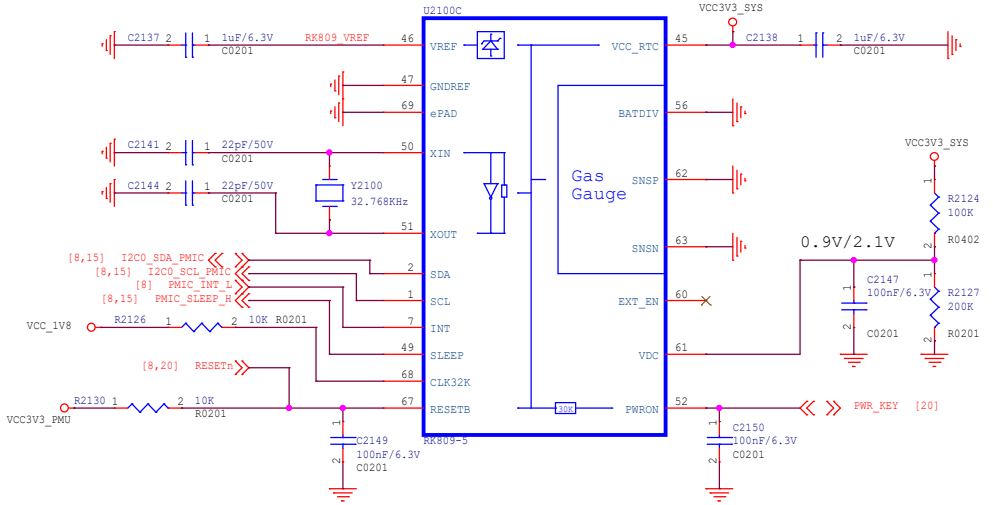


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

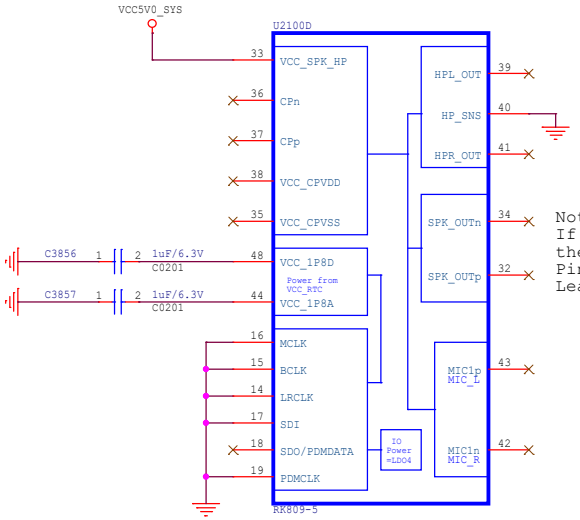
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC



Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

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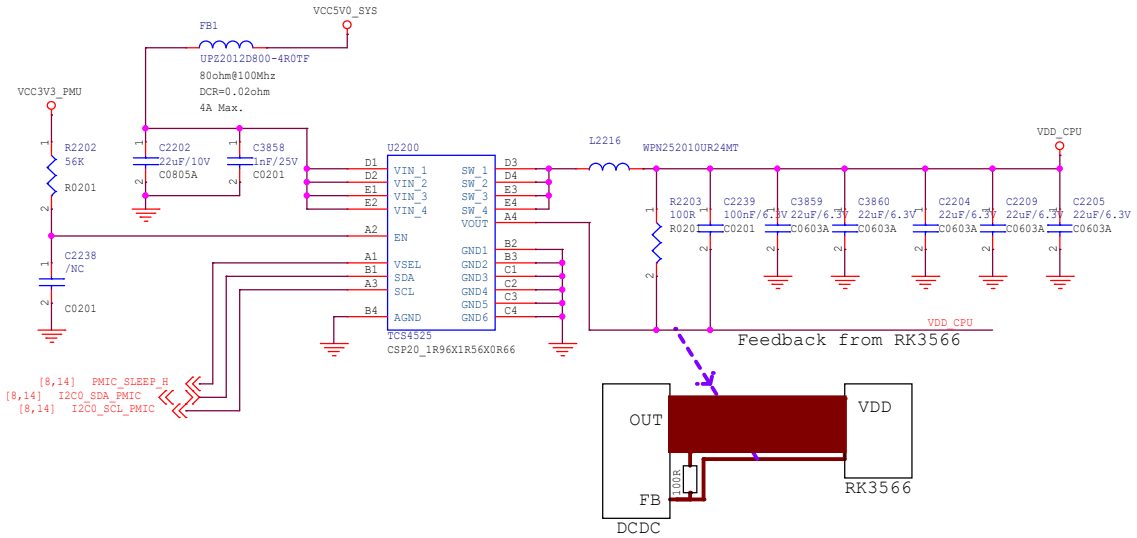
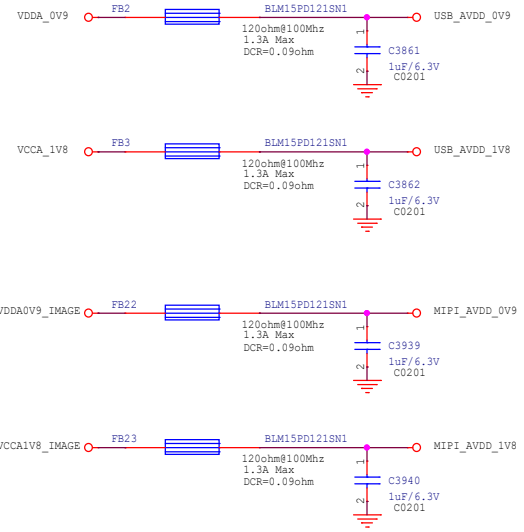
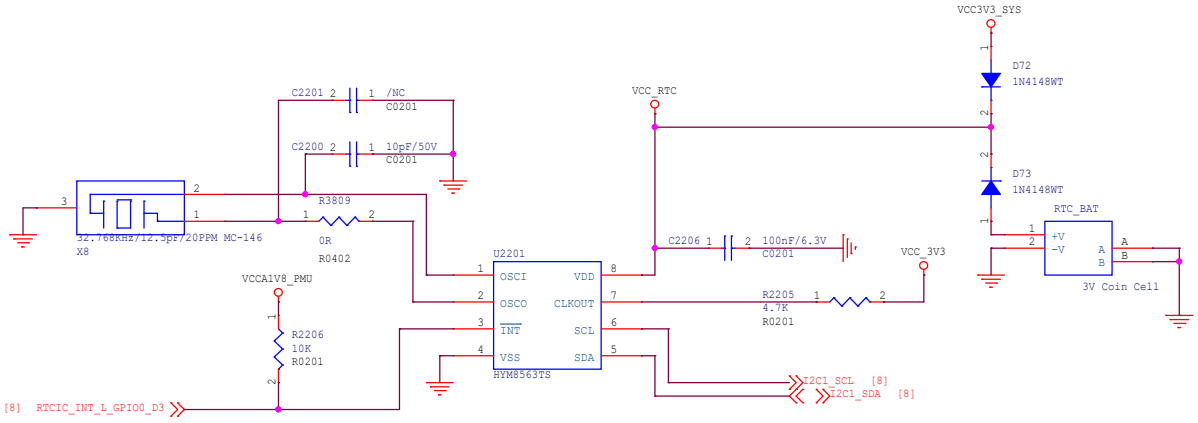
VDD_CPU



VDD_USB

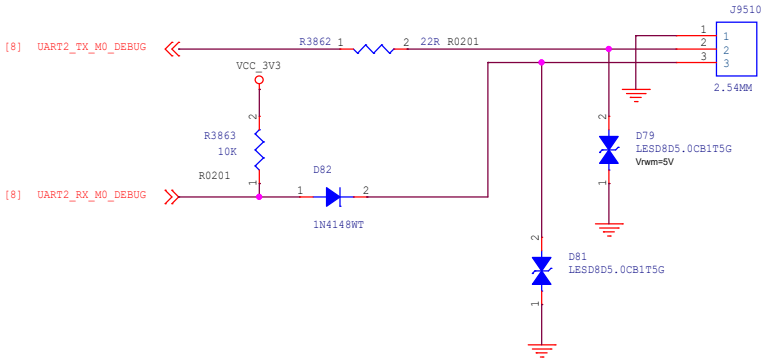


RTC



Address:Read A3H, Write A2H
7bit address: 0x51

Debug UART



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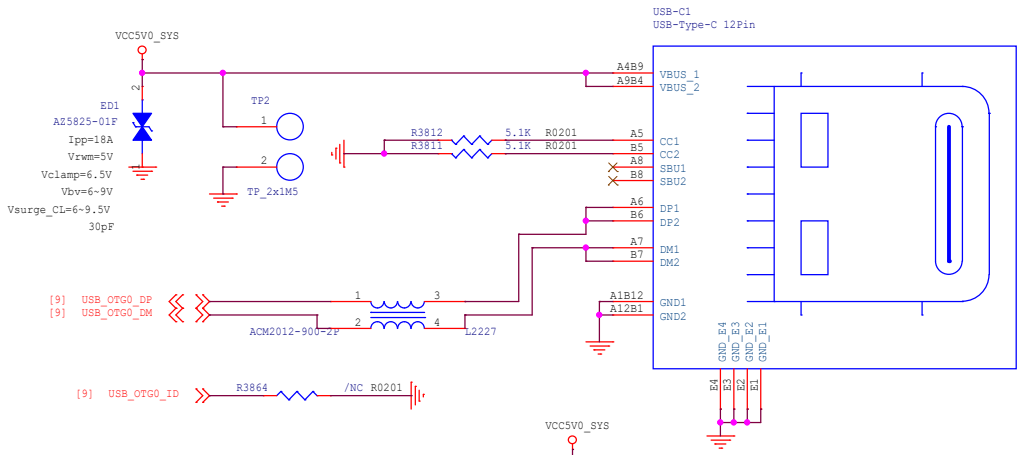
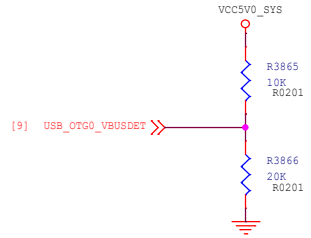
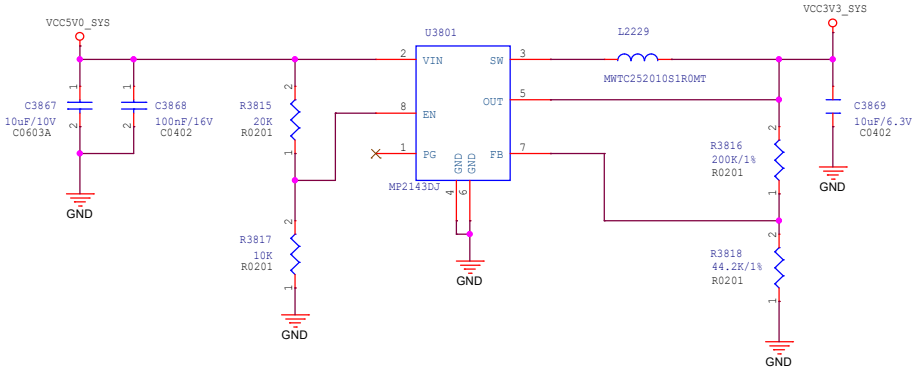
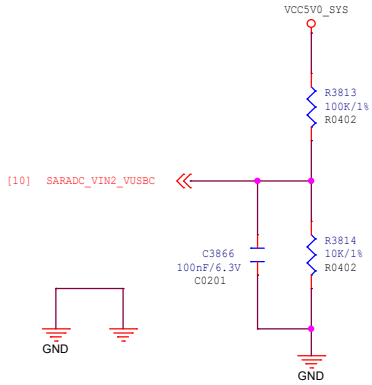
Power IN









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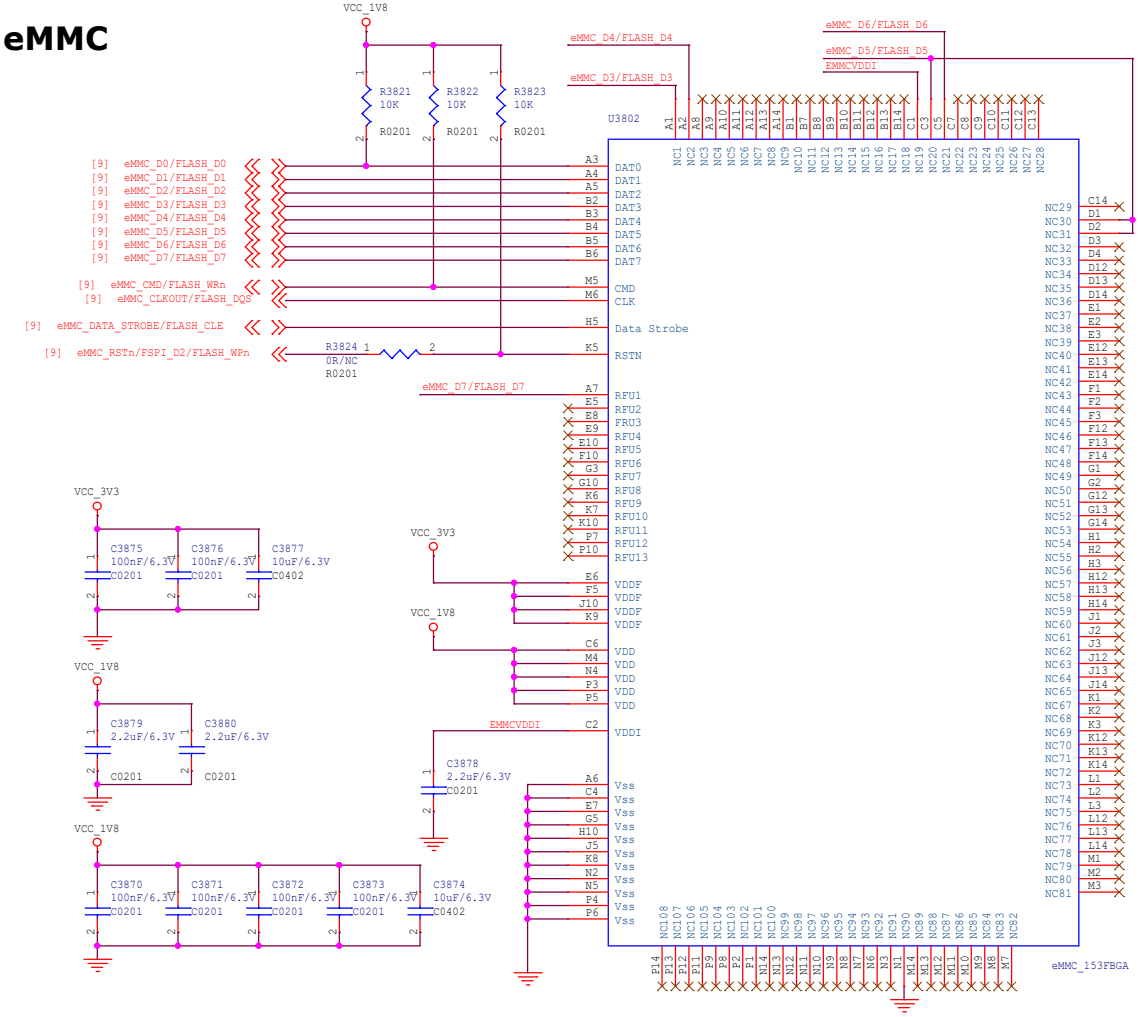
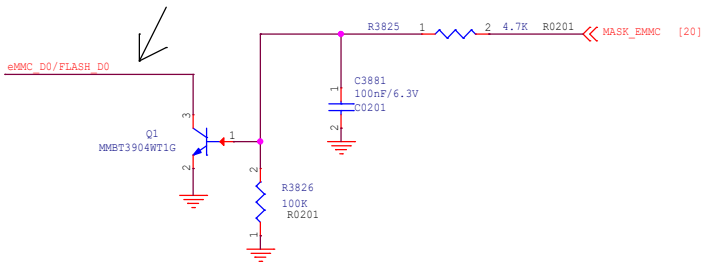
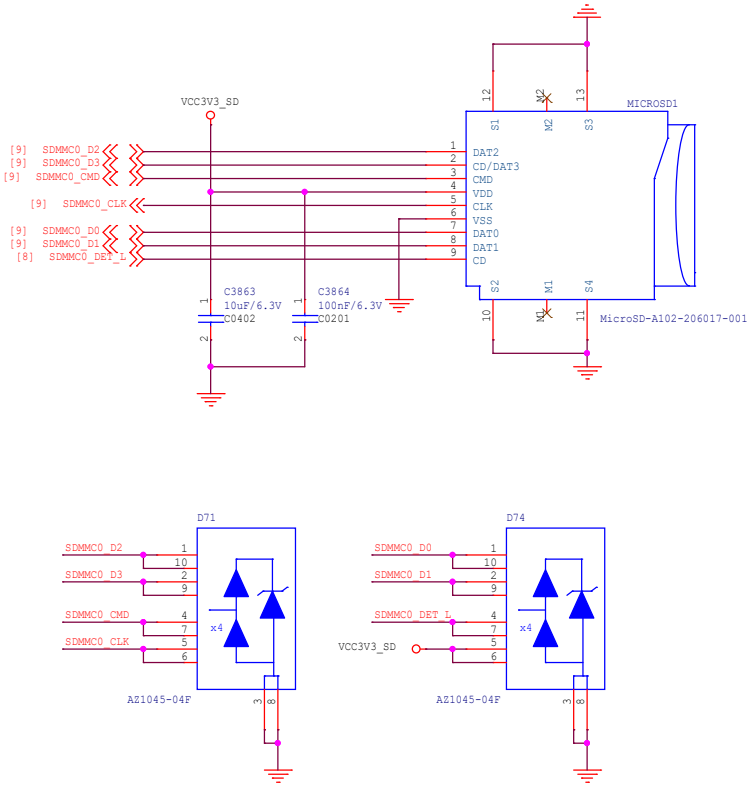
eMMC



Stub as short as possible



microSD



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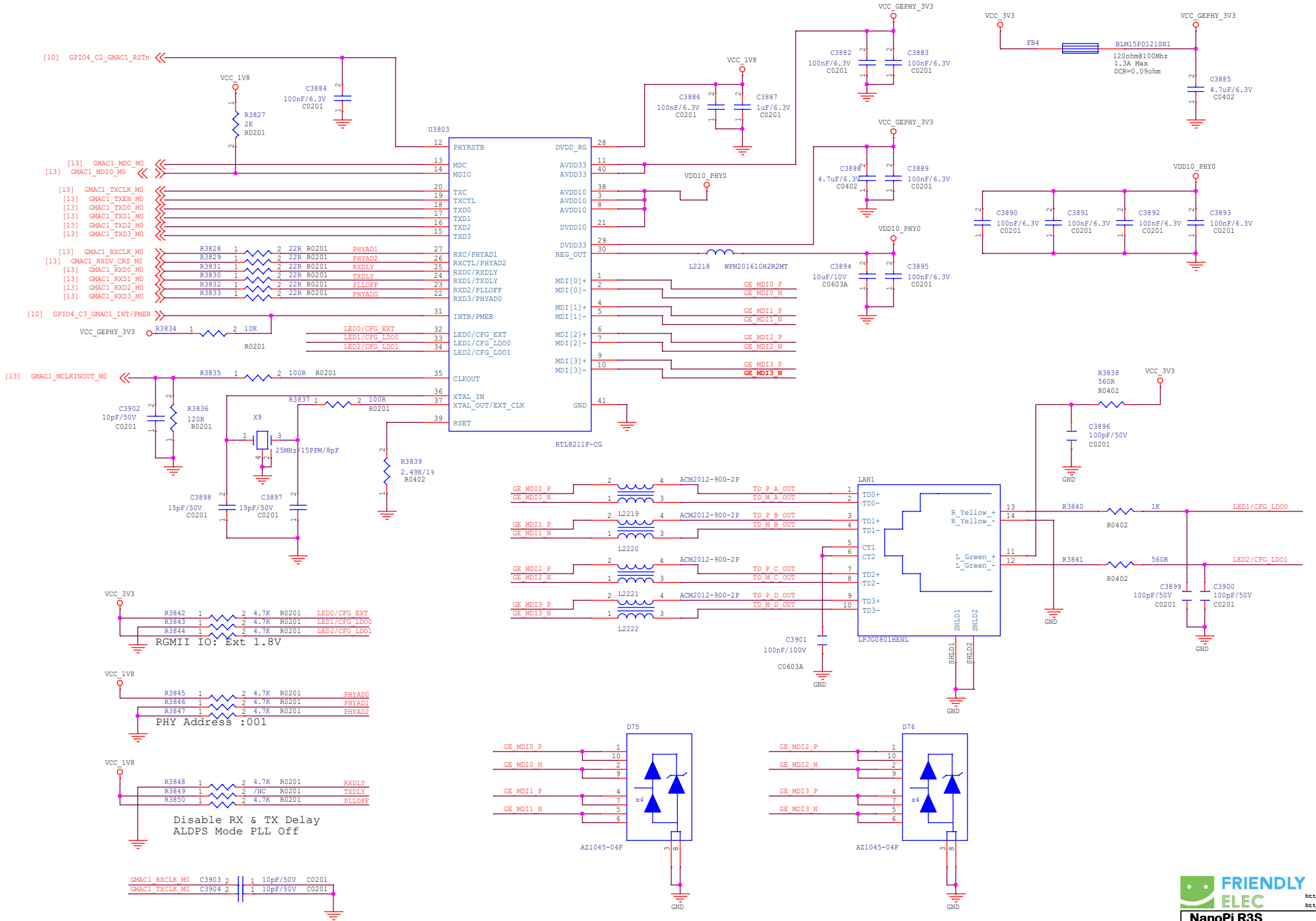
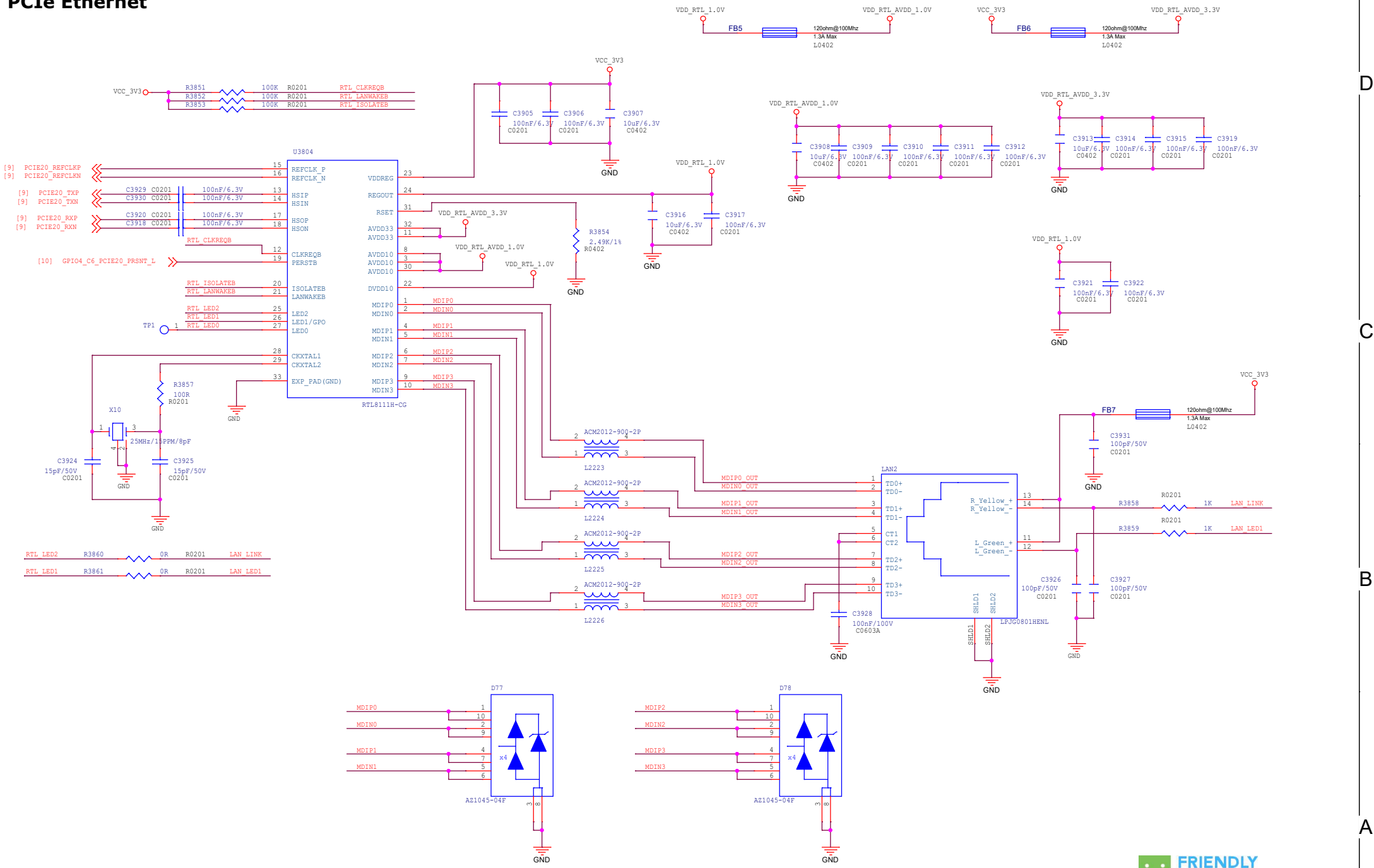
GMAC Ethernet



PCIe Ethernet



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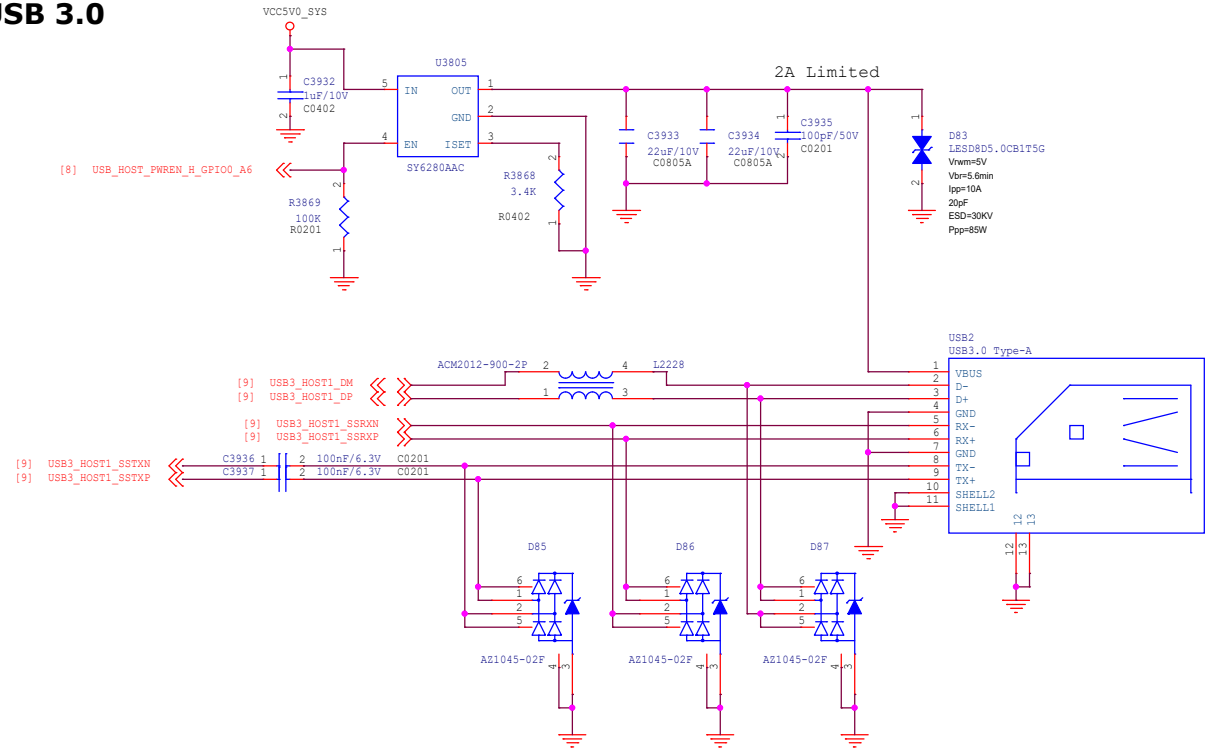
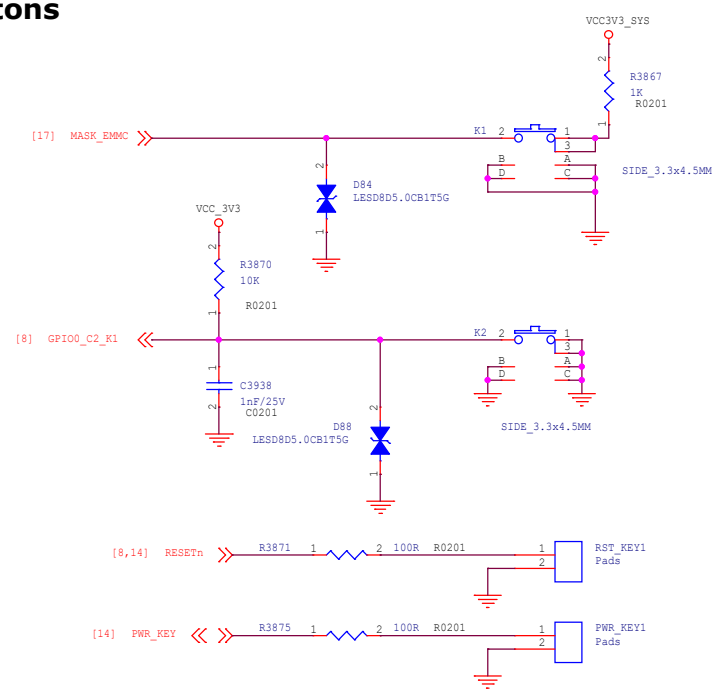
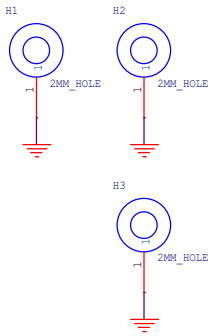
USB 3.0



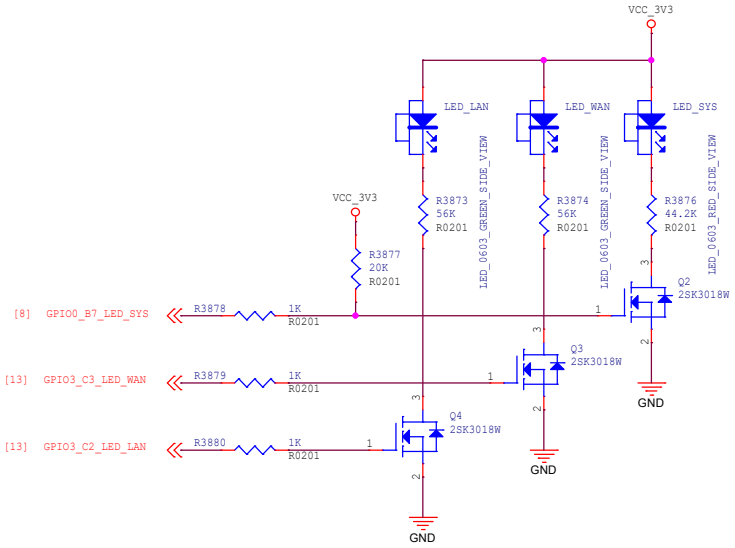
Buttons



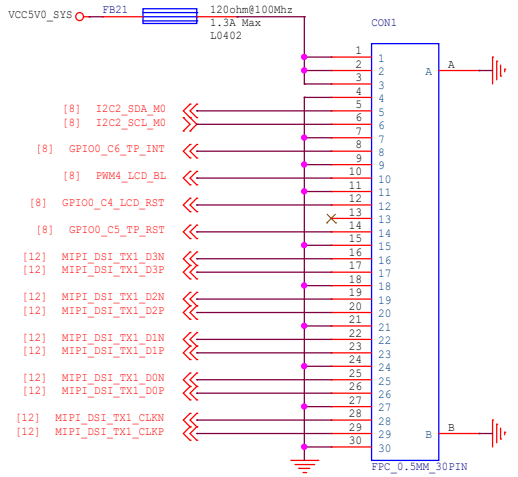
Screw Holes



LEDs



MIPI LCD



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