

# Rockchip RK3528A Datasheet

## Revision History

| Date       | Revision | Description                                   |
|------------|----------|---|
| 2024-04-10 | 1.2      | Update the description about HDMI and LPDDR4X |
| 2024-01-03 | 1.1      | Update the description about DDR and USB      |
| 2023-07-12 | 1.0      | Initial release                               |

**Table of Content**

Table of Content .....2

Figure Index .....3

Table Index.....4

Warranty Disclaimer.....5

Chapter 1 Introduction ..... 5

    1.1 Overview .....6

    1.2 Features .....6

    1.3 Block Diagram ..... 15

Chapter 2 Package Information.....16

    2.1 Order Information ..... 16

    2.2 Top Marking ..... 16

    2.3 Package Dimension ..... 16

    2.4 MSL Information ..... 18

    2.5 Lead Finish/Ball Material Information ..... 18

    2.6 Pin Number List ..... 18

Chapter 3 Electrical Specification .....24

    3.1 Absolute Ratings ..... 24

    3.2 Recommended Operating Conditions ..... 24

    3.3 DC Characteristics ..... 25

    3.4 Electrical Characteristics for General IO ..... 25

    3.5 Electrical Characteristics for PLL ..... 26

    3.6 Electrical Characteristics for USB2.0 Interface ..... 26

    3.7 Electrical Characteristics for HDMI ..... 27

    3.8 Electrical Characteristics for Audio CODEC interface ..... 27

    3.9 Electrical Characteristics for SARADC ..... 28

    3.10 Electrical Characteristics for TSADC..... 28

Chapter 4 Thermal Management.....29

    4.1 Overview ..... 29

    4.2 Package Thermal Characteristics ..... 29

**Figure Index**

Fig.1-1 Block Diagram ..... 15  
Fig.2-1 Package Definition ..... 16  
Fig.2-2 Package Top View ..... 16  
Fig.2-3 Package Bottom View ..... 17  
Fig.2-4 Package Side View ..... 18  
Fig.2-5 Package Dimension ..... 18

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**Table Index**

Table 2-1 Pin Number Order Information ..... 18

Table 3-1 Absolute Ratings ..... 24

Table 3-2 Recommended Operating Conditions ..... 24

Table 3-3 DC Characteristics ..... 25

Table 3-4 Electrical Characteristics for Digital General IO ..... 25

Table 3-5 Electrical Characteristics for INT PLL ..... 26

Table 3-6 Electrical Characteristics for FRAC PLL ..... 26

Table 3-7 Electrical Characteristics for USB2.0 Interface ..... 26

Table 3-8 Electrical Characteristics for HDMI ..... 27

Table 3-9 Electrical Characteristics for Audio CODEC ..... 27

Table 3-10 Electrical Characteristics for SARADC ..... 28

Table 3-11 Electrical Characteristics for TSADC ..... 28

Table 4-1 Thermal Resistance Characteristics ..... 29

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## Chapter 1 Introduction

### 1.1 Overview

RK3528A is a high performance Quad-core application processor designed for Smart IPTV/OTT/DBS and high-end multimedia application. It is a high integration and cost efficient SOC for 4K video application.

Quad-core Cortex-A53 is integrated with separate Neon and FPU coprocessor, also with shared L2 Cache to enhance system performance.

ARM Mali-450 GPU supports high-resolution display and game. It handles graphics programs like OpenGL ES1.1/2.0, OpenVG.

Dedicated ARM TrustZone based secure system to handle safety management for video and display applications. It includes crypto, rng, firewall engine to guarantee the whole system's security.

32-bit DRAM interface providing high bandwidth DDR3(L)/LPDDR3/DDR4/LPDDR4 support.

The advanced video decoder supports 60fps playback of 4K ultra-high-definition video with up to 10-bit pixels. It supports H.265, H.264, AVS2, etc. video standards.

The advanced video encoder also supports 60fps capture of 1080p high-definition video. It supports H.265 and H.264 encoding.

Display controller supports flexible surface and output stream. Outputs include two outputs switchable between HDMI 2.0 transmitter with HDR, CEC, HDCP2.2 support and CVBS.

In addition to these major elements, RK3528A processors have a broad range of peripheral interfaces like pcie2, usb2, mac, i2s, etc. to enable communication with wireless baseband, other communications peripherals, audio codec, power management, and mass storage.

### 1.2 Features

#### 1.2.1 Application Processor

- Quad core ARM Cortex-A53
- Full implementation of the ARM v8-A architecture.
- Separately Integrated Neon and FPU
- TrustZone Extension support
- One isolated voltage domain to support DVFS

#### 1.2.2 Graphic Processor

- ARM Mali-450 GPU
- Concurrent multi-core processing
- Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support
- One isolated voltage domain to support DVFS

#### 1.2.3 Memory Organization

- Internal on-chip memory
  - BootRom
    - ◆ Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
    - ◆ Support system code download by the following interface:

- USB interface
  - 64KB Share Memory
  - 8KB PMU SRAM
- External off-chip memory
  - eMMC Interface
    - ◆ Fully compliant with JEDEC eMMC5.1 specification
    - ◆ Support HS400, support CMD Queue
    - ◆ Support three data bus width: 1bit, 4bits or 8bits
  - SD/MMC Interface
    - ◆ Compatible with SD3.0, MMC ver4.51
    - ◆ Data bus width is 4bits
  - Flexible Serial Flash Interface (FSPI)
    - ◆ Support transfer data from/to serial flash device
    - ◆ Support 1bit, 2bits or 4bits data bus width
- Dynamic Memory Interface : DDR3(L)/LPDDR3/DDR4/LPDDR4/LPDDR4X
  - Compatible with JEDEC standard DDR3-2133/DDR3L-2133/LPDDR3-2133/DDR4-2400/LPDDR4(X)-2400 SDRAM
  - Supports 32 Bits data width, 4GB addressing space

### 1.2.4 System Component

- MCU
  - Cortex-M0 in PMU domain integrate 8KB TCM.
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 5 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 4 separate voltage domains, VDD\_ARM,VDD\_GPU,VDD\_LOGIC,VDD\_PMU.
- Timer
  - Support 2 secure timers with 64bits counter and interrupt-based operation
  - Support 6 non-secure timers with 64bits counter and interrupt-based operation
  - Support 1 high precision timer.
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable
- PWM
  - Support 8 on-chip PWMs (PWM0~PWM7) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3, PWM7
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:

- ◆ Generate a system reset
- ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- One Watchdog for non-secure application
- One Watchdog for secure application
- One Watchdog for MCU
- Interrupt Controller
  - Support 256 SPI interrupt sources input from different components inside RK3528A
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive or rising edge sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming-based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - Totally three embedded DMA controllers for peripheral system
  - Each DMAC features:
    - ◆ Support 8 channels
    - ◆ 32 hardware requests from peripherals
    - ◆ 2 interrupt output
    - ◆ Support TrustZone technology and programmable secure state for each DMA channel
- Secure System
  - Embedded one cipher engines
    - ◆ Support Link List Item (LLI) DMA transfer
    - ◆ Support SHA-1, SHA-256/224, MD5, SM3 with hardware padding
    - ◆ Support HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
    - ◆ Support AES-128, AES-192, AES-256 encrypt and decrypt cipher
    - ◆ Support DES and TDES cipher
    - ◆ Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/GCM/CBC-MAC/CMAC mode
    - ◆ Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/GCM/CBC-MAC/CMAC mode
    - ◆ Support DES/TDES ECB/CBC/OFB/CFB mode
    - ◆ Support up to 4096 bits PKA mathematical operations for RSA
    - ◆ Support SM2/SM3/SM4 cipher
  - Support generating random numbers, one secure only engine, another one security configurable
  - Support secure OTP
  - Support secure debug
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM (share memory), security programmable.
  - External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master
- Mailbox
  - One Mailbox in SoC to service CPU and MCU communication
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is



occupied

### 1.2.5 Video CODEC

- Video Decoder
  - Real-time video decoder of
    - ◆ MPEG-1, MPEG-2, MPEG-4
    - ◆ H.263, H.264/AVC, H.265/HEVC, MVC
    - ◆ VC-1
    - ◆ AVS, AVS+,AVS2
  - MMU Embedded
  - Supports frame timeout interrupt, frame finish interrupt and bit stream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format YUV420 semi-planar, YUV400(monochrome), YUV422 is supported by H.264
  - H.264/AVC BP/MP/HP profile @ level 5.1; H.264/AVC MVC; up to 4Kx2K @ 60fps
  - H.265/HEVC Main/Main10 profile @ level 5.1 High-tier; up to 4Kx2K @ 60fps
  - AVS2 4KX2K @60fps
  - MPEG-1, Main profile, up to 1080P @ 60fps
  - MPEG-2, SP@ML, MP@HL, up to 1080P @ 60fps
  - MPEG-4, ASP profile @ level 5, up to 1080P @ 60fps
  - AVS, Jizhun profile @ level 6.0; up to 1080P @ 60fps
  - AVS-P16 (AVS+), up to 1080P @ 60fps
  - H.263, up to 576P @ 60fps
  - VC-1, SP@ML, MP@HL, AP@L0-3, up to 1080P @ 60fps
- Video Encoder
  - Support video encoder for H.264, HP@level4.2
  - H.264 maximum frame rate is up to 1920x1080 @60fps
  - Capable of encoding HEVC Main Profile @ L4.1 High-tier
  - H.265 resolution and frame rate are up to 1920x1080 @60fps
  - JPEG encoder included

### 1.2.6 JPEG Decoder

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate is up to 76million pixels per second

### 1.2.7 Image Enhancement (VDPP module)

- Image format support
  - Input data: YUV420/YUV422
  - Output data: YUV420/YUV422/YUV444
  - YUV swap
  - UV SP/P
  - BT601\_l/BT601\_f/BT709\_l/BT709\_f color space conversion
  - YUV up/down sampling
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configured high frequency de-interlace
  - I4O2 (Input 4 field, output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Post-Processing
  - Support DMSR
  - Support ZME(polyphaser filter based zoom in/zoom out)

### 1.2.8 2D Graphics Engine

- 2D Graphics Engine:
  - Source formats:
    - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
    - ◆ RGB888, RGB565
    - ◆ RGBA5551, RGBA4444
    - ◆ YUV420 planar, YUV420 semi-planar
    - ◆ YUV422 planar, YUV422 semi-planar
    - ◆ YUV 10-bit for YUV420/422 semi-planar
    - ◆ BPP8, BPP4, BPP2, BPP1
  - Destination formats:
    - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
    - ◆ RGB888, RGB565
    - ◆ RGBA5551, RGBA4444
    - ◆ YUV420 planar, YUV420 semi-planar
    - ◆ YUV422 planar, YUV422 semi-planar
  - Pixel Format conversion, BT.601/BT.709
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - BitBLT
    - ◆ Two source BitBLT:
      - ◆ A+B=B only BitBLT, A support rotate and scale when B fixed
      - ◆ A+B=C second source (B) has same attribute with (C) plus rotation function
  - Color fill with gradient fill, and pattern fill
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - New comprehensive per-pixel alpha (color/alpha channel separately)
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, pattern mask, fading
  - Dither operation
  - 0, 90, 180 and 270-degree rotation
  - x-mirror and y-mirror rotation operation

### 1.2.9 Video Output Processor

- Video ports
  - Video Port0, max output resolution: 4096x2304@60Hz
  - Video Port1, max output resolution: 720x576@60Hz
- Cluster
  - Max input and output resolution 4096x2304
  - Support AFBCD
  - Support RGB/YUV/YUYV format
  - Support scale up/down
  - Support rotation
- ESMART 0/1/2/3
  - Max input resolution 2048x2160 and output resolution 4096x2304
  - Support RGB/YUV/YUYV format
  - Support scale up/down
  - Support 4 regions
- Overlay
  - Support up to 4-layer overlay for port0 and 2-layer overlay for port1
  - Support RGB/YUV domain overlay
  - Support HDR
    - ◆ Support HDR10
    - ◆ Support SDR2HLG
    - ◆ Support HDR VIVID
    - ◆ Support HLG
- Write back
  - Format: XRGB8888/RGB888/RGB565/YUV420
  - Max resolution: 1920x1080

### 1.2.10 Display Interface

- HDMI
  - Compliant with HDMI 2.0b
  - Support YUV440 4k x 2k @ 60fps
  - Support for 4k x 2k and 3D video formats
  - Support for up to 18Gbps bandwidth
  - HPD input analog comparator
  - Compliance HDMI compliance Test specification 1.4 and 2.x
  - Support HDCP 1.4 and 2.2
- CVBS
  - BT656 decoder
    - ◆ Support for interlace output
  - TV interface
    - ◆ TV encoder 10bit out for DAC
    - ◆ Up sample to 27MHz/108MHz
  - Resolution
    - ◆ PAL/NTSC
  - VDAC
    - ◆ 10-bit 1-channel current-steering DAC
    - ◆ Up to 300MHz update rate
    - ◆ Support single-ended or differential output
    - ◆ Programmable current output range: 0~34.7mA
    - ◆ 58dBc SFDR @Iout = 18.7mA, fclk = 300MHz and fout = 2MHz;
    - ◆ 55dBc SFDR @Iout = 26.7mA, fclk = 300MHz and fout = 2MHz;
    - ◆ DNL<1LSB, 1NL<2LSB
    - ◆ Support cable detection
    - ◆ Support BIST logic
    - ◆ APB slave interface for internal register access
    - ◆ Build-in bandgap reference
    - ◆ 1.8V IO supply and 0.9V core supply

### 1.2.11 Audio Interface

- SAI(Serial Audio Interface):
  - SAI0/SAI2 with 2 channel
    - ◆ Up to 2 channels for TX and 2 channels RX path
    - ◆ Audio resolution from 16bits to 32bits
    - ◆ Sample rate up to 192KHz
    - ◆ Provides master and slave work mode, software configurable
    - ◆ Support 3 I2S formats (normal, left-justified, right-justified)
    - ◆ Support 4 PCM formats (early, late1, late2, late3)
    - ◆ SAI and PCM cannot be used at the same time
    - ◆ SAI0 connect to GPIO
    - ◆ SAI2 connect to Audio CODEC, RX path not supported
  - SAI1/SAI3 with 8 channel
    - ◆ Up to 8 channels TX and 8 channels RX path
    - ◆ Audio resolution from 16bits to 32bits
    - ◆ Sample rate up to 192KHz
    - ◆ Provides master and slave work mode, software configurable
    - ◆ Support 3 I2S formats (normal, left-justified, right-justified)
    - ◆ SAI1 connect to GPIO
    - ◆ SAI3 connect to HDMI, RX path not supported
- PDM
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode

- SPDIF
  - SPDIF connect to HDMI and GPIO
- Audio CODEC
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz

### 1.2.12 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths
- TS interface
  - Supports 2 TS input channels.
  - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
  - Supports 2 TS sources: demodulators and local memory.
  - Supports 2 Built-in PTIs (Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
    - ◆ 96 PID filters.
    - ◆ TS descrambling with 8 sets of Control Word under CSA2.0 standard
    - ◆ 32 PES/ES filters with PTS/DTS extraction and ES start code detection.
    - ◆ 16 PCR extraction channels
    - ◆ 96 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
    - ◆ PID done and error interrupts for each channel
    - ◆ PCR/DTS/PTS extraction interrupt for each channel
  - Supports 1 PVR (Personal Video Recording) output channel.
  - 1 built-in multi-channel DMA Controller.
  - Support MMU
- Smart Card
  - Support ISO-7816
  - Support card activation and deactivation
  - Support cold/warm reset
  - Support Answer to Reset(ATR) response reception
  - Support T0 for asynchronous half-duplex character transmission
  - Support T1 for asynchronous half-duplex block transmission
  - Support automatic operating voltage class selection
  - Support adjustable clock rate and bit (baud) rate
  - Support configurable automatic byte repetition
- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode
  - 2 on-chip SPI controller
- UART Controller
  - 8 on-chip UART controller
  - DMA-based or interrupt-based operation
  - UART0/1/2Embedded two 64Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity

- Support different input clock for UART operation to get up to 4Mbps or another special baud rate
- Support non-integer clock divides for baud clock generation
- Support auto flow control mode
- I2C controller
  - 8 on-chip I2C controller
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
- MAC 10/100/1000 Ethernet Controller
  - Support 10/100/1000 Mbps data transfer rates with the RGMII interfaces
  - Support 10/100 Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
  - Support for TCP Segmentation Offload (TSO) and UDP Fragmentation Offload (UFO)
- MAC 10/100M Ethernet controller and MAC PHY
  - Support one Ethernet controllers
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation
- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Support One USB 2.0 Host
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- USB3.0
  - One Dual-Role-Device (DRD) USB Subsystem
  - Support USB3.0 (5Gbps ) stand, equal to USB3.1 Gen1, USB3.2 Gen1 or USB 5Gbps
  - Support USB2.0 (up to 480Mbps) stand
  - Compatible Specification
    - ◆ Universal Serial Bus 3.0 Specification, Revision 1.0
    - ◆ Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG\_2)
    - ◆ eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB3.0
  - Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  - LPM protocol in USB 2.0 and U0, U1, U2, and U3 states for USB3.0
  - USB3.0 Device Features
    - ◆ Up to 10 IN endpoints, including control endpoint 0
    - ◆ Up to 6 OUT endpoints, including control endpoint 0
    - ◆ Up to 16 endpoint transfer resources, each one for each endpoint
    - ◆ Flexible endpoint configuration for multiple applications/USB set-configuration modes
    - ◆ Hardware handles ERDY and burst
    - ◆ Stream-based bulk endpoints with controller automatically initiating data

- movement
  - ◆ Isochronous endpoints with isochronous data in data buffers
  - ◆ Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB3.0 xHCI Host Features
  - ◆ Support up to 64 devices
  - ◆ Support 1 interrupter
  - ◆ Support 1 USB2.0 port and 1 Super-Speed port
  - ◆ Support standard or open-source xHCI and class driver
- USB3.0 Dual-Role Device (DRD) Features
  - ◆ Static Device Operation
  - ◆ Static Host Operation
  - ◆ USB3.0/USB2.0 OTG A device and B device basing on ID
  - ◆ Not Support USB3.0/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  - ◆ USB2.0 PHY support Battery Charge detection
  - ◆ USB3.0 PHY combos with PCIE
- Multi-PHY Interface
  - Support multi-PHYs with PCIe2.1/USB3.0
  - One USB3 Host controller
  - One PCIe2.1 controller
  - USB 3.0 xHCI Host Controller
    - ◆ Support 1 USB2.0 port and 1 Super-Speed port
    - ◆ Concurrent USB3.0/USB2.0 traffic, up to 8.48Gbps bandwidth
    - ◆ Support standard or open-source xHCI and class driver
    - ◆ Static USB3.0 Device
    - ◆ Static USB3.0 xHCI host
    - ◆ USB3.0/USB2.0 OTG A device and B device basing on ID
  - PCIe2.1 interface
    - ◆ Compatible with PCI Express Base Specification Revision 3.0
    - ◆ Support Root Complex(RC) mode
    - ◆ Support 2.5Gbps and 5.0Gbps serial data transmission rate per lane per direction
    - ◆ Support one lane

### 1.2.13 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt to CPU
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
- HDMI 5V IO
  - 3.3V power supply, 5V voltage tolerance
  - 4 IOs for HDMI HPD/CEC/DDC connection
- Temperature Sensor(TS-ADC)
  - 10-bits ADC up to 50KS/s sampling rate
  - -40~125°C temperature range and 5°C temperature resolution
- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate

- 4 single-ended input channels
- Current consumption: 0.5mA @ 1MS/s
- OTP
  - Support 8192bits
  - Support Idle, Read, Program operation
  - Support boot function
  - Support Bist function
- Package Type
  - WBBGA401L (body:13.3mm x 13.5mm; ball size: 0.3mm; ball pitch: 0.65/0.6mm)

Notes :

① DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X are not used simultaneously

② Support 1x USB2 Host+1x USB2 Otg+ PCIE or 1x USB2 Host + 1x USB3.0

### 1.3 Block Diagram

The following figure shows the basic block diagram.

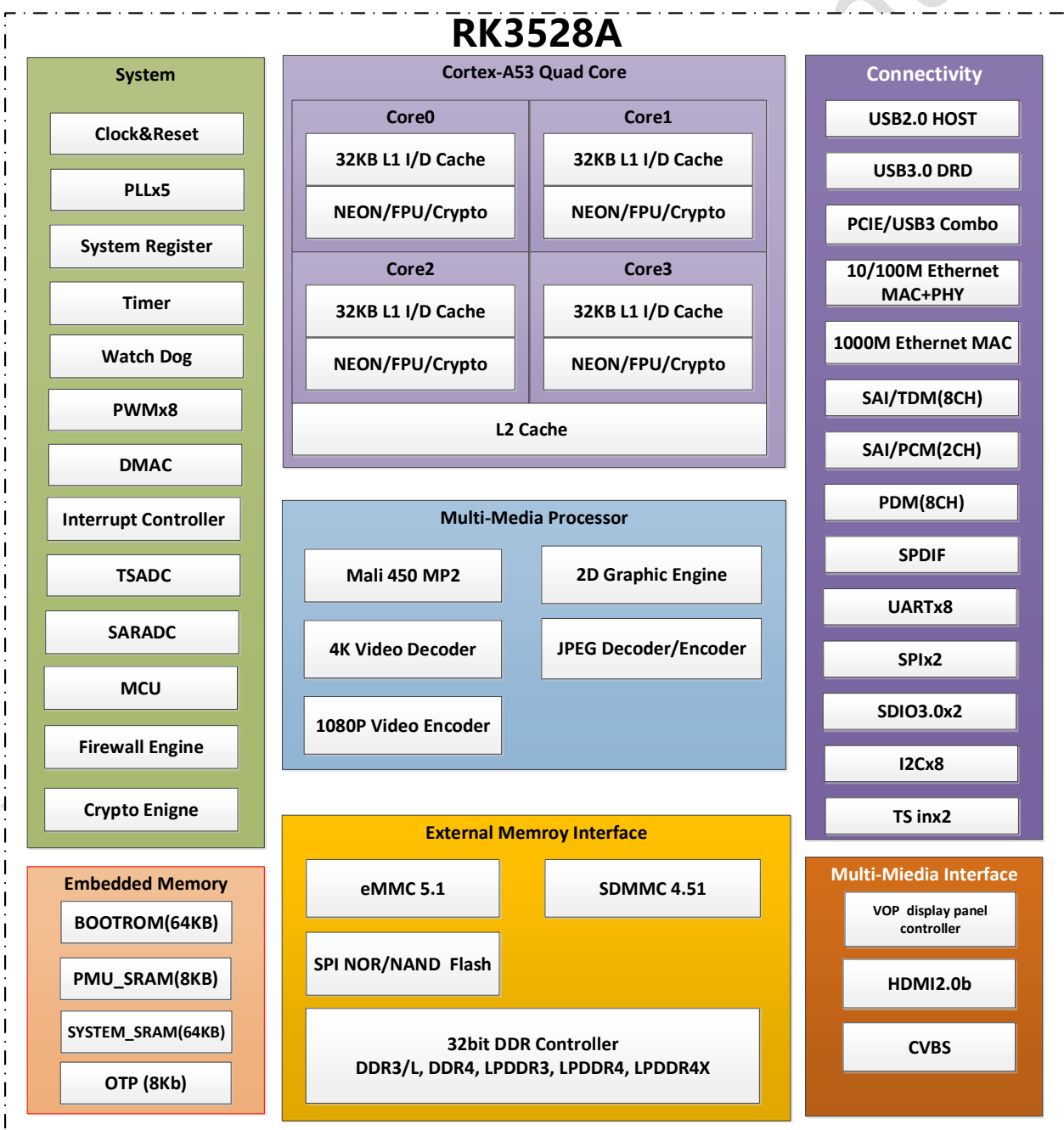


Fig.1-1 Block Diagram

## Chapter 2 Package Information

### 2.1 Order Information

| Orderable Device | RoHS status | Package   | Package Q'ty | Device Feature                  |
|------------------|-------------|-----------|--------------|---------------------------------|
| RK3528A          | RoHS        | WBBGA401L | 1190pcs      | Quad-core Application Processor |

### 2.2 Top Marking

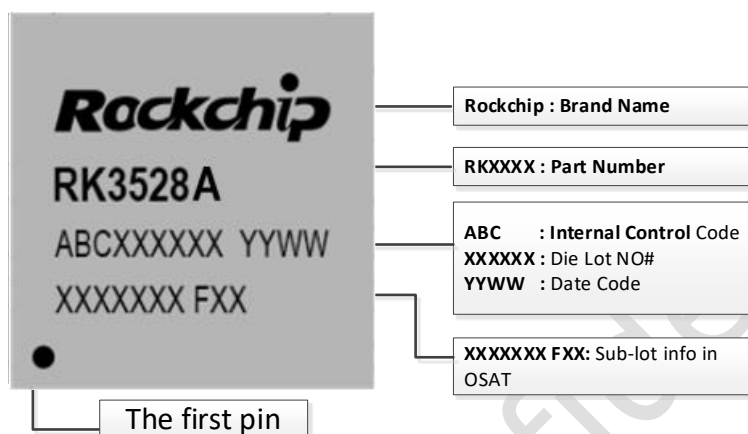


Fig.2-1 Package definition

### 2.3 Package Dimension

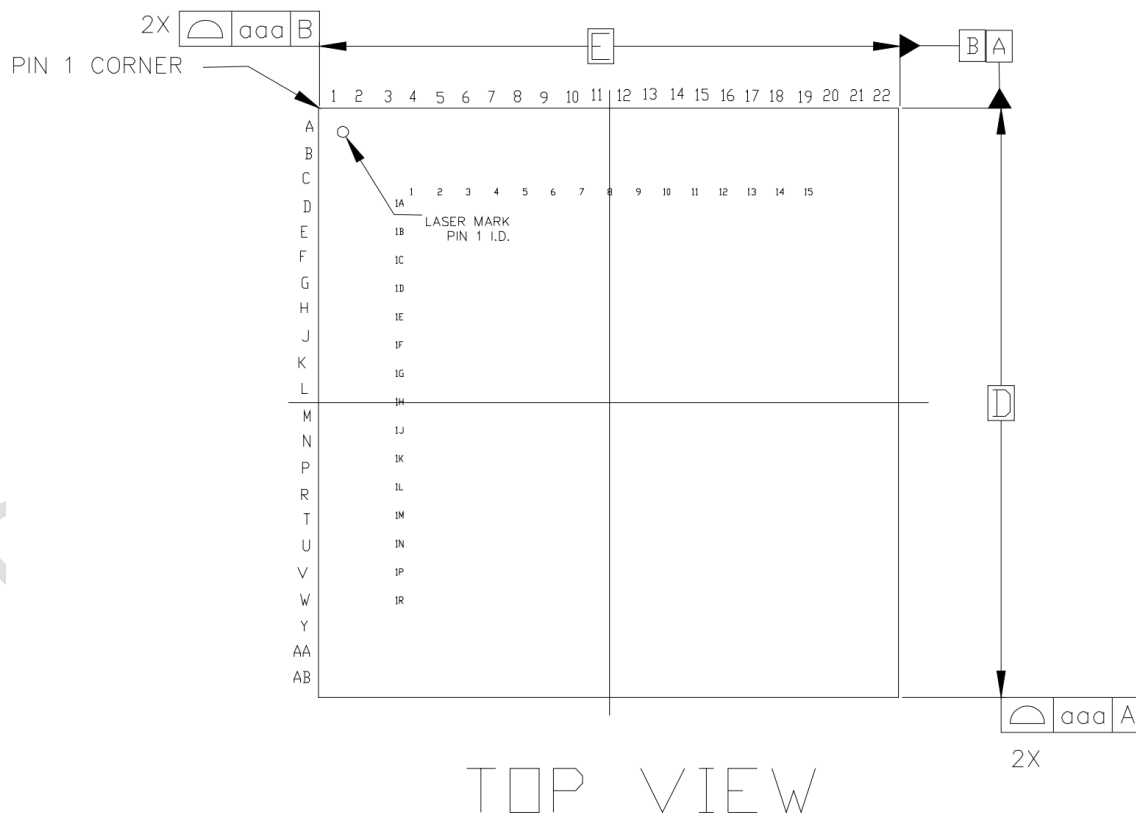


Fig.2-2 Package Top View



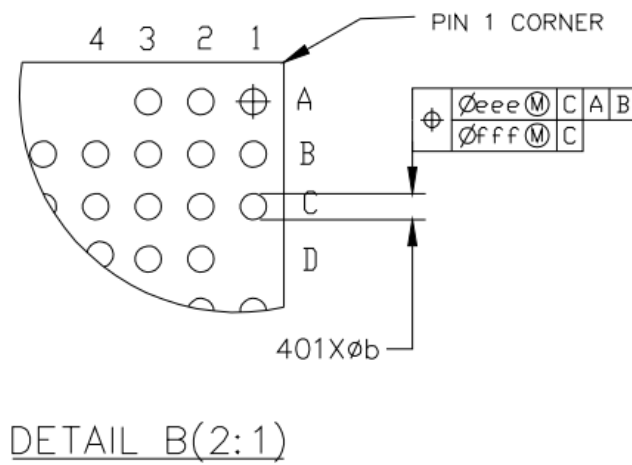
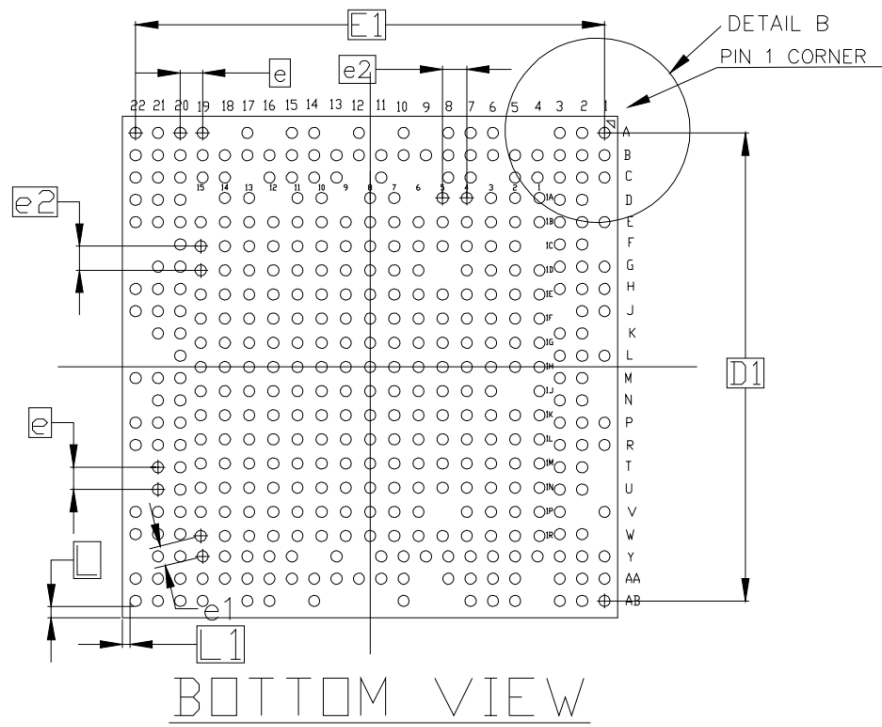
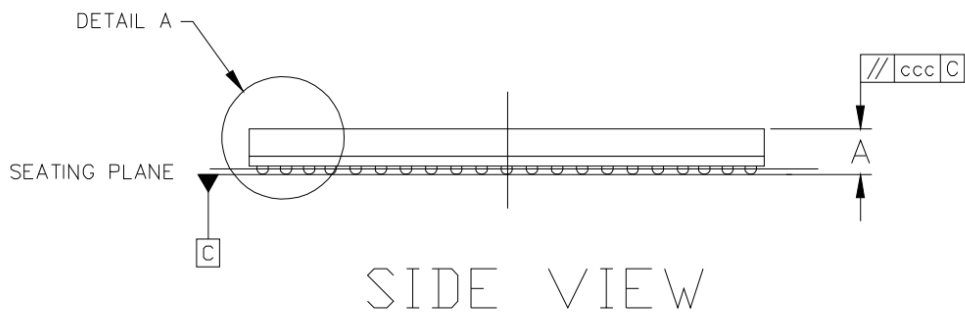


Fig.2-3 Package Bottom View



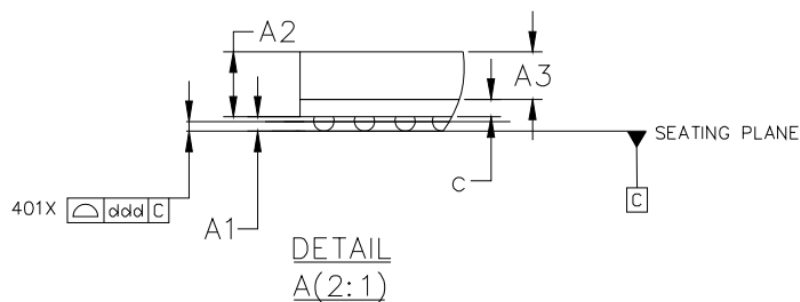


Fig.2-4 Package Side View

| SYMBOL | MILLIMETER  |       |       |
|--------|-------------|-------|-------|
|        | MIN         | NOM   | MAX   |
| A      | 1.09        | 1.17  | 1.25  |
| A1     | 0.16        | 0.21  | 0.26  |
| A2     | 0.91        | 0.96  | 1.01  |
| A3     | 0.70 BASIC  |       |       |
| c      | 0.22        | 0.26  | 0.30  |
| D      | 13.40       | 13.50 | 13.60 |
| D1     | 12.60 BASIC |       |       |
| E      | 13.20       | 13.30 | 13.40 |
| E1     | 12.6 BASIC  |       |       |
| e      | 0.60 BASIC  |       |       |
| e1     | 0.55 BASIC  |       |       |
| e2     | 0.65 BASIC  |       |       |
| b      | 0.25        | 0.30  | 0.35  |
| L      | 0.30 REF    |       |       |
| L1     | 0.20 REF    |       |       |
| aaa    | 0.15        |       |       |
| ccc    | 0.15        |       |       |
| ddd    | 0.10        |       |       |
| eee    | 0.15        |       |       |
| fff    | 0.08        |       |       |

Fig.2-5 Package Dimension

## 2.4 MSL Information

Moisture sensitivity level: MSL3

## 2.5 Lead Finish/Ball Material Information

Lead finish/Ball material: SnAgCu

## 2.6 Pin Number List

Table 2-1 Pin Number Order Information

| Pin name  | Pin# | Pin name | Pin# |
|---|------|----------|------|
| VSS0  | A1   | VSS38    | 1B7  |
| DDRPHY_A_DQS1N/DDR4_DQSU_N_A/LPDDR4_DQS1N_A/DDR3_DQS1N/LPDDR3_DQS2N | A2   | VSS39    | 1B8  |

| Pin name  | Pin# | Pin name  | Pin# |
|---|------|---|------|
| VSS1  | A3   | DDRPHY_A_DQ5/DDR4_DQL5_A/LPDDR4_DQ5_A/DDR3_D7/LPDDR3_D5   | 1B9  |
| DDRPHY_A_DQS0P/DDR4_DQSL_P_A/LPDDR4_DQS0P_A/DDR3_DQS0P/LPDDR3_DQS0P | A6   | DDRPHY_B_DQ7/DDR4_DQU2_B/LPDDR4_DQ7_B/DDR3_D25/LPDDR3_D11 | 1B10 |
| VSS2  | A7   | DDRPHY_B_DQ5/DDR4_DQU3_B/LPDDR4_DQ5_B/DDR3_D24/LPDDR3_D15 | 1B11 |
| DDRPHY_A_DQ3/DDR4_DQL1_A/LPDDR4_DQ3_A/DDR3_D1/LPDDR3_D3             | A8   | VSS40   | 1B12 |
| DDRPHY_B_DQ3/DDR4_DQU5_B/LPDDR4_DQ3_B/DDR3_D30/LPDDR3_D8            | A10  | VSS41   | 1B13 |
| DDRPHY_B_DQS0N/DDR4_DQSU_N_B/LPDDR4_DQS0N_B/DDR3_DQS3N/LPDDR3_DQS1N | A12  | VCCIO2  | 1B14 |
| DDRPHY_B_DQ0/DDR4_DQU4_B/LPDDR4_DQ0_B/DDR3_D29/LPDDR3_D14           | A14  | VSS42   | 1B15 |
| DDRPHY_B_DM0/DDR4_DMU_B/LPDDR4_DM0_B/DDR3_DM3/LPDDR3_DM1            | A15  | DDRPHY_A7/DDR4_A7/LPDDR4_A4_A/DDR3_A6                     | 1C2  |
| DDRPHY_B_DQS1N/DDR4_DQSL_N_B/LPDDR4_DQS1N_B/DDR3_DQS2N/LPDDR3_DQS3N | A17  | DDR_RZQ   | 1C3  |
| VSS3  | A19  | DDR_PLL_AVSS  | 1C4  |
| DDRPHY_B_DQ11/DDR4_DQL6_B/LPDDR4_DQ11_B/DDR3_D22/LPDDR3_D31         | A20  | VSS43   | 1C5  |
| SDMMC_D2/JTAG_CPU_TCK_M0/UART4_RX/HSM_CLK_OUT_M0/GPIO2_A2_u         | A21  | DDR_VDDQ_3  | 1C6  |
| VSS4  | A22  | DDR_VDDQ_4  | 1C7  |
| PWM3_M0/UART1_RX_M1/I2C1_SDA_M1/GPIO4_C6_d                          | AA1  | DDR_VDDQ_5  | 1C8  |
| SDIO0_DET_N/UART5_CTSN_M0/I2C2_SDA_M1/GPIO1_A6_d                    | AA2  | VSS44   | 1C9  |
| SDIO0_CLK/UART5_RTSN_M0/I2C2_SCL_M1/GPIO1_A5_d                      | AA3  | VSS45   | 1C10 |
| VSS27   | AA5  | VSS46   | 1C11 |
| EMMC_CMD/UART5_RX_M1/I2C6_SCL_M1/GPIO1_D4_u                         | AA6  | VSS47   | 1C12 |
| EMMC_D4/FSPI_CSN0/GPIO1_D0_u  | AA7  | VSS48   | 1C13 |
| EMMC_D1/FSPI_D1/GPIO1_C5_u  | AA8  | VSS49   | 1C14 |
| SARADC_IN0  | AA10 | VSS50   | 1C15 |
| USB30_OTG0_SSRXP/PCIE20_RXDP  | AA11 | VSS51   | 1D1  |
| AVSS2_VSS1  | AA12 | VSS52   | 1D2  |
| USB30_OTG0_SSTXN/PCIE20_TXDN  | AA13 | VSS53   | 1D3  |
| PCIE20_REFCLKP  | AA14 | DDR_VDDQ_2  | 1D4  |
| PWM6_M2/RGMII1_TXER/UART6_TX_M1/I2C3_SCL_M1/GPIO3_C1_d              | AA15 | DDR_VDDQL_2   | 1D6  |
| I2S0_SDI_M0/RGMII1_MDIO/TSIO_D3/GPIO3_B7_d                          | AA16 | DDR_VDDQL_3   | 1D7  |
| I2S0_LRCK_M0/RGMII1_MDC/TSIO_D2/GPIO3_B6_d                          | AA17 | DDR_VDDQL_4   | 1D8  |
| UART2_CTSN_M0/RGMII1_RXD0/TSIO_D4/GPIO3_A3_d                        | AA18 | VSS54   | 1D9  |
| UART2_RX_M0/RGMII1_TXD1/TSIO_D7/GPIO3_A0_d                          | AA19 | PMUPLL_AVSS1  | 1D10 |
| SDIO1_D1/RGMII1_RXD2/TSI1_SYNC/UART6_RX_M0/PCIE_WAKEN_M0/GPIO3_A7_d | AA20 | USB20_DVDD0V9   | 1D11 |
| SDIO1_D3/RGMII1_TXD2/TSIO_D0/UART7_RTSN_M0/GPIO3_B1_d               | AA21 | USB20_AVDD1V8   | 1D12 |
| SDIO1_CLK/RGMII1_TXCLK/TSI1_D0/UART6_CTSN/GPIO3_A4_d                | AA22 | USB20_AVDD3V3   | 1D13 |
| VSS28   | AB1  | USB20_OTG0_VBUSDET  | 1D14 |
| SDIO0_D0/I2C3_SCL_M0/SCR_DET_N_M0/PCIE_CLKREQN_M1/GPIO1_A0_d        | AB2  | AVSS1_VSS4  | 1D15 |
| SDIO0_CMD/PWM4_M1/HSM_CLK_OUT_M1/GPIO1_A4_d                         | AB3  | DDRPHY_A0/DDR4_A0/LPDDR4_ODT1_B/DDR3_A9/LPDDR3_ODT2       | 1E1  |
| EMMC_CLK/FSPI_CLK/GPIO1_D5_d  | AB5  | DDRPHY_ODT0/DDR4_ODT0/LPDDR4_ODT1_A/DDR3_WEN/LPDDR3_ODT0  | 1E2  |
| EMMC_STRB/UART5_TX_M1/I2C6_SDA_M1/GPIO1_D7_d                        | AB6  | VSS55   | 1E3  |
| EMMC_D3/FSPI_D3/GPIO1_C7_u  | AB7  | DDR_VDDQ_1  | 1E4  |

| Pin name   | Pin# | Pin name  | Pin# |
|--|------|---|------|
| SARADC_IN1   | AB10 | DDR_VDDQL_1   | 1E5  |
| PCIE20_REFCLKN   | AB14 | VSS56   | 1E6  |
| I2S0_SDO_M0/RGMII1_TXEN/TSIO_FAIL/GPIO3_C0_d   | AB16 | VSS57   | 1E7  |
| I2S0_SCLK_M0/ETH_CLK_25M_OUT/TSIO_D1/GPIO3_B5_d  | AB17 | VSS58   | 1E8  |
| RGMII1_RXDV_CRS/GPIO3_C2_d   | AB19 | VSS59   | 1E9  |
| PWM5_M1/SPDIF_TX_M2/CLK_32K_OUT_M0/UART6_RX_M1/I2C3_SDA_M1/REF_CLK_OUT_M1/GPIO3_C3_d   | AB20 | FEPHY_REXT  | 1E10 |
| SDIO1_D0/RGMII1_RXD3/TSI1_VALID/UART6_TX_M0/PCI_E_CLKREQN_M0/GPIO3_A6_d                | AB21 | FEPHY_AVDD0V9   | 1E11 |
| VSS29  | AB22 | FEPHY_AVDD1V8   | 1E12 |
| DDRRPHY_A_DM1/DDR4_DMU_A/LPDDR4_DM1_A/DDR3_D_M1/LPDDR3_DM2                             | B1   | OTP_VCC1V8  | 1E13 |
| DDRRPHY_A_DQS1P/DDR4_DQSU_P_A/LPDDR4_DQS1P_A/DDR3_DQS1P/LPDDR3_DQS2P                   | B2   | FEPHY_AVDD3V3   | 1E14 |
| DDRRPHY_A_DQ13/DDR4_DQU3_A/LPDDR4_DQ13_A/DDR3_D8/LPDDR3_D23                            | B3   | AVSS1_VSS5  | 1E15 |
| VSS5   | B4   | DDRRPHY_A2/DDR4_A2/LPDDR4_ODT0_B/DDR3_A13/LPDDR3_ODT3   | 1F1  |
| DDRRPHY_A_DQ1/DDR4_DQL2_A/LPDDR4_DQ1_A/DDR3_D0/LPDDR3_D1                               | B5   | VSS60   | 1F2  |
| DDRRPHY_A_DQS0N/DDR4_DQSL_N_A/LPDDR4_DQS0N_A/DDR3_DQS0N/LPDDR3_DQS0N                   | B6   | VSS61   | 1F3  |
| VSS6   | B7   | DDR_VDDQ_0  | 1F4  |
| DDRRPHY_A_DQ2/DDR4_DQL0_A/LPDDR4_DQ2_A/DDR3_D2/LPDDR3_D2                               | B8   | DDR_VDDQL_0   | 1F5  |
| DDRRPHY_A_DQ4/DDR4_DQL4_A/LPDDR4_DQ4_A/DDR3_D6/LPDDR3_D4                               | B9   | VSS62   | 1F6  |
| DDRRPHY_B_DQ4/DDR4_DQU7_B/LPDDR4_DQ4_B/DDR3_D26/LPDDR3_D9                              | B10  | VSS63   | 1F7  |
| DDRRPHY_B_DQ2/DDR4_DQU1_B/LPDDR4_DQ2_B/DDR3_D28/LPDDR3_D13                             | B11  | VSS64   | 1F8  |
| DDRRPHY_B_DQS0P/DDR4_DQSU_P_B/LPDDR4_DQS0P_B/DDR3_DQS3P/LPDDR3_DQS1P                   | B12  | VSS65   | 1F9  |
| DDRRPHY_B_DQ1/DDR4_DQU0_B/LPDDR4_DQ1_B/DDR3_D31/LPDDR3_D12                             | B13  | VSS66   | 1F10 |
| VSS7   | B14  | AVSS1_VSS6  | 1F11 |
| DDRRPHY_B_DQ6/DDR4_DQU6_B/LPDDR4_DQ6_B/DDR3_D27/LPDDR3_D10                             | B15  | AVSS1_VSS7  | 1F12 |
| DDRRPHY_B_DQ13/DDR4_DQL2_B/LPDDR4_DQ13_B/DDR3_D20/LPDDR3_D24                           | B16  | AVSS1_VSS8  | 1F13 |
| DDRRPHY_B_DQS1P/DDR4_DQSL_P_B/LPDDR4_DQS1P_B/DDR3_DQS2P/LPDDR3_DQS3P                   | B17  | AVSS1_VSS9  | 1F14 |
| DDRRPHY_B_DQ8/DDR4_DQL1_B/LPDDR4_DQ8_B/DDR3_D17/LPDDR3_D27                             | B18  | AVSS1_VSS10   | 1F15 |
| DDRRPHY_B_DQ12/DDR4_DQL0_B/LPDDR4_DQ12_B/DDR3_D16/LPDDR3_D28                           | B19  | DDRRPHY_BA0/DDR4_BA0/LPDDR4_CKE0_B/DDR3_BA2/LPDDR3_CKE0 | 1G1  |
| DDRRPHY_B_DQ10/DDR4_DQL4_B/LPDDR4_DQ10_B/DDR3_D18/LPDDR3_D30                           | B20  | DDRRPHY_A6/DDR4_A6/LPDDR4_CSN1_B/DDR3_A3/LPDDR3_CSN2    | 1G2  |
| SDMMC_D3/JTAG_CPU_TMS_M0/UART4_TX/SCR_DATA_M1/GPIO2_A3_u                               | B21  | VSS67   | 1G3  |
| SDMMC_CLK/JTAG_MCU_TMS_M0/SCR_CLK_M1/I2C7_SCL/FEPHY_LED_SPD_M1/TEST_CLK_OUT/GPIO2_A5_d | B22  | VSS68   | 1G4  |
| DDRRPHY_A_DQ8/DDR4_DQU1_A/LPDDR4_DQ8_A/DDR3_D12/LPDDR3_D19                             | C1   | VSS69   | 1G5  |
| DDRRPHY_A_DQ9/DDR4_DQU5_A/LPDDR4_DQ9_A/DDR3_D14/LPDDR3_D16                             | C2   | VSS70   | 1G6  |
| DDRRPHY_A_DM0/DDR4_DML_A/LPDDR4_DM0_A/DDR3_DM0/LPDDR3_DM0                              | C3   | VSS71   | 1G7  |
| DDRRPHY_A_DQ0/DDR4_DQL6_A/LPDDR4_DQ0_A/DDR3_D4/LPDDR3_D0                               | C4   | VSS72   | 1G8  |
| DDRRPHY_A5/DDR4_A5/LPDDR4_A1_A/DDR3_A4   | C5   | VSS73   | 1G9  |
| VSS8   | C7   | VSS74   | 1G10 |
| DDRRPHY_A_DQ10/DDR4_DQU0_A/LPDDR4_DQ10_A/DDR3_D15/LPDDR3_D21                           | C8   | HDMI_REXT   | 1G11 |

| Pin name  | Pin# | Pin name   | Pin# |
|---|------|--|------|
| DDRRPHY_A_DQ15/DDR4_DQU6_A/LPDDR4_DQ15_A/DDR3_D11/LPDDR3_D18              | C11  | HDMI_TX_DVDD0V9  | 1G12 |
| DDRRPHY_A_DQ6/DDR4_DQL7_A/LPDDR4_DQ6_A/DDR3_D5/LPDDR3_D6                  | C13  | HDMI_TX_AVDD1V8  | 1G13 |
| VSS9  | C14  | AVSS1_VSS11  | 1G14 |
| VSS10   | C15  | AVSS1_VSS12  | 1G15 |
| DDRRPHY_B_DQ15/DDR4_DQL5_B/LPDDR4_DQ15_B/DDR3_D23/LPDDR3_D29              | C16  | DDRRPHY_A14/DDR4_WEN/A14/LPDDR4_CSN0_B/DDR3_ODT0/LPDDR3_CSN3 | 1H1  |
| DDRRPHY_B_DM1/DDR4_DML_B/LPDDR4_DM1_B/DDR3_DM2/LPDDR3_DM3                 | C18  | DDRRPHY_CKE/DDR4_CKE/LPDDR4_CKE1_B/DDR3_RASN                 | 1H2  |
| VSS11   | C19  | VSS75  | 1H3  |
| SDMMC_CMD/JTAG_MCU_TCK_M0/PWM3_M1/SCR_RSTN_M1/FEPHY_LED_DPX_M1/GPIO2_A4_u | C20  | DDR_VREFOUT  | 1H4  |
| SDMMC_D0/UART0_RX_M1/UART4_RTSN/I2C4_SCL/GPIO2_A0_u                       | C21  | GPU_DVDD_0   | 1H5  |
| SDMMC_D1/UART0_TX_M1/UART4_CTSN/I2C4_SDA/GPIO2_A1_u                       | C22  | VSS76  | 1H6  |
| DDRRPHY_A_DQ12/DDR4_DQU7_A/LPDDR4_DQ12_A/DDR3_D10/LPDDR3_D20              | D2   | VSS77  | 1H7  |
| VSS12   | D3   | LOGIC_DVDD_0   | 1H8  |
| USB20_OTG0_ID   | D20  | LOGIC_DVDD_1   | 1H9  |
| SDMMC_DET/SCR_DET_M1/I2C7_SDA/FEPHY_LED_LIN_K_M1/GPIO2_A6_u               | D21  | VSS78  | 1H10 |
| VSS13   | D22  | TVSS   | 1H11 |
| DDRRPHY_A12/DDR4_A12/LPDDR4_A2_A/DDR3_A10/LPDDR3_A4                       | E1   | PMU_LOGIC_DVDD   | 1H12 |
| DDRRPHY_A15/DDR4_CASN/A15/LPDDR4_A3_A/DDR3_BA1/LPDDR3_A0                  | E2   | PMU_PLL_AVDD0V9  | 1H13 |
| VSS14   | E3   | PMU_PLL_AVDD1V8  | 1H14 |
| USB20_HOST1_DP  | E20  | VSS79  | 1H15 |
| USB20_OTG0_DP   | E21  | VSS80  | 1J1  |
| USB20_OTG0_DM   | E22  | VCCIO4   | 1J3  |
| DDRRPHY_BA1/DDR4_BA1/LPDDR4_A5_A/DDR3_A12/LPDDR3_A1                       | F2   | VSS81  | 1J4  |
| DDRRPHY_CSN0/DDR4_CSN0/LPDDR4_CSN1_A/DDR3_CSN/LPDDR3_CSN1                 | F3   | GPU_DVDD_1   | 1J5  |
| USB20_HOST1_DM  | F20  | GPU_DVDD_2   | 1J6  |
| DDRRPHY_A9/DDR4_A9/LPDDR4_CLKP_A/DDR3_A11/LPDDR3_A2                       | G1   | VSS82  | 1J7  |
| DDRRPHY_A13/DDR4_A13/LPDDR4_CLKN_A/DDR3_A8/LPDDR3_A3                      | G2   | VSS83  | 1J8  |
| VSS15   | G3   | LOGIC_DVDD_2   | 1J9  |
| FEPHY_TXP   | G20  | LOGIC_DVDD_3   | 1J10 |
| FEPHY_TXN   | G21  | PMUPLL_AVSS2   | 1J11 |
| DDRRPHY_CLKP/DDR4_CLKP/LPDDR4_CLKP_B/DDR3_CLKP/LPDDR3_CLKP                | H1   | NPOR   | 1J12 |
| DDRRPHY_CLKN/DDR4_CLKN/LPDDR4_CLKN_B/DDR3_CLKN/LPDDR3_CLKN                | H2   | PMUIO_VCC3V3   | 1J13 |
| VSS16   | H3   | REF_CLK_OUT_M0/GPIO0_A1_d                                    | 1J14 |
| AVSS1_VSS0  | H20  | VSS84  | 1J15 |
| FEPHY_RXP   | H21  | VSS85  | 1K1  |
| FEPHY_RXN   | H22  | DDR_PLL_AVDD1V8  | 1K2  |
| VSS17   | J1   | VSS86  | 1K3  |
| DDRRPHY_A1/DDR4_A1/LPDDR4_CKE1_A/DDR3_A14                                 | J2   | VSS87  | 1K4  |
| AVSS1_VSS1  | J20  | VSS88  | 1K5  |
| HDMI_TX_D2N   | J21  | VSS89  | 1K6  |
| HDMI_TX_D2P   | J22  | VSS90  | 1K7  |
| VSS18   | K2   | VSS91  | 1K8  |
| DDRRPHY_A3/DDR4_A3/LPDDR4_CKE0_A/DDR3_A1                                  | K3   | LOGIC_DVDD_4   | 1K9  |

| Pin name   | Pin# | Pin name                                  | Pin# |
|--|------|---|------|
| HDMI_TX_D1N  | K20  | VSS92                                     | 1K10 |
| HDMI_TX_D1P  | K21  | VDAC_AVSS                                 | 1K11 |
| DDRRPHY_A4/DDR4_A4/LPDDR4_A0_B/DDR3_A2/LPDDR3_A5       | L1   | VDAC_IREF                                 | 1K12 |
| VSS19  | L2   | VDAC_AVDD1V8                              | 1K13 |
| DDRRPHY_A10/DDR4_A10/LPDDR4_A1_B/DDR3_A0               | L3   | ACODEC_AVDD1V8                            | 1K14 |
| HDMI_TX_D0P  | L20  | VSS93                                     | 1K15 |
| DDRRPHY_A8/DDR4_A8/LPDDR4_A4_B/DDR3_A5/LPDDR3_A6       | M2   | PWR_CTRL1/SPI0_CSN0/GPIO4_B6_u            | 1L1  |
| DDRRPHY_A11/DDR4_A11/LPDDR4_A5_B/DDR3_A7/LPDDR3_A7     | M3   | VSS94                                     | 1L2  |
| HDMI_TX_D0N  | M20  | VSS95                                     | 1L3  |
| AVSS1_VSS2   | M21  | CPU_DVDD_0                                | 1L4  |
| AVSS1_VSS3   | M22  | CPU_DVDD_1                                | 1L5  |
| DDRRPHY_BG0/DDR4_BG0/LPDDR4_A3_B/DDR3_BA0/LPDDR3_A8    | N2   | VSS96                                     | 1L6  |
| DDRRPHY_ACTN/DDR4_ACTN/LPDDR4_A2_B/DDR3_CSN0/LPDDR3_A9 | N3   | VSS97                                     | 1L7  |
| HDMI_TX_CLKP   | N20  | VSS98                                     | 1L8  |
| HDMI_TX_CLKN   | N21  | LOGIC_DVDD_5                              | 1L9  |
| DDRRPHY_RESETN/DDR4_RESETN/LPDDR4_RESETN/DDR3_RESETN   | P1   | VSS99                                     | 1L10 |
| VSS20  | P2   | VSS100                                    | 1L11 |
| PWM7_M0/PWR_CTRL0/GPIO4_C2_d                           | P3   | ACODEC_AVSS                               | 1L12 |
| HDMI_TX_SDA_5V0_od                                     | P20  | VSS101                                    | 1L13 |
| HDMI_TX_CEC_3V3_u                                      | P21  | VSS102                                    | 1L14 |
| HDMI_TX_SCL_5V0_od                                     | P22  | VSS103                                    | 1L15 |
| SDMMC0_PWREN/I2C0_SCL_M1/GPIO4_A1_d                    | R1   | I2S1_LRCK/UART1_TX_M0/GPIO4_A6_d          | 1M1  |
| I2S1_SDI0/SPI0_CLK/GPIO4_B4_d                          | R2   | I2S1_MCLK/UART1_CTSN/PDM_CLK1/GPIO4_A4_d  | 1M2  |
| SPDIF_TX_M0/I2C0_SDA_M1/PMU_DEBUG/GPIO4_A0_d           | R3   | CPU_DVDD_2                                | 1M3  |
| VSS21  | R20  | CPU_DVDD_3                                | 1M4  |
| GPIO0_A0_d   | R21  | CPU_DVDD_4                                | 1M5  |
| HDMI_TX_HPD_5V0_d                                      | R22  | VSS104                                    | 1M6  |
| UART0_TX_M0/JTAG_CPU_TCK_M1/JTAG_MCU_TCK_M1/GPIO4_D0_d | T2   | VSS105                                    | 1M7  |
| UART0_RX_M0/JTAG_CPU_TMS_M1/JTAG_MCU_TMS_M1/GPIO4_C7_u | T3   | I2S0_SDO_M1/SPI1_MISO/GPIO1_C0_d          | 1M8  |
| OSC_SOC_XOUT   | T20  | VSS106                                    | 1M9  |
| OSC_SOC_XIN  | T21  | VSS107                                    | 1M10 |
| I2S1_SDI3/I2C1_SDA_M0/UART3_RTSN/GPIO4_A2_d            | U2   | VSS108                                    | 1M11 |
| I2S1_SDI2/I2C1_SCL_M0/UART3_CTSN/GPIO4_A3_d            | U3   | ACODEC_VCM                                | 1M12 |
| VDAC_IOUTP   | U20  | VCCIO3                                    | 1M13 |
| VSS22  | U21  | VSS109                                    | 1M14 |
| PWM1_M0/I2C0_SCL_M0/ARM_AVS/GPIO4_C4_d                 | V1   | VSS110                                    | 1M15 |
| PWM4_M0/FEPHY_LED_SPD_M0/UART3_RX_M1/GPIO4_B7_d        | V3   | PWM0_M0/I2C0_SDA_M0/GPU_AVS/GPIO4_C3_d    | 1N1  |
| VSS23  | V20  | I2S1_SDO2/UART3_TX_M0/PDM_SDI1/GPIO4_B1_d | 1N2  |
| VSS24  | V21  | I2S1_SDO3/SPI0_MOSI/PDM_SDI0/GPIO4_B2_d   | 1N3  |
| ACODEC_LINEOUT_L                                       | V22  | SPI1_CSN1/PWM7_M1/GPIO1_C2_d              | 1N4  |
| PWM6_M0/SPI0_CSN1/PDM_SDI3/GPIO4_C1_d                  | W2   | I2S0_MCLK_M1/GPIO1_B4_d                   | 1N5  |
| I2S1_SDI1/SPI0_MISO/PDM_SDI2/GPIO4_B3_d                | W3   | VCCIO0                                    | 1N6  |

| Pin name  | Pin# | Pin name  | Pin# |
|---|------|---|------|
| VSS25   | W20  | SPI1_CSNO/GPIO1_C1_u                                      | 1N7  |
| VSS26   | W21  | I2S0_LRCK_M1/SPI1_CLK/GPIO1_B6_d                          | 1N8  |
| ACODEC_LINEOUT_R  | W22  | AVSS2_VSS2  | 1N9  |
| FEPHY_LED_DPX_M0/PDM_CLK0/GPIO4_B5_d                              | Y1   | AVSS2_VSS3  | 1N10 |
| PWM5_M0/FEPHY_LED_LINK_M0/UART3_TX_M1/GPIO4_C0_d                  | Y2   | SARADC_AVDD1V8  | 1N11 |
| SDIO0_D1/I2C3_SDA_M0/SCR_DATA_M0/PCIE_WAKEN_M1/GPIO1_A1_d         | Y3   | VSS111  | 1N12 |
| SDIO0_D2/UART5_RX_M0/SCR_CLK_M0/PCIE_PERSTN_M1/PWM0_M1/GPIO1_A2_d | Y4   | VSS112  | 1N13 |
| CLK_32K_OUT_M1/SPDIF_TX_M1/PWM6_M1/GPIO1_C3_d                     | Y5   | VSS113  | 1N14 |
| EMMC_D5/FSPI_CSNO1/GPIO1_D1_u                                     | Y6   | VDAC_IOUTN  | 1N15 |
| EMMC_D0/FSPI_D0/GPIO1_C4_u  | Y7   | PWM2_M0/UART1_TX_M1/I2C1_SCL_M1/GPIO4_C5_d                | 1P1  |
| EMMC_D2/FSPI_D2/GPIO1_C6_u  | Y8   | I2S1_SCLK/UART1_RTSN/GPIO4_A5_d                           | 1P2  |
| EMMC_D6/UART5_RTSN_M1/I2C5_SCL_M1/GPIO1_D2_u                      | Y9   | I2S1_SDO0/UART1_RX_M0/GPIO4_A7_d                          | 1P3  |
| I2S0_SDI_M1/SPI1_MOSI/GPIO1_B7_d                                  | Y10  | UART2_RTSN_M1/I2C5_SCL_M0/UART7_TX_M1/GPIO1_B2_d          | 1P4  |
| USB30_OTG0_SSRXN/PCIE20_RXDN                                      | Y11  | UART2_CTSN_M1/I2C5_SDA_M0/UART7_RX_M1/GPIO1_B3_d          | 1P6  |
| USB30_OTG0_SSTXP/PCIE20_TXDP                                      | Y13  | UART2_RX_M1/UART7_CTSN_M1/GPIO1_B0_d                      | 1P7  |
| AVSS2_VSS0  | Y15  | VCCIO1  | 1P8  |
| I2S0_MCLK_M0/RGMII1_CLK/TSIO_SYNC/GPIO3_B4_d                      | Y16  | SARADC_IN3  | 1P9  |
| UART2_RTSN_M0/RGMII1_RXD1/TSIO_D5/GPIO3_A2_d                      | Y17  | AVSS2_VSS4  | 1P10 |
| UART2_TX_M0/RGMII1_TXD0/TSIO_D6/GPIO3_A1_d                        | Y18  | PCIE20_USB30_AVDD0V9                                      | 1P11 |
| SDIO1_D2/RGMII1_TXD3/UART7_CTSN_M0/PCIE_PERSTN_M0/GPIO3_B0_d      | Y19  | PCIE20_USB30_AVDD1V8                                      | 1P12 |
| SDIO1_CMD/RGMII1_RXCLK/TSI1_CLKIN/UART6_RTSN/GPIO3_A5_d           | Y20  | VSS114  | 1P13 |
| SDIO1_DET/TSIO_VALID/UART7_RX_M0/I2C6_SDA_M0/GPIO3_B3_d           | Y21  | VSS115  | 1P14 |
| VSS30   | 1A1  | VSS116  | 1P15 |
| DDRRPHY_CSNO1/DDR4_CSNO1/LPDDR4_CSNO_A/DDR3_CSNO1/LPDDR3_CSNO     | 1A2  | SDIO0_D3/UART5_TX_M0/SCR_RSTN_M0/PWM1_M1/GPIO1_A3_d       | 1R1  |
| DDRRPHY_A16/DDR4_RASN/A16/LPDDR4_A0_A/DDR3_CKE0                   | 1A3  | I2S1_SDO1/UART3_RX_M0/GPIO4_B0_d                          | 1R2  |
| VSS31   | 1A4  | VSS117  | 1R3  |
| DDRRPHY_A_DQ11/DDR4_DQU2_A/LPDDR4_DQ11_A/DDR3_D9/LPDDR3_D17       | 1A5  | VSS118  | 1R4  |
| DDRRPHY_A_DQ14/DDR4_DQU4_A/LPDDR4_DQ14_A/DDR3_D13/LPDDR3_D22      | 1A7  | EMMC_D7/UART5_CTSN_M1/I2C5_SDA_M1/GPIO1_D3_u              | 1R5  |
| DDRRPHY_A_DQ7/DDR4_DQL3_A/LPDDR4_DQ7_A/DDR3_D3/LPDDR3_D7          | 1A8  | UART2_TX_M1/UART7_RTSN_M1/GPIO1_B1_d                      | 1R6  |
| VSS32   | 1A10 | SDIO0_PWREN/PWM2_M1/GPIO1_A7_d                            | 1R7  |
| DDRRPHY_B_DQ14/DDR4_DQL7_B/LPDDR4_DQ14_B/DDR3_D21/LPDDR3_D25      | 1A11 | I2S0_SCLK_M1/GPIO1_B5_d                                   | 1R8  |
| DDRRPHY_B_DQ9/DDR4_DQL3_B/LPDDR4_DQ9_B/DDR3_D19/LPDDR3_D26        | 1A13 | SARADC_IN2  | 1R9  |
| VSS33   | 1A14 | AVSS2_VSS5  | 1R10 |
| VSS34   | 1B1  | AVSS2_VSS6  | 1R11 |
| DDRRPHY_ODT1/DDR4_ODT1/LPDDR4_ODT0_A/DDR3_ODT1/LPDDR3_ODT1        | 1B2  | AVSS2_VSS7  | 1R12 |
| DDRRPHY_BG1/DDR4_BG1/DDR3_A15                                     | 1B3  | VSS119  | 1R13 |
| VSS35   | 1B4  | VSS120  | 1R14 |
| VSS36   | 1B5  | SDIO1_PWREN/TSIO_CLKIN/UART7_TX_M0/I2C6_SCL_M0/GPIO3_B2_d | 1R15 |
| VSS37   | 1B6  |   |      |

## Chapter 3 Electrical Specification

### 3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

| Parameters                  | Related Power Group  | Min  | Max | Unit |
|-----------------------------|--|------|-----|------|
| Supply voltage for CPU      | CPU_DVDD   | -0.3 | TBD | V    |
| Supply voltage for GPU      | GPU_DVDD   | -0.3 | TBD | V    |
| Supply voltage for Logic    | LOGIC_DVDD   | -0.3 | TBD | V    |
| Supply voltage for PMU      | PMU_LOGIC_DVDD   | -0.3 | TBD | V    |
| 0.9V supply voltage         | PMU_PLL_AVDD0V9<br>HDMI_TX_DVDD0V9<br>USB20_DVDD0V9<br>FEPHY_AVDD0V9<br>PCIE20_USB30_AVDD0V9   | -0.3 | TBD | V    |
| 1.8V/3.3V supply voltage    | VCCIOi(i=0~4, 1.8V/3.3V mode)  | -0.3 | TBD | V    |
| 1.8V supply voltage         | PMU_PLL_AVDD1V8<br>HDMI_TX_AVDD1V8<br>OTP_VCC1V8<br>USB20_AVDD1V8<br>FEPHY_AVDD1V8<br>VDAC_AVDD1V8<br>ACODEC_AVDD1V8<br>PCIE20_USB30_AVDDD1V8<br>SARADC_AVDD1V8<br>DDR_PLL_AVDD1V8 | -0.3 | TBD | V    |
| 3.3V supply voltage         | PMUIO_VCC3V3<br>USB20_AVDD3V3<br>FEPHY_AVDD3V3   | -0.3 | TBD | V    |
| Supply voltage for DDR IO   | DDR_VDDQ<br>DDR_VDDQL  | -0.3 | TBD | V    |
| Storage Temperature         | Tstg   | NA   | NA  | °C   |
| Max Conjunction Temperature | Tj   | NA   | NA  | °C   |

### 3.2 Recommended Operating Conditions

The following table describes the recommended operating conditions.

Table 3-2 Recommended operating conditions

| Parameters                      | Symbol                             | Min         | Typ        | Max           | Unit |
|---------------------------------|------------------------------------|-------------|------------|---------------|------|
| Voltage for CPU                 | CPU_DVDD                           | 0.81        | 0.90       | TBD           | V    |
| Voltage for GPU                 | GPU_DVDD                           | 0.81        | 0.90       | TBD           | V    |
| Voltage for LOGIC               | LOGIC_DVDD                         | 0.81        | 0.90       | 0.99          | V    |
| Voltage for PMU                 | PMU_LOGIC_DVDD                     | 0.81        | 0.90       | 0.99          | V    |
| Voltage for PLL Analog (1.8V)   | PMU_PLL_AVDD1V8<br>DDR_PLL_AVDD1V8 | 1.62        | 1.8        | TBD           | V    |
| Voltage for GPIO (1.8V/3.3V)    | VCCIOi(i=0~4)                      | 1.62<br>3.0 | 1.8<br>3.3 | 1.98<br>3.465 | V    |
| Voltage for GPIO (3.3V only)    | PMUIO_VCC3V3                       | 3.0         | 3.3        | 3.465         | V    |
| Voltage for HDMI Analog (1.8V)  | HDMI_TX_AVDD1V8                    | 1.62        | 1.8        | 1.98          | V    |
| Voltage for USB Analog (1.8V)   | USB20_AVDD1V8                      | 1.62        | 1.8        | 1.98          | V    |
| Voltage for USB Analog (3.3V)   | USB20_AVDD3V3                      | 3.0         | 3.3        | 3.6           | V    |
| Voltage for FEPHY Analog (1.8V) | FEPHY_AVDD1V8                      | 1.62        | 1.8        | 1.98          | V    |
| Voltage for FEPHY Analog (3.3V) | FEPHY_AVDD3V3                      | 2.97        | 3.3        | 3.63          | V    |
| Voltage for OTP Analog(1.8V)    | OTP_VCC1V8                         | 1.62        | 1.8        | 1.98          | V    |
| Voltage for VDAC Analog(1.8V)   | VDAC_AVDD1V8                       | 1.62        | 1.8        | 1.98          | V    |
| Voltage for ACODEC Analog(1.8V) | ACODEC_AVDD1V8                     | 1.62        | 1.8        | 1.98          | V    |



| Parameters                       | Symbol               | Min   | Typ  | Max   | Unit |
|----------------------------------|----------------------|-------|------|-------|------|
| Voltage for PCIE/U3 Analog(1.8V) | PCIE20_USB30_AVDD1V8 | 1.62  | 1.8  | 1.98  | V    |
| Voltage for SARADC Analog(1.8V)  | SARADC_AVDD1V8       | 1.62  | 1.8  | 1.98  | V    |
| DDR3 IO VDDQ Voltage             | DDR_VDDQ             | 1.425 | 1.5  | 1.575 | V    |
| DDR3L IO VDDQ Voltage            | DDR_VDDQ             | 1.283 | 1.35 | 1.417 | V    |
| LPDDR3 IO VDDQ Voltage           | DDR_VDDQ             | 1.14  | 1.2  | 1.3   | V    |
| DDR4 IO VDDQ Voltage             | DDR_VDDQ             | 1.14  | 1.2  | 1.3   | V    |
| LPDDR4 IO VDDQ Voltage           | DDR_VDDQ             | 1.06  | 1.1  | 1.17  | V    |
| LPDDR4X IO VDDQ Voltage          | DDR_VDDQL            | 0.54  | 0.6  | 0.66  | V    |
| Max CPU frequency                |                      | NA    | NA   | TBD   | GHz  |
| Max GPU frequency                |                      | NA    | NA   | TBD   | MHz  |
| Ambient Operating Temperature    | T <sub>A</sub>       | 0     | NA   | 80    | °C   |

### 3.3 DC Characteristics

Table 3-3 DC Characteristics

| Parameters         | Symbol              | Min             | Typ       | Max | Unit      |      |
|--------------------|---------------------|-----------------|-----------|-----|-----------|------|
| Digital GPIO @3.3V | Input Low Voltage   | V <sub>il</sub> | -0.3      | NA  | 0.8       | V    |
|                    | Input High Voltage  | V <sub>ih</sub> | 2.0       | NA  | VDDO+0.3  | V    |
|                    | Output Low Voltage  | V <sub>ol</sub> | -0.3      | NA  | 0.4       | V    |
|                    | Output High Voltage | V <sub>oh</sub> | 2.4       | NA  | VDDO+0.3  | V    |
|                    | Pullup Resistor     | R <sub>pu</sub> | 16        | 26  | 43        | Kohm |
|                    | Pulldown Resistor   | R <sub>pd</sub> | 16        | 26  | 43        | Kohm |
| Digital GPIO @1.8V | Input Low Voltage   | V <sub>il</sub> | -0.3      | NA  | 0.35*VDDO | V    |
|                    | Input High Voltage  | V <sub>ih</sub> | 0.65*VDDO | NA  | VDDO+0.3  | V    |
|                    | Output Low Voltage  | V <sub>ol</sub> | -0.3      | NA  | 0.4       | V    |
|                    | Output High Voltage | V <sub>oh</sub> | 1.4       | NA  | VDDO+0.3  | V    |
|                    | Pullup Resistor     | R <sub>pu</sub> | 16        | 26  | 43        | Kohm |
|                    | Pulldown Resistor   | R <sub>pd</sub> | 16        | 26  | 43        | Kohm |

| Parameters           | Symbol             | Min                 | Typ                   | Max | Unit                  |     |
|----------------------|--------------------|---------------------|-----------------------|-----|-----------------------|-----|
| DDR IO @DDR3 mode    | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQ              | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |
| DDR IO @DDR3L mode   | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQ              | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |
| DDR IO @DDR4 mode    | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQ              | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |
| DDR IO @LPDDR3 mode  | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQ              | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |
| DDR IO @LPDDR4 mode  | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQ              | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |
| DDR IO @LPDDR4X mode | Input High Voltage | V <sub>ih_dds</sub> | V <sub>ref</sub> +0.1 | NA  | DDR_VDDQL             | V   |
|                      | Input Low Voltage  | V <sub>il_dds</sub> | VSS                   | NA  | V <sub>ref</sub> -0.1 | V   |
|                      | output impedance   | R <sub>tt</sub>     | 20                    | NA  | 60                    | Ohm |

### 3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

| Parameters                           |                                  | Symbol          | Test condition                            | Min | Typ | Max | Unit |
|--------------------------------------|----------------------------------|-----------------|---|-----|-----|-----|------|
| Digital GPIO @3.3V                   | Input leakage current            | I <sub>i</sub>  | V <sub>in</sub> = 3.3V or 0V              | NA  | NA  | 10  | uA   |
|                                      | Tri-state output leakage current | I <sub>oz</sub> | V <sub>out</sub> = 3.3V or 0V             | NA  | NA  | 10  | uA   |
|                                      | High level input current         | I <sub>ih</sub> | V <sub>in</sub> = 3.3V, pulldown disabled | NA  | NA  | 10  | uA   |
|                                      |                                  |                 | V <sub>in</sub> = 3.3V, pulldown enabled  | NA  | NA  | 10  | uA   |
|                                      | Low level input current          | I <sub>il</sub> | V <sub>in</sub> = 0V, pullup disabled     | NA  | NA  | 10  | uA   |
| V <sub>in</sub> = 0V, pullup enabled |                                  |                 | NA  | NA  | 10  | uA  |      |
| Digital GPIO @1.8V                   | Input leakage current            | I <sub>i</sub>  | V <sub>in</sub> = 1.8V or 0V              | NA  | NA  | 10  | uA   |
|                                      | Tri-state output leakage current | I <sub>oz</sub> | V <sub>out</sub> = 1.8V or 0V             | NA  | NA  | 10  | uA   |
|                                      | High level input current         | I <sub>ih</sub> | V <sub>in</sub> = 1.8V, pulldown disabled | NA  | NA  | 10  | uA   |
|                                      |                                  |                 | V <sub>in</sub> = 1.8V, pulldown enabled  | NA  | NA  | 10  | uA   |
|                                      | Low level input current          | I <sub>il</sub> | V <sub>in</sub> = 0V, pullup disabled     | NA  | NA  | 10  | uA   |
| V <sub>in</sub> = 0V, pullup enabled |                                  |                 | NA  | NA  | 10  | uA  |      |

Note: VDDO and DVDD are both IO power Supply

### 3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

| Parameters |                             | Symbol           | Test condition                              | Min | Typ  | Max  | Unit               |
|------------|-----------------------------|------------------|---|-----|------|------|--------------------|
|            | Input clock frequency(Frac) | F <sub>in</sub>  | F <sub>in</sub> = FREF @1.8V/0.99V          | 10  | NA   | 800  | MHz                |
|            | VCO operating range         | F <sub>vco</sub> | F <sub>vco</sub> = Fref * FBDIV @3.3V/0.99V | 475 | NA   | 1900 | MHz                |
|            | Output clock frequency      | F <sub>out</sub> | F <sub>out</sub> = Fvco/POSTDIV @3.3V/0.99V | 9   | NA   | 1900 | MHz                |
|            | Lock time                   | T <sub>lt</sub>  | @ 3.3V/0.99V, FREF=24M,REFDIV=1             | NA  | 1000 | 1500 | Input clock cycles |

Table 3-6 Electrical Characteristics for FRAC PLL

| Parameters |                             | Symbol           | Test condition                              | Min | Typ | Max  | Unit               |
|------------|-----------------------------|------------------|---|-----|-----|------|--------------------|
|            | Input clock frequency(Frac) | F <sub>in</sub>  | F <sub>in</sub> = FREF @1.8V/0.99V          | 1   | NA  | 1200 | MHz                |
|            | VCO operating range         | F <sub>vco</sub> | F <sub>vco</sub> = Fref * FBDIV @3.3V/0.99V | 950 | NA  | 3800 | MHz                |
|            | Output clock frequency      | F <sub>out</sub> | F <sub>out</sub> = Fvco/POSTDIV @3.3V/0.99V | 19  | NA  | 3800 | MHz                |
|            | Lock time                   | T <sub>lt</sub>  | @ 3.3V/0.99V, FREF=24M,REFDIV=1             | NA  | 250 | 500  | Input clock cycles |

Notes:

- ① REF<sub>DIV</sub> is the input divider value;
- ② F<sub>B</sub><sub>DIV</sub> is the feedback divider value;
- ③ P<sub>O</sub><sub>ST</sub><sub>D</sub><sub>I</sub><sub>V</sub> is the output divider value

### 3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

| Parameters                 | Symbol           | Test condition                              | Min  | Typ  | Max  | Unit |
|----------------------------|------------------|---|------|------|------|------|
| Transmitter                |                  |   |      |      |      |      |
| Output resistance          | R <sub>OUT</sub> | Classic mode (V <sub>out</sub> = 0 or 3.3V) | 40.5 | 45   | 49.5 | ohms |
|                            |                  | HS mode (V <sub>out</sub> = 0 to 800mV)     | 40.5 | 45   | 49.5 | ohms |
| Output Capacitance         | C <sub>OUT</sub> | seen from D+ or D-                          |      |      | 3    | pF   |
| Output Common Mode Voltage | V <sub>M</sub>   | Classic (LS/FS) mode                        | 1.45 | 1.65 | 1.85 | V    |

| Parameters                           | Symbol | Test condition                                | Min   | Typ  | Max   | Unit |
|--------------------------------------|--------|---|-------|------|-------|------|
|                                      |        | HS mode                                       | 0.175 | 0.2  | 0.225 | V    |
| Differential output signal high      | VOH    | Classic (LS/FS); Io=0mA                       | 2.97  | 3.3  | 3.63  | V    |
|                                      |        | Classic (LS/FS); Io=6mA                       | 2.2   | 2.7  | NA    | V    |
|                                      |        | HS mode; Io=0mA                               | 360   | 400  | 440   | mV   |
| Differential output signal low       | VOL    | Classic (LS/FS); Io=0mA                       | -0.33 | 0    | 0.33  | V    |
|                                      |        | Classic (LS/FS); Io=6mA                       | NA    | 0.3  | 0.8   | V    |
|                                      |        | HS mode; Io=0mA                               | -40   | 0    | 40    | mV   |
| Receiver                             |        |   |       |      |       |      |
| Receiver sensitivity                 | RSENS  | Classic mode                                  |       | ±250 |       | mV   |
|                                      |        | HS mode                                       |       | ±25  |       | mV   |
| Receiver common mode                 | RCM    | Classic mode                                  | 0.8   | 1.65 | 2.5   | V    |
|                                      |        | HS mode (differential and squelch comparator) | 0.1   | 0.2  | 0.3   | V    |
|                                      |        | HS mode (disconnect comparator)               | 0.5   | 0.6  | 0.7   | V    |
| Input capacitance (seen at D+ or D-) |        |   | NA    | NA   | 3     | pF   |
| Squelch threshold                    |        |   | 100   | NA   | 150   | mV   |
| Disconnect threshold                 |        |   | 570   | 600  | 664   | mV   |

### 3.7 Electrical Characteristics for HDMI

Table 3-8 Electrical Characteristics for HDMI

| Parameters                           | Symbol   | Test condition   | Min  | Typ | Max | Unit |
|--------------------------------------|----------|------------------|------|-----|-----|------|
| Differential output signal rise time | tR       | 20~80%<br>RL=50Ω | 75   | NA  | NA  | ps   |
|                                      | tR_DATA  | 20~80%<br>RL=50Ω | 42.5 | NA  | NA  | ps   |
|                                      | tR_CLOCK | 20~80%<br>RL=50Ω | 75   | NA  | NA  | ps   |
| Differential output signal fall time | tF       | 20~80%<br>RL=50Ω | 75   | NA  | NA  | ps   |
|                                      | tF_DATA  | 20~80%<br>RL=50Ω | 42.5 | NA  | NA  | ps   |
|                                      | tF_CLOCK | 20~80%<br>RL=50Ω | 75   | NA  | NA  | ps   |

### 3.8 Electrical Characteristics for Audio CODEC interface

Table 3-9 Electrical Characteristics for Audio CODEC

Test conditions: AVDD = 1.8V, DVDD = 0.8V, TA = 25°C, 1KHz Sine Input, Fs = 48KHz

| Parameters                | Symbol           | Test condition             | Min  | Typ  | Max  | Units |
|---------------------------|------------------|----------------------------|------|------|------|-------|
| Operating Condition       |                  |                            |      |      |      |       |
| Analog Supply             | AVDD             |                            | 1.62 | 1.8  | 1.98 | V     |
| DAC Line Output           |                  |                            |      |      |      |       |
| Programmable Gain         | G <sub>DRV</sub> |                            | -39  | NA   | 6    | dB    |
| Gain Step Size            |                  |                            | NA   | 1.5  | NA   | dB    |
| Signal to Noise Ratio     | SNR              | A-weighted                 | NA   | 93   | NA   | dB    |
| Total Harmonic Distortion | THD              | -3dBFS output<br>600Ω load | NA   | -84  | NA   | dB    |
| Power Supply Rejection    | PSRR             | 1KHz                       | NA   | 55   | NA   | dB    |
| Power Consumption         |                  |                            |      |      |      |       |
| Standby                   |                  |                            | NA   | 0.05 | NA   | mA    |
| Stereo Playback           |                  | Quiescent output           | NA   | 5    | NA   | mA    |

### 3.9 Electrical Characteristics for SARADC

Table 3-10 Electrical Characteristics for SARADC

| Parameters                         | Symbol          | Test condition                                  | Min | Typ | Max | Unit |
|------------------------------------|-----------------|---|-----|-----|-----|------|
| Resolution                         |                 |   | NA  | 10  | NA  | bit  |
| Effective Number of Bit            | ENOB            |   | NA  | 9   | NA  | bit  |
| Differential Non-Linearity         | DNL             |   | -1  | NA  | +1  | LSB  |
| Integral Non-Linearity             | INL             |   | -2  | NA  | +2  | LSB  |
| Input Capacitance                  | C <sub>IN</sub> |   | NA  | 8   | NA  | pF   |
| Sampling Rate                      | f <sub>S</sub>  |   | NA  | NA  | 1   | MS/s |
| Spurious Free Dynamic Range        | SFDR            | f <sub>S</sub> =1MS/S f <sub>OUT</sub> =1.17KHZ | NA  | 61  | NA  | dB   |
| Signal to Noise and Harmonic Ratio | SNDR            |   | NA  | 56  | NA  | dB   |

### 3.10 Electrical Characteristics for TSADC

Table 3-11 Electrical Characteristics for TSADC

| Parameters                   | Symbol             | Test condition | Min | Typ | Max | Unit |
|------------------------------|--------------------|----------------|-----|-----|-----|------|
| Accuracy from -40°C to 125°C | T <sub>JACC</sub>  |                | NA  | NA  | ±3  | °C   |
| Sensing Temperature Range    | T <sub>RANGE</sub> |                | -40 | NA  | 125 | °C   |
| Resolution                   | T <sub>LSB</sub>   |                | NA  | 0.6 | NA  | °C   |

## Chapter 4 Thermal Management

### 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125°C.

### 4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

| Parameter                              | Symbol        | Typical | Unit   |
|--|---------------|---------|--------|
| Junction-to-ambient thermal resistance | $\theta_{JA}$ | 22.8    | (°C/W) |
| Junction-to-board thermal resistance   | $\theta_{JB}$ | 9.3     | (°C/W) |
| Junction-to-case thermal resistance    | $\theta_{JC}$ | 6.87    | (°C/W) |

Note: The PCB is 4 layers, 114.3 mm.\*101.6 mm