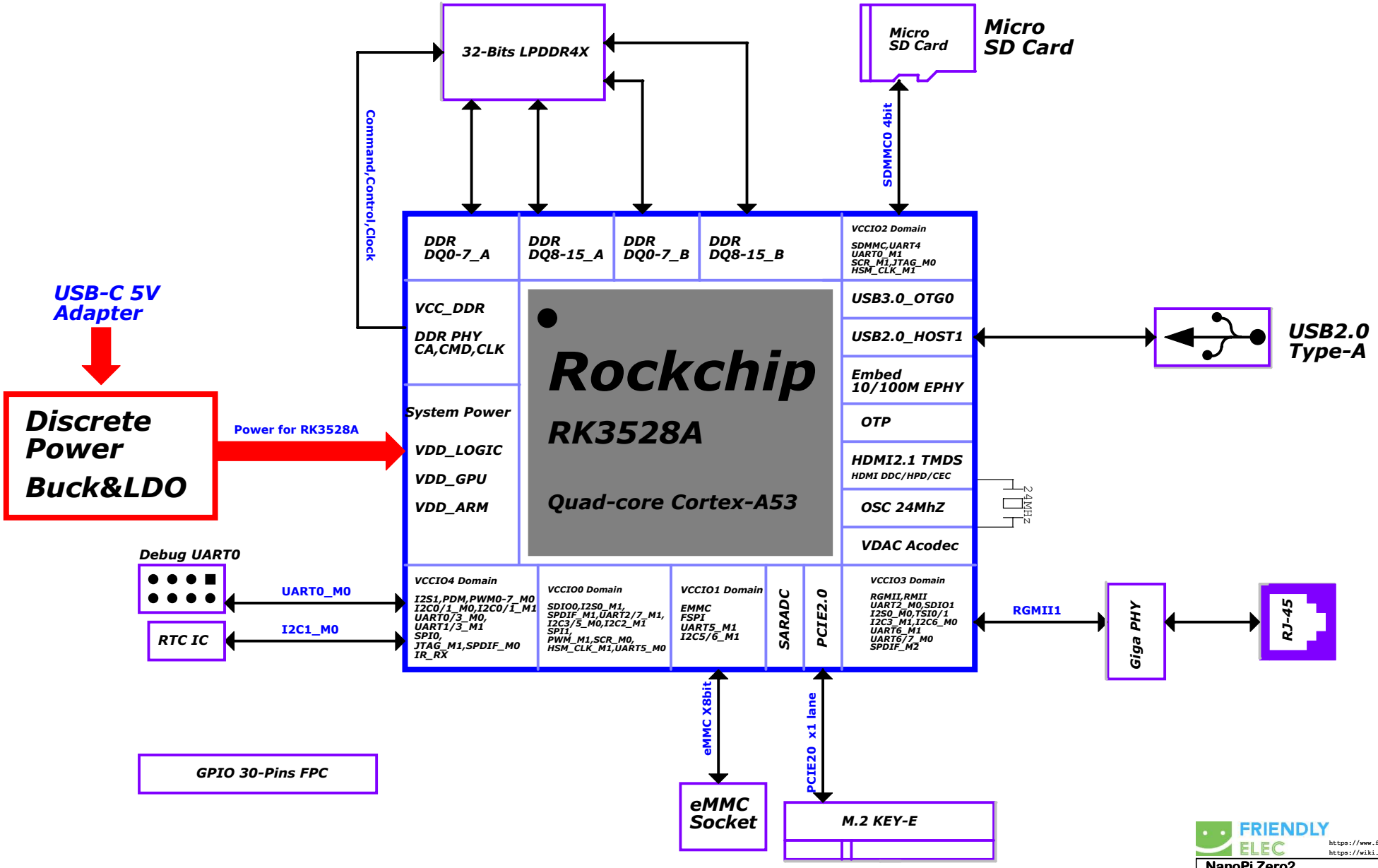
# NanoPi Zero2

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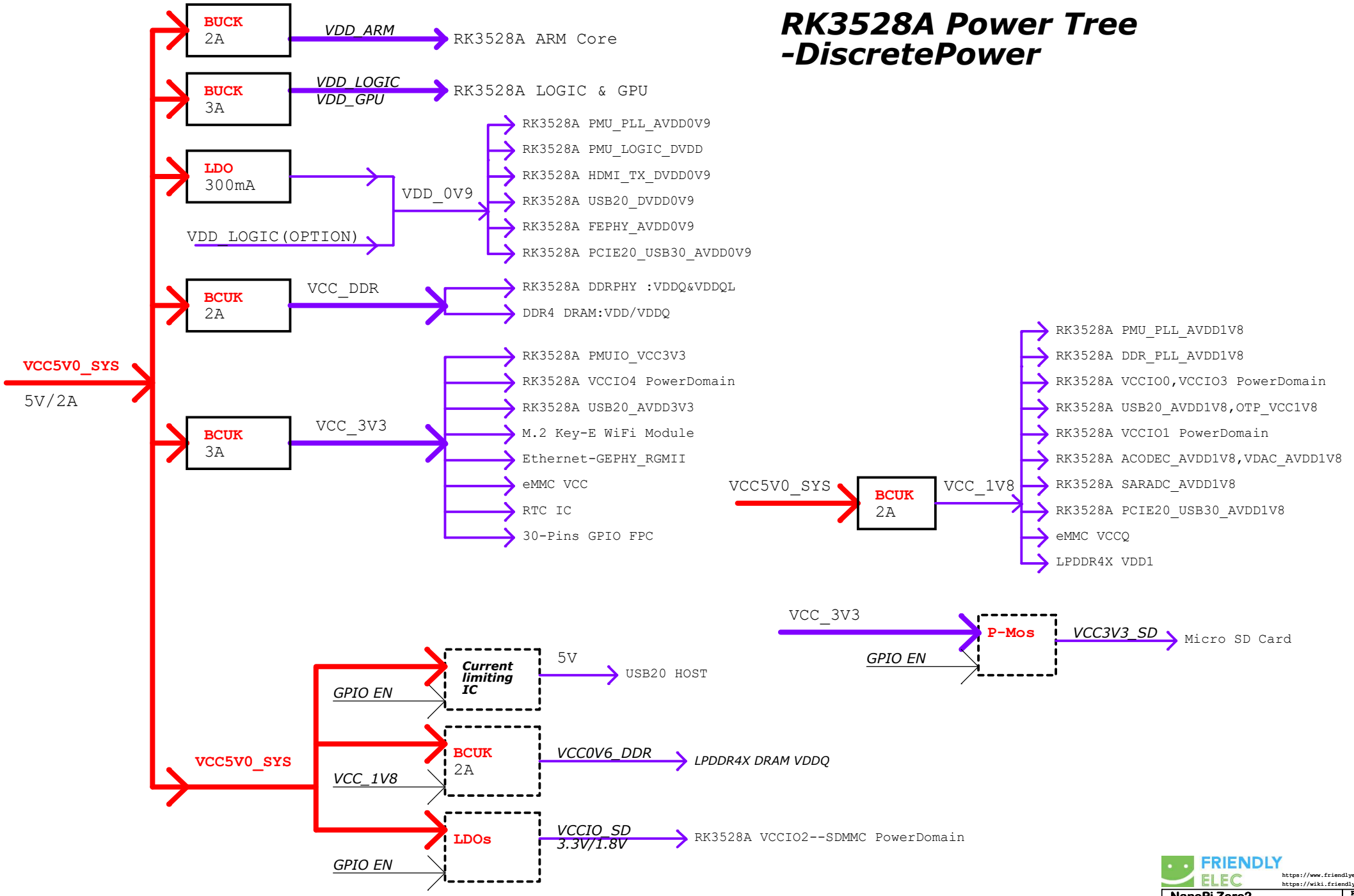
| NanoPi Zero2 | Rev 2407 |
|---|---|
| Size A3 | Page Name 01.Block Diagram |
| Date: Monday, July 22, 2024 | Sheet: 1 / 16 |

# RK3528A Power Tree -DiscretePower

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|---|---|
| Size A3 | Page Name 02.Power Tree-DiscretePower |
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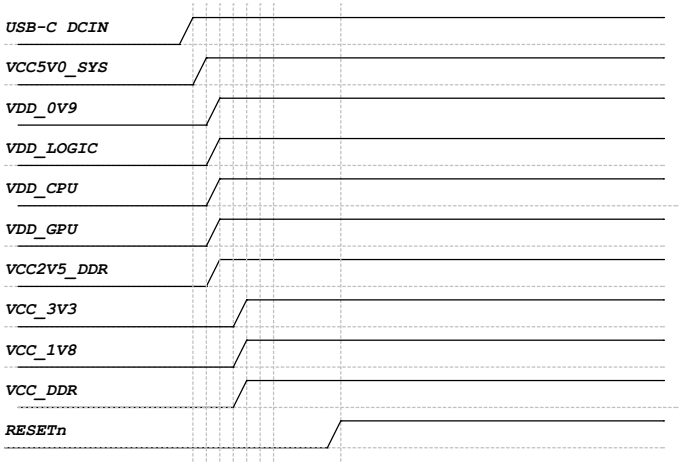
# DiscretePower Power Sequence




| Power Supply | EXT BUCK&LDO | Supply Limit | Power Name | Time Slot | Default Voltage | Default ON/OFF | Sleep ON/OFF | Peak Current | Sleep Current |
|---|---|---|---|---|---|---|---|---|---|
| VCC5V0_SYS | BUCK1 | 2.0A | VDD_LOGIC<br>VDD_GPU | Slot:1 | 0.9V | ON | ON | TBD | TBD |
| VCC5V0_SYS | BUCK2 | 2.0A | VDD_ARM | Slot:1 | 0.95V | ON | ON | TBD | TBD |
| VCC5V0_SYS | LDO1 | 0.3A | VDD_0V9 | Slot:1 | 0.9V | ON | ON | TBD | TBD |
| VCC_3V3 | LDO2 | 1.0A | VCC_1V8 | Slot:2 | 1.8V | ON | ON | TBD | TBD |
| VCC5V0_SYS | BUCK3 | 2.0A | VCC_3V3 | Slot:2 | 3.3V | ON | ON | TBD | TBD |
| VCC5V0_SYS | BUCK4 | 2.0A | VCC_DDR | Slot:2 | ADJ<br>FB=0.6V | ON | ON | TBD | TBD |
| USB-C DCIN | / | 3.0A | VCC5V0_SYS | Slot:0 | 5.0V | ON | ON | TBD | TBD |

# IO Power Domain Map

| IO Domain | Pin Num | Support IO Voltage | | Actual assigned IO Domain Voltage | | | Notes |
|---|---|---|---|---|---|---|---|
| | | 3.3V | 1.8V | Supply Power Net Name | Power Source | Voltage | |
| PMUIO | Pin 1J13 | ✓ | ✗ | VCCIO_PMU | VCC_3V3 | 3.3V | |
| VCCIO0 | Pin 1N6 | ✓ | ✓ | VCCIO0 | VCCIO_WL | 1.8V | |
| VCCIO1 | Pin 1P8 | ✓ | ✓ | VCCIO1 | VCCIO_FLASH | 1.8V/3.3V | Select as required |
| VCCIO2 | Pin 1B14 | ✓ | ✓ | VCCIO2 | VCCIO_SD | 1.8V/3.3V | SD3.0 Voltage=1.8V SD2.0 Voltage=3.3V<br>3.3V-->1.8V |
| VCCIO3 | Pin 1M13 | ✓ | ✓ | VCCIO3 | VCC_1V8<br>VCC_3V3 | 1.8V<br>3.3V | Select as required |
| VCCIO4 | Pin 1J3 | ✓ | ✓ | VCCIO4 | VCC_3V3 | 3.3V | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

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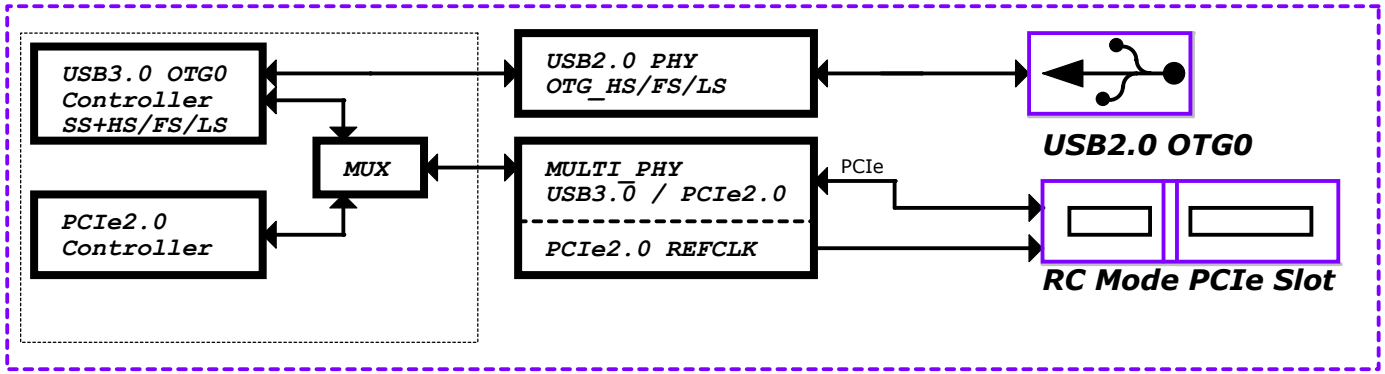
| Size A3 | Page Name 03.Power Sequence-DiscretePower |
| Date: Monday, July 22, 2024 | Sheet: 3 / 16 |

# USB3/PCIE Fun Map

## Case1: USB2.0 OTG0 + PCIe2.0 x1 Lane



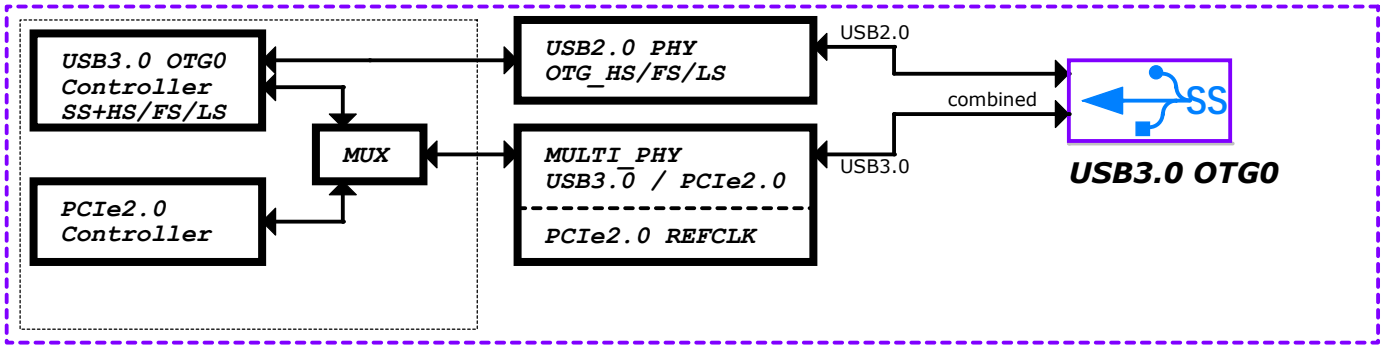

**Note 1:**

USB3.0 OTG is backward compatible with USB2.0, it needs to occupy the USB2.0 OTG signal pair.

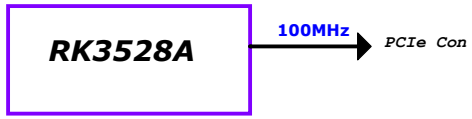
**Note 2:**

MULTI PHY can be configured for PCIe2.0 or USB3.0 interface.
PCIe2.0 only work in RC mode,
and support both internal/external clock.

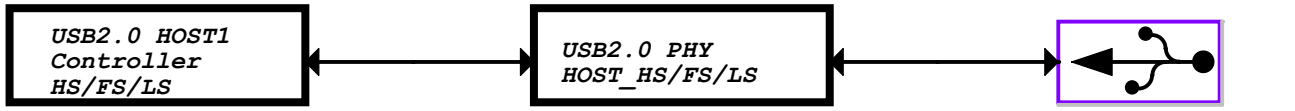
## Case2: USB3.0 OTG0




## PCIe2.0 REFCLK




## USB2.0 HOST1

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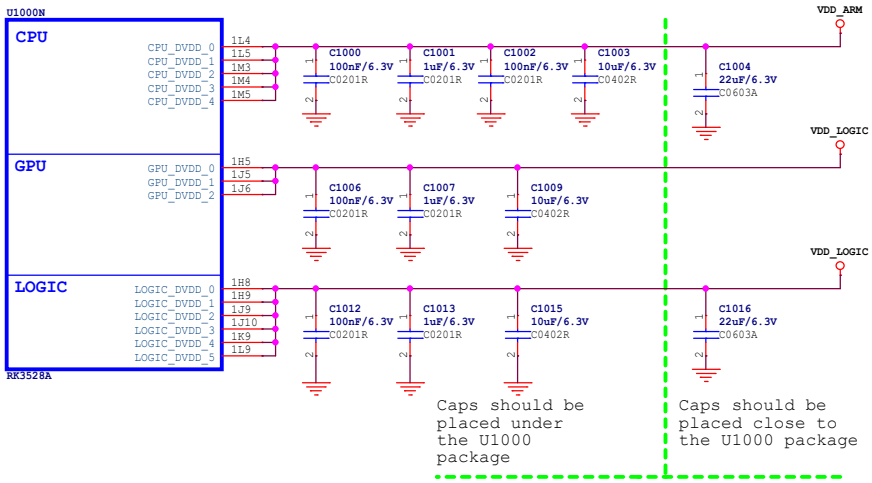
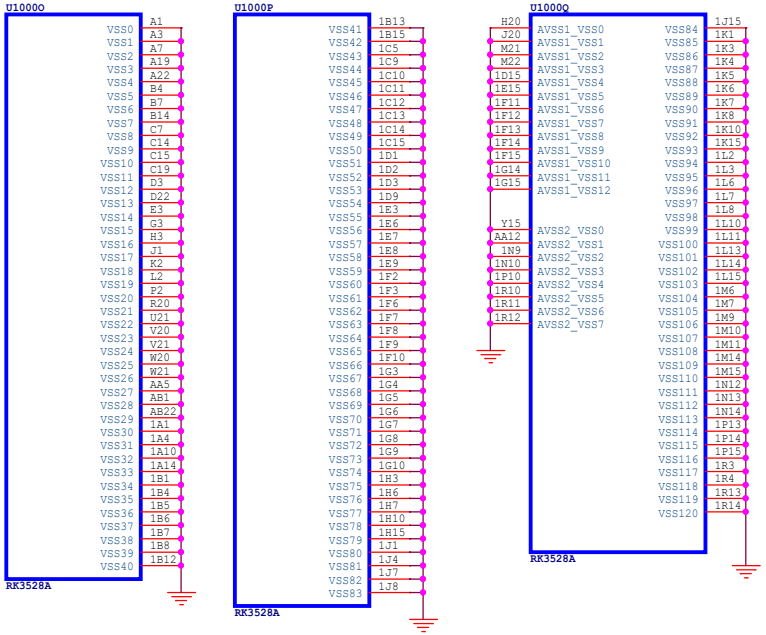
|---|---|
| Size A3 | Page Name 04.USB3/PCIE Fun Map |
| Date: Monday, July 22, 2024 | Sheet: 4 / 16 |

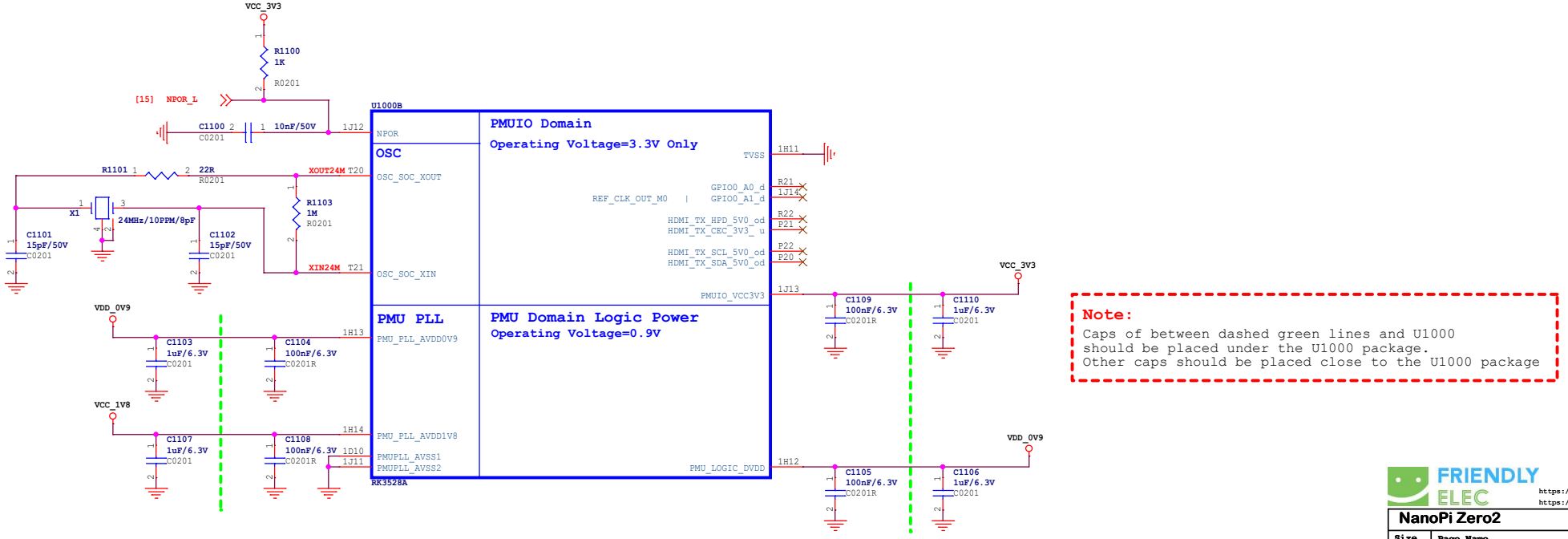
# RK3528A_N(POWER)




**Note:**
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

# RK3528A_O/P/Q(GND)




**Note:**
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| NanoPi Zero2 | Rev 2407 |
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| Size A3 | Page Name 05.RK3528A Power/OSC/PLL/PMUIO |
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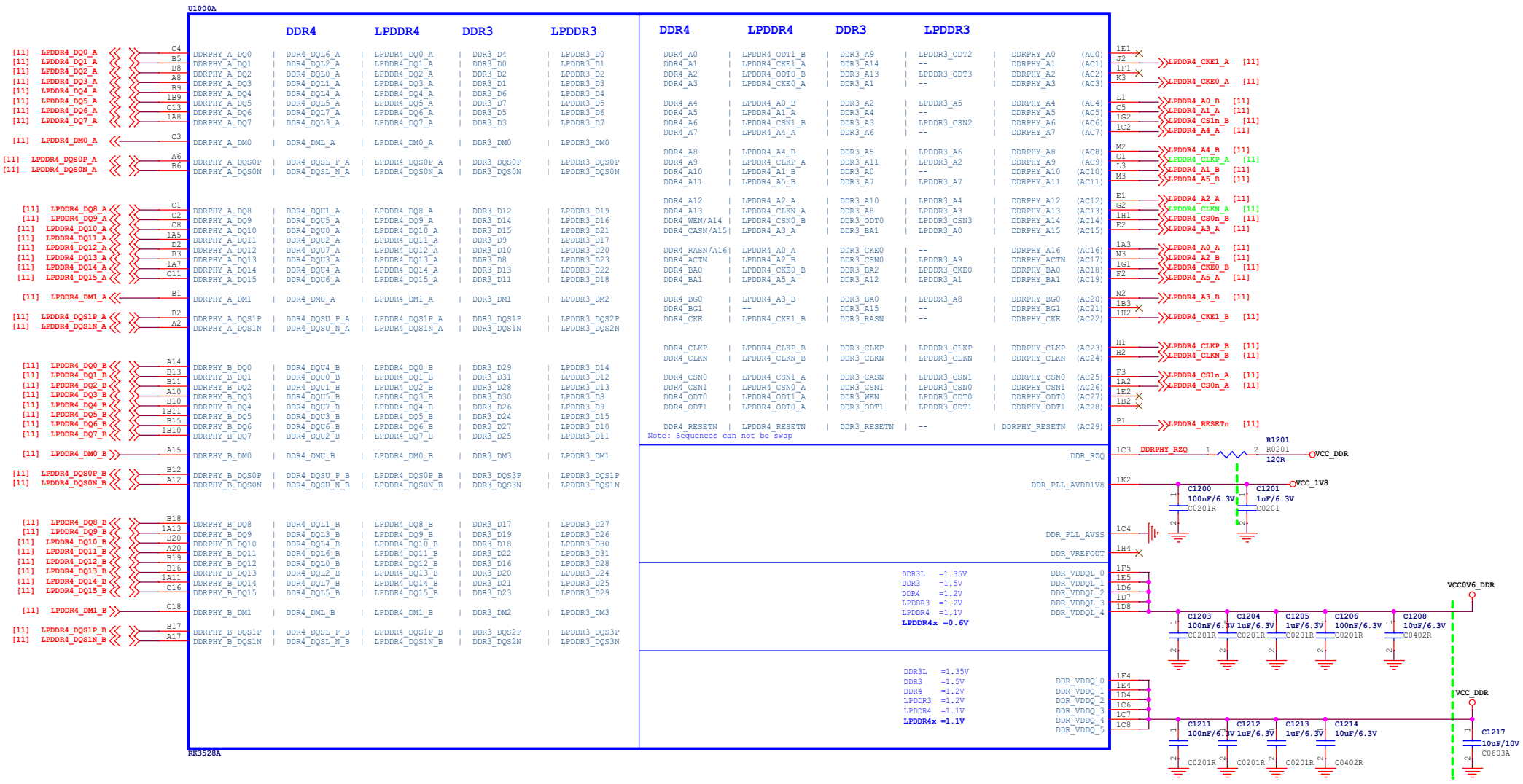
# RK3528A_A(DDR PHY)

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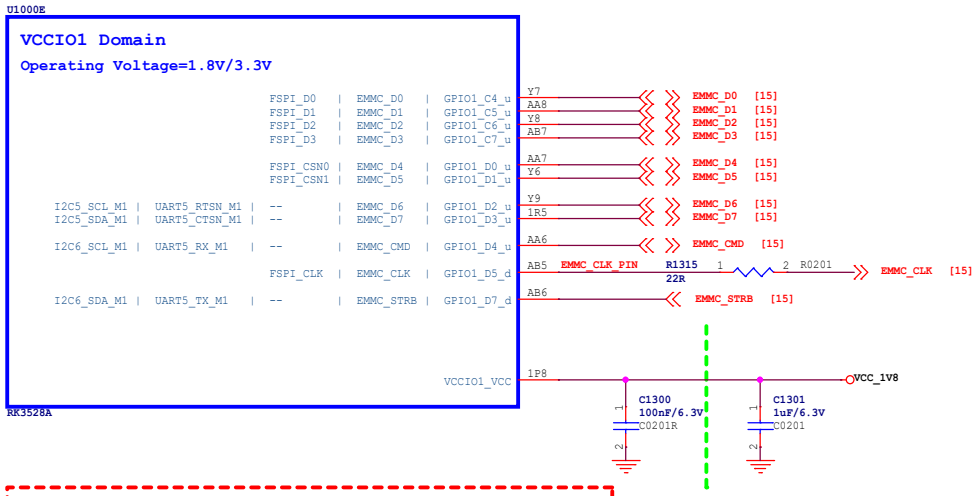
|---|---|
| Size A3 | Page Name 06.RK3528A DDR Controller |
| Date: Monday, July 22, 2024 | Sheet: 6 / 16 |

# RK3528A_E(VCCIO1 Domain)




**Note:**
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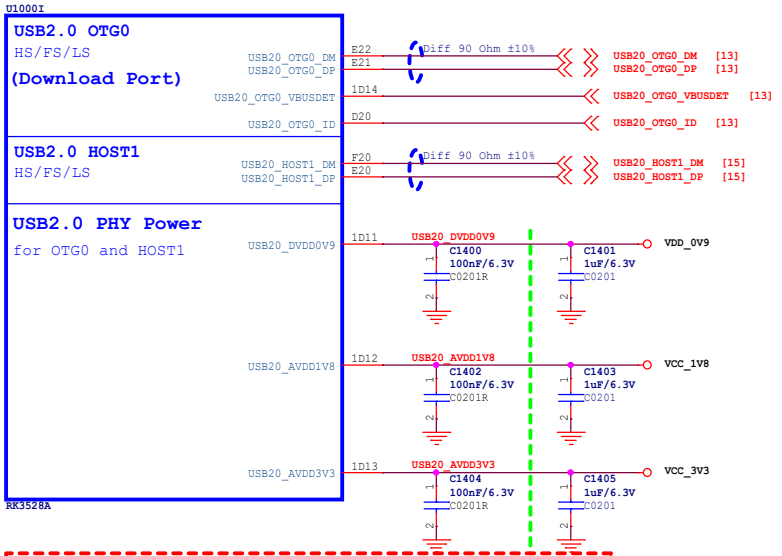
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

# RK3528A_I(USB2.0 OTG/HOST)




**Note:**
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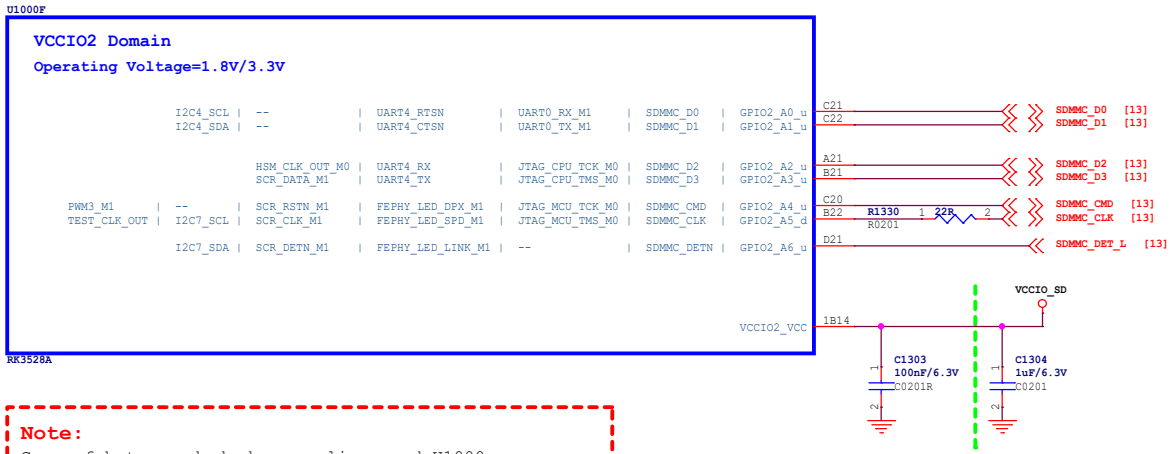
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

# RK3528A_F(VCCIO2 Domain)




**Note:**
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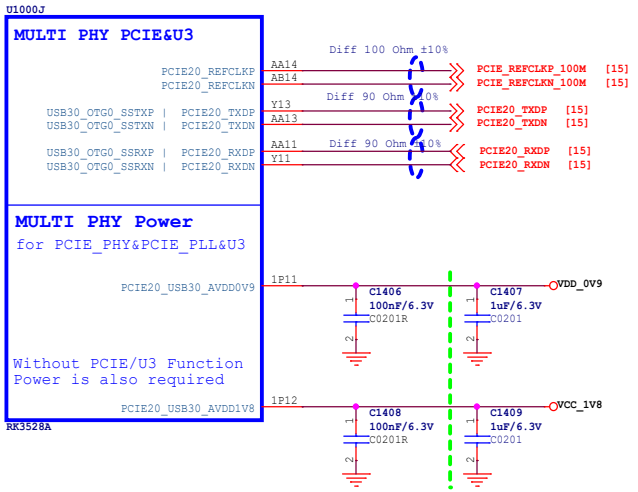
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

# RK3528A_J(PCIE2.0/U3 PHY)




**Note:**
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| NanoPi Zero2 | Rev 2407 |
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| Size A3 | Page Name 07.RK3528A FLASH/SD/USB/PCIE |
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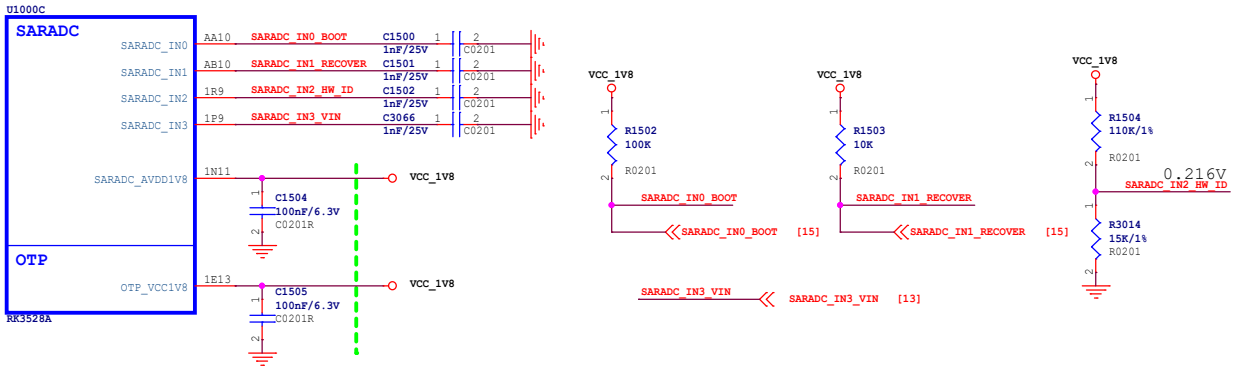
# RK3528A_C(Saradc/OTP)




**Note:**
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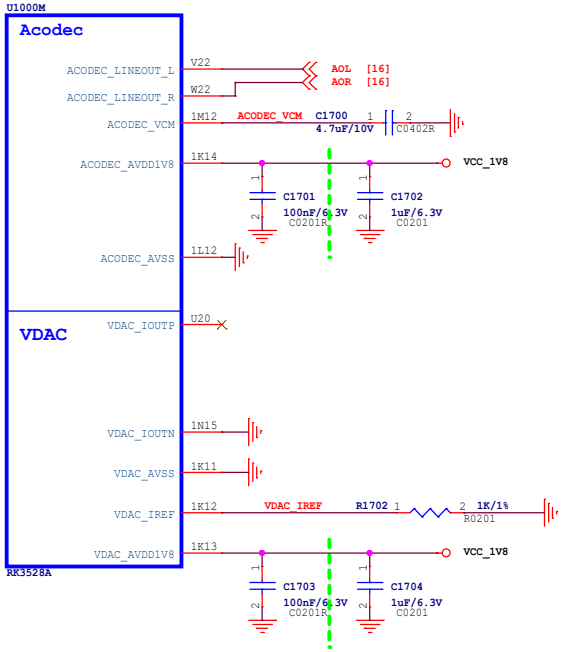
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

***TABLE***

| Item | Rup | Rdown | ADC | BOOT MODE |
|---|---|---|---|---|
| *LEVEL1* | *DNP* | *100K* | *0* | *USB (Maskrom mode)* |
| *LEVEL2* | *100K* | *12K* | *114* | |
| *LEVEL3* | *100K* | *27K* | *228* | *FSPI--USB* |
| *LEVEL4* | *100K* | *51K* | *342* | |
| *LEVEL5* | *100K* | *82K* | *456* | |
| *LEVEL6* | *100K* | *120K* | *570* | *EMMC--USB* |
| *LEVEL7* | *100K* | *200K* | *683* | *EMMC--SD Card--USB* |
| *LEVEL8* | *100K* | *330K* | *796* | *SD Card--USB* |
| *LEVEL9* | *100K* | *820K* | *910* | |
| *LEVEL10* | *100K* | *DNP* | *1023* | *FSPI--EMMC--SD Card--USB* |

# RK3528A_M(Acodec/VDAC)

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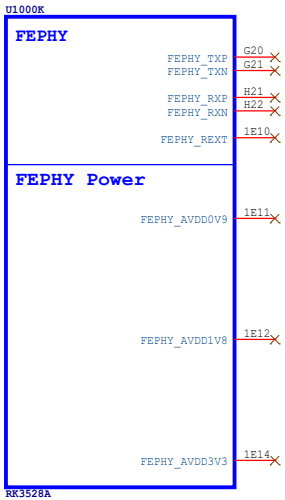
# RK3528A_K(Embed FEPHY)

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| Size A3 | Page Name 08.RK3528A SARADC/AV/FE |
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# RK3528A_G(VCCIO3 Domain)

U1000G

**VCCIO3 Domain**

**Operating Voltage=1.8V/3.3V**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | TSI0_D7 | UART2_RX_M0 | RGMII1_TXD1 | GPIO3_A0_d | AA19 → GMAC1_TXD1 [14] |
| | | | | TSI0_D6 | UART2_TX_M0 | RGMII1_TXD0 | GPIO3_A1_d | Y18 → GMAC1_TXD0 [14] |
| | | | | TSI0_D5 | UART2_RTSN_M0 | RGMII1_RXD1 | GPIO3_A2_d | Y17 → GMAC1_RXD1 [14] |
| | | | | TSI0_D4 | UART2_CTSN_M0 | RGMII1_RXD0 | GPIO3_A3_d | AA18 → GMAC1_RXD0 [14] |
| | | UART6_CTSN | -- | TSI1_D0 | SDIO1_CLK | RGMII1_TXCLK | GPIO3_A4_d | AA22 GMAC1_TXCLK_PIN R1902 1 2 22R R0201 → GMAC1_TXCLK [14] |
| | | UART6_RTSN | -- | TSI1_CLKIN | SDIO1_CMD | RGMII1_RXCLK | GPIO3_A5_d | Y20 → GMAC1_RXCLK [14] |
| PCIE_CLKREQN_M0 | -- | UART6_TX_M0 | -- | TSI1_VALID | SDIO1_D0 | RGMII1_RXD3 | GPIO3_A6_d | AB21 → GMAC1_RXD3 [14] |
| PCIE_WAKEN_M0 | -- | UART6_RX_M0 | -- | TSI1_SYNC | SDIO1_D1 | RGMII1_RXD2 | GPIO3_A7_d | AA20 → GMAC1_RXD2 [14] |
| PCIE_PERSTN_M0 | -- | UART7_CTSN_M0 | -- | -- | SDIO1_D2 | RGMII1_TXD3 | GPIO3_B0_d | Y19 → GMAC1_TXD3 [14] |
| | | UART7_RTSN_M0 | -- | TSI0_D0 | SDIO1_D3 | RGMII1_TXD2 | GPIO3_B1_d | AA21 → GMAC1_TXD2 [14] |
| | | UART7_TX_M0 | I2C6_SCL_M0 | TSI0_CLKIN | SDIO1_PWREN | -- | GPIO3_B2_d | 1R15 / Y21 |
| | | UART7_RX_M0 | I2C6_SDA_M0 | TSI0_VALID | SDIO1_DETN | -- | GPIO3_B3_d | |
| | | | | TSI0_SYNC | I2S0_MCLK_M0 | RGMII1_CLK | GPIO3_B4_d | Y16 → GMAC1_MCLKINOUT [14] |
| | | | | TSI0_D1 | I2S0_SCLK_M0 | ETH_CLK_25M_OUT | GPIO3_B5_d | AB17 |
| | | | | TSI0_D2 | I2S0_LRCK_M0 | RGMII1_MDC | GPIO3_B6_d | AA17 → GMAC1_MDC [14] |
| | | | | TSI0_D3 | I2S0_SDI_M0 | RGMII1_MDIO | GPIO3_B7_d | AA16 → GMAC1_MDIO [14] |
| | | | | TSI0_FAIL | I2S0_SDO_M0 | RGMII1_TXEN | GPIO3_C0_d | AB16 → GMAC1_TXEN [14] |
| PWM6_M2 | -- | UART6_TX_M1 | I2C3_SCL_M1 | -- | -- | RGMII1_TXER | GPIO3_C1_d | AA15 |
| | | | | | | RGMII1_RXDV_CRS | GPIO3_C2_d | AB19 → GMAC1_RXDV_CRS [14] |
| PWM5_M1 | SPDIF_TX_M2 | UART6_RX_M1 | I2C3_SDA_M1 | REF_CLK_OUT_M1 | CLK_32K_OUT_M0 | -- | GPIO3_C3_d | AB20 |

RK3528A

VCCIO3_VCC 1M13

C1902 100nF/6.3V C0201R

C1903 1uF/6.3V C0201

VCC_1V8

# RK3528A_H(VCCIO4 Domain)

U1000H

**VCCIO4 Domain**

**Operating Voltage=1.8V/3.3V**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| PMU_DEBUG | -- | I2C0_SDA_M1 | -- | SPDIF_TX_M0 | -- | -- | GPIO4_A0_d | R3 → GPIO4_A0 [16] |
| | | I2C0_SCL_M1 | -- | SDMMC0_PWREN | -- | -- | GPIO4_A1_d | R1 → SDMMC_PWREN_L [13] |
| | | I2C1_SDA_M0 | UART3_RTSN | -- | -- | I2S1_SDI3 | GPIO4_A2_d | U2 → I2C1_SDA_M0 [13] |
| | | I2C1_SCL_M0 | UART3_CTSN | -- | -- | I2S1_SDI2 | GPIO4_A3_d | U3 → I2C1_SCL_M0 [13] |
| | | UART1_CTSN | -- | -- | PDM_CLK1 | I2S1_MCLK | GPIO4_A4_d | 1M2 → GPIO4_A4 [16] |
| | | UART1_RTSN | -- | -- | -- | I2S1_SCLK | GPIO4_A5_d | 1P2 → GPIO4_A5 [16] |
| | | UART1_TX_M0 | -- | -- | -- | I2S1_LRCK | GPIO4_A6_d | 1M1 → GPIO4_A6 [16] |
| | | UART1_RX_M0 | -- | -- | -- | I2S1_SDO0 | GPIO4_A7_d | 1P3 → GPIO4_A7 [16] |
| | | | UART3_RX_M0 | -- | -- | I2S1_SDO1 | GPIO4_B0_d | 1R2 → LED_SYS [13] |
| | | | UART3_TX_M0 | -- | PDM_SDI1 | I2S1_SDO2 | GPIO4_B1_d | 1N2 → LED1 [13] |
| | | | | SPI0_MOSI | PDM_SDI0 | I2S1_SDO3 | GPIO4_B2_d | 1N3 / W3 |
| | | | | SPI0_MISO | PDM_SDI2 | I2S1_SDI1 | GPIO4_B3_d | |
| | | | | SPI0_CLK | -- | I2S1_SDI0 | GPIO4_B4_d | R2 → GPIO4_B4 [16] |
| | | FEPHY_LED_DPX_M0 | -- | -- | PDM_CLK0 | -- | GPIO4_B5_d | Y1 → USB20_HOST1_PWREN [15] |
| | | | | SPI0_CSN0 | -- | PWR_CTRL1 | GPIO4_B6_u | 1L1 → SDMMC_VOL_CTRL_H [13] |
| PWM4_M0 | -- | FEPHY_LED_SPD_M0 | UART3_RX_M1 | -- | -- | -- | GPIO4_B7_d | V3 / Y2 |
| PWM5_M0 | -- | FEPHY_LED_LINK_M0 | UART3_TX_M1 | -- | -- | -- | GPIO4_C0_d | |
| PWM6_M0 | -- | -- | -- | SPI0_CSN1 | PDM_SDI3 | -- | GPIO4_C1_d | W2 → RTC_INT_L [13] |
| PWM7_M0 | -- | -- | -- | -- | -- | PWR_CTRL0 | GPIO4_C2_d | P3 → GMAC1_RSTn_L [14] |
| PWM0_M0 | -- | -- | -- | GPU_AVS | -- | I2C0_SDA_M0 | GPIO4_C3_d | 1N1 → GPIO4_C3 [16] |
| PWM1_M0 | -- | -- | -- | ARM_AVS | -- | I2C0_SCL_M0 | GPIO4_C4_d | V1 → PWM1_M0_ARM [12] |
| PWM2_M0 | -- | UART1_TX_M1 | -- | -- | -- | I2C1_SCL_M1 | GPIO4_C5_d | 1P1 → PWM2_M0_LOGIC [12] |
| PWM3_M0 | -- | UART1_RX_M1 | -- | -- | -- | I2C1_SDA_M1 | GPIO4_C6_d | AA1 → GPIO4_C6 [16] |
| | | | UART0_RX_M0 | JTAG_MCU_TMS_M1 | JTAG_CPU_TMS_M1 | -- | GPIO4_C7_u | T3 → UART0_RX_M0_DEBUG [13] |
| | | | UART0_TX_M0 | JTAG_MCU_TCK_M1 | JTAG_CPU_TCK_M1 | -- | GPIO4_D0_d | T2 → UART0_TX_M0_DEBUG [13] |

RK3528A

VCCIO4_VCC 1J3

C1904 100nF/6.3V C0201R

C1905 1uF/6.3V C0201

VCC_3V3

I2C1_SDA_M0 R3880 1 2 2.2K R0201

I2C1_SCL_M0 R3881 1 2 2.2K R0201

VCC_3V3

**DiscretePower**

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
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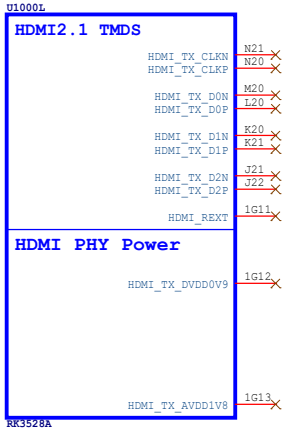
|---|---|---|
| NanoPi Zero2 | | Rev 2407 |
| Size A3 | Page Name 09.RK3528A GPIO3/GPIO4 | |
| Date: Monday, July 22, 2024 | | Sheet: 9 / 16 |

# RK3528A_L(HDMI PHY)

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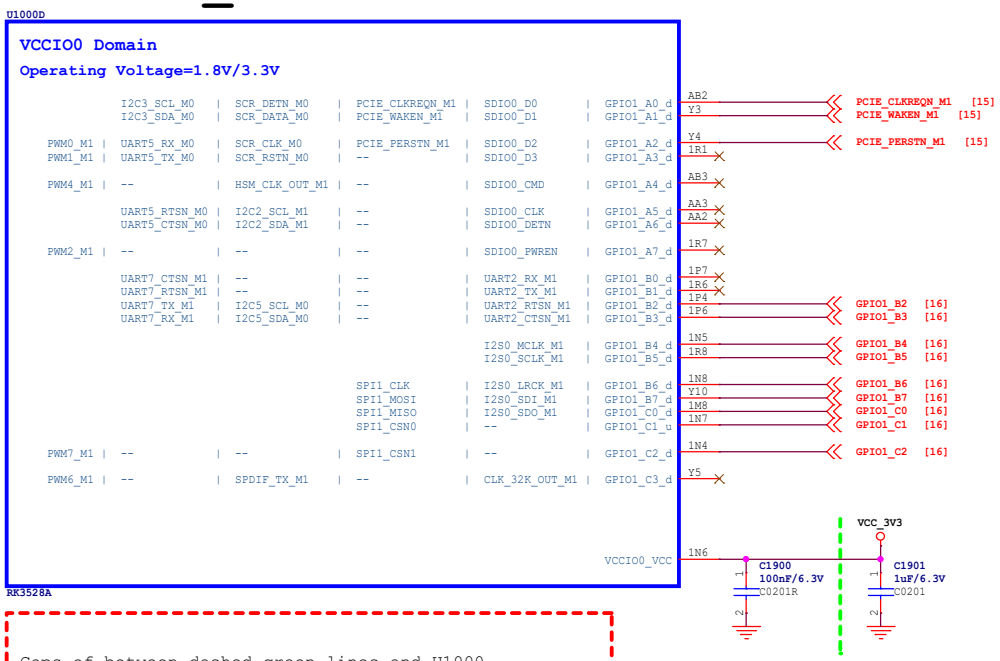
# RK3528A_D(VCCIO0 Domain)

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Other caps should be placed close to the U1000 package

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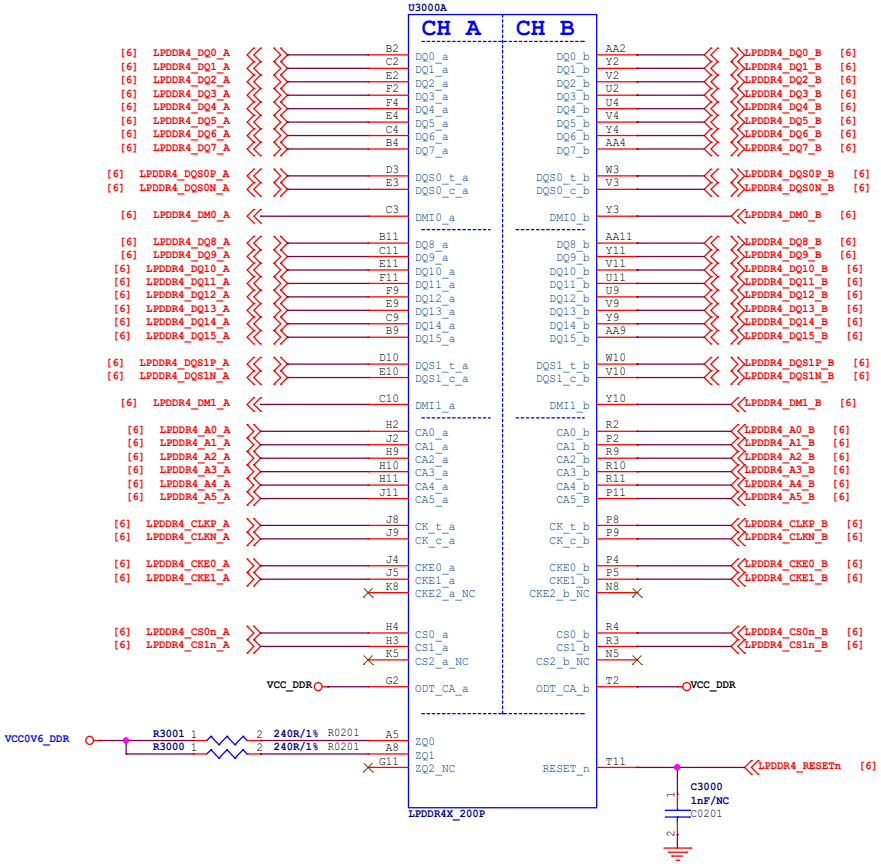
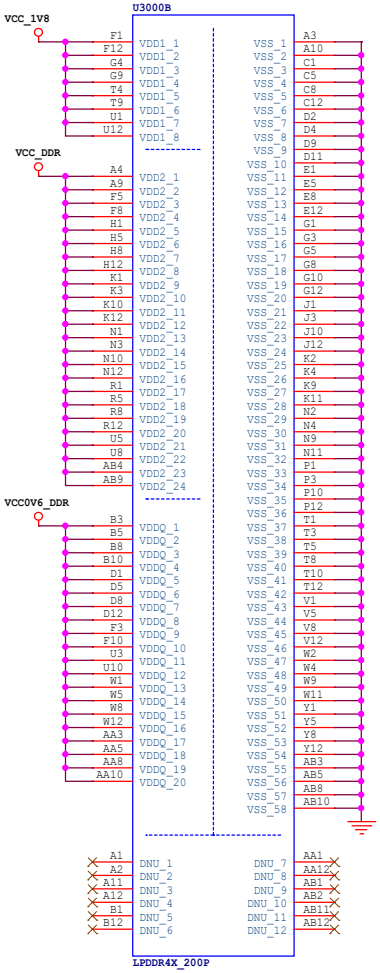
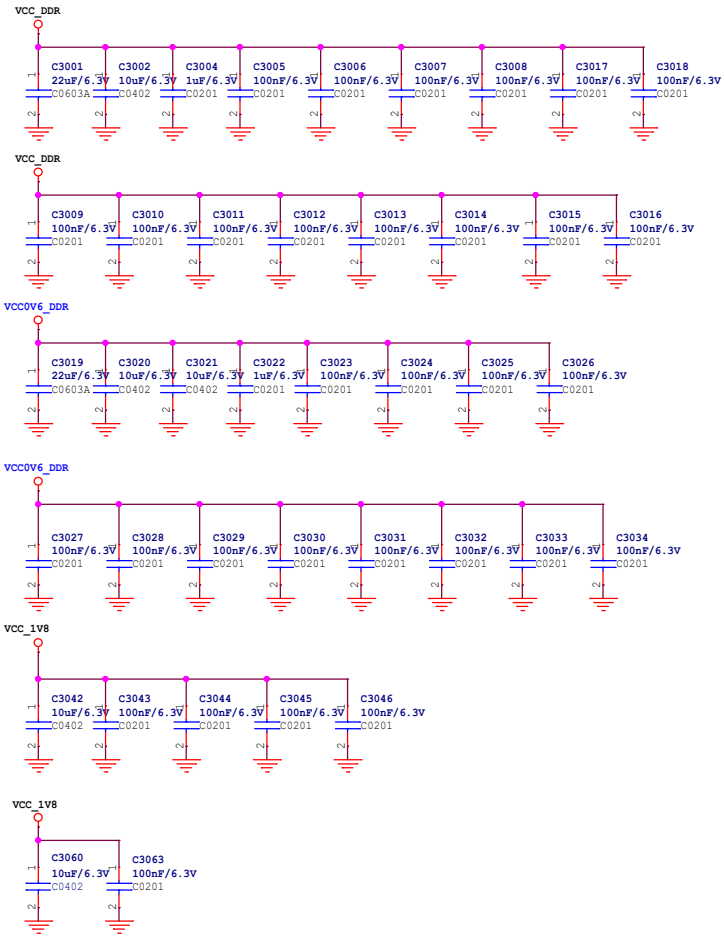
|---|---|
| Size A3 | Page Name 10.RK3528A HDMI/GPIO1 |
| Date: Monday, July 22, 2024 | Sheet: 10/ 16 |

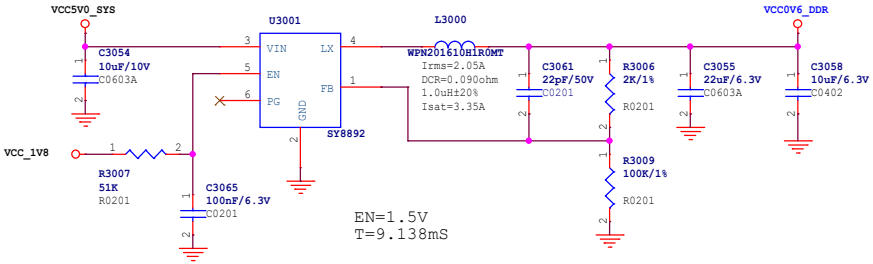
# LPDDR4X 200Ball




## VCC0V6_DDR

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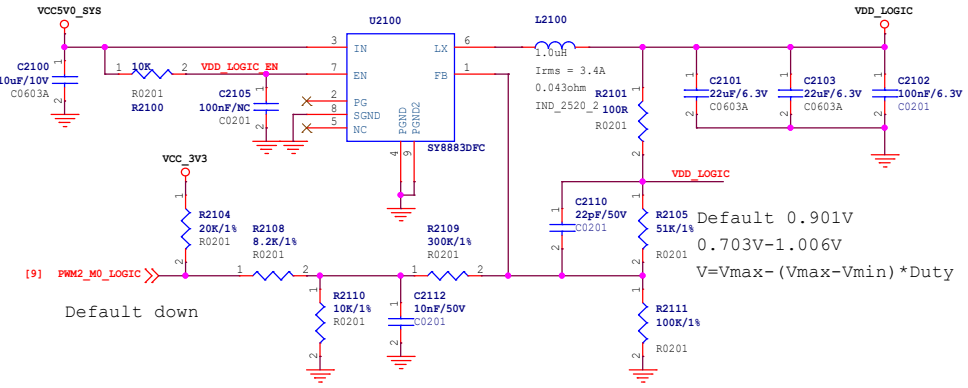
| Size A3 | Page Name 11.DRAM-LPDDR4X_1X32bit_200P |
| Date: Monday, July 22, 2024 | Sheet: 11/ 16 |

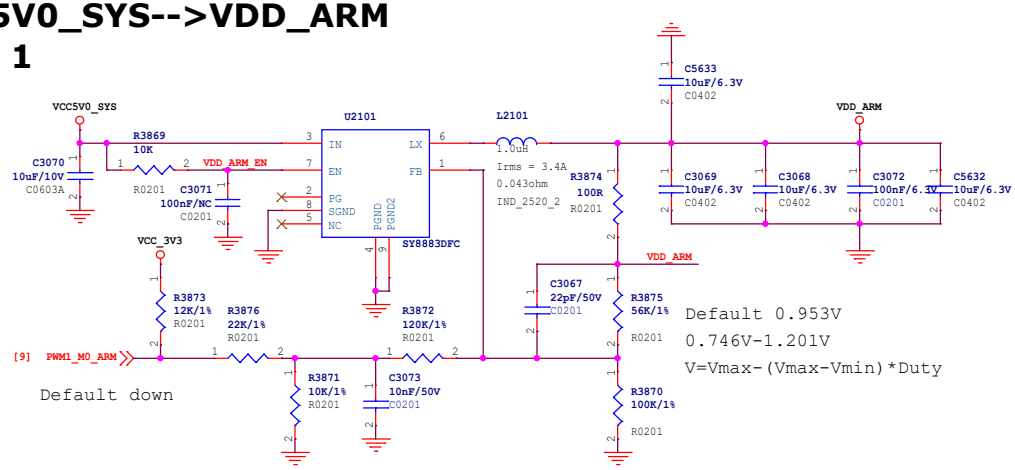
## VCC5V0_SYS-->VDD_LOGIC

### Step 1




## VCC5V0_SYS-->VDD_ARM

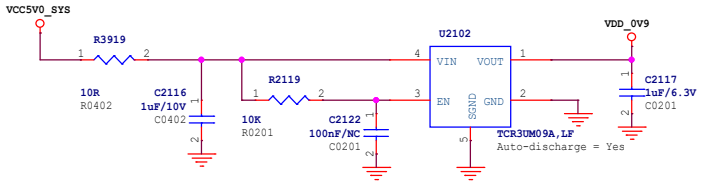
### Step 1




## VCC5V0_SYS-->VDD_0V9

### Step 1

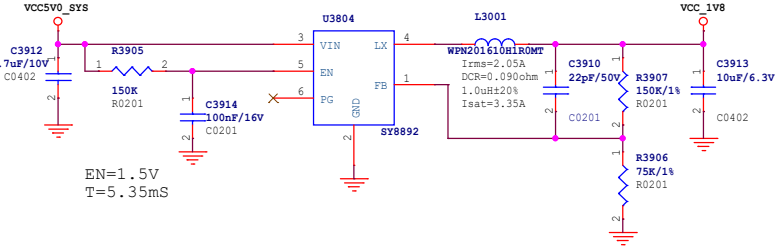
Note:
When LAYOUT, a star must be used,
Branch to each load




## VCC_3V3->VCC_1V8

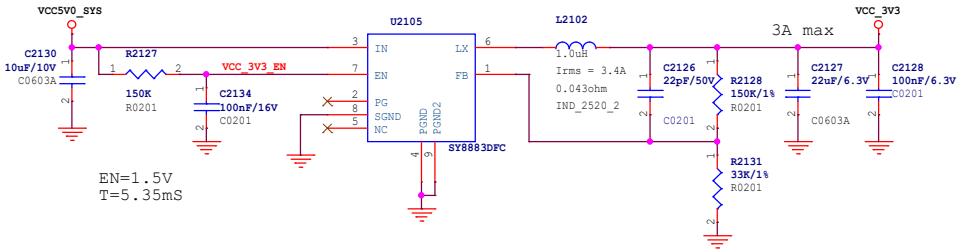
### Step 2

Note:
When LAYOUT, a star must be used,
Branch to each load



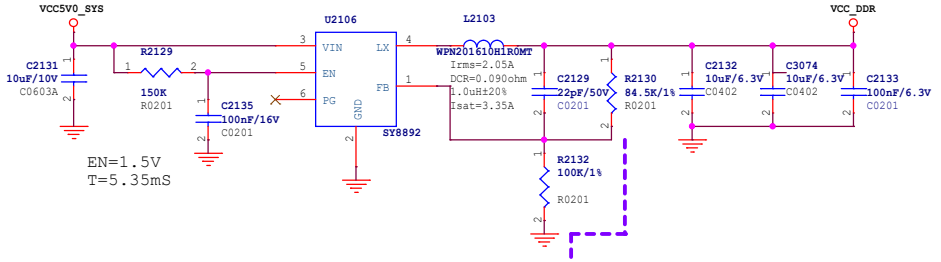

## VCC5V0_SYS-->VCC_3V3

### Step 2




## VCC5V0_SYS-->VCC_DDR

### Step 2




| | | |
|---|---|---|
| DDR4 | 1.20V | 100K 1% |
| ***LPDDR4/4x*** | 1.10V | 84.5K 1% |
| DDR3 | 1.5V | 150K 1% |
| DDR3L | 1.35V | 127K 1% |
| LPDDR3 | 1.25V | 110K 1% |

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| | | |
|---|---|---|
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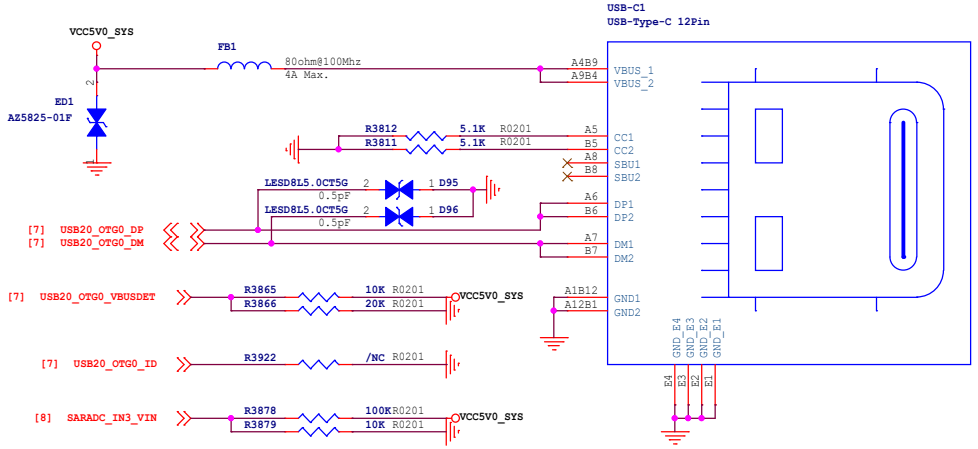
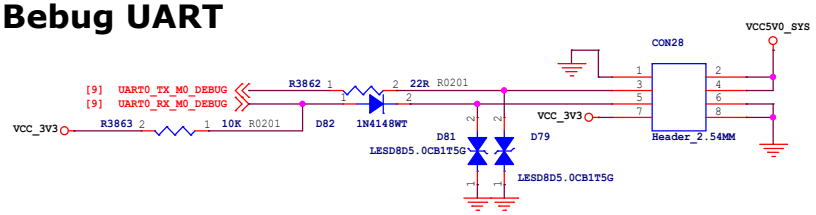
| Size A3 | Page Name 12.Power-DiscretePower | |
| Date: Monday, July 22, 2024 | | Sheet: 12/ 16 |

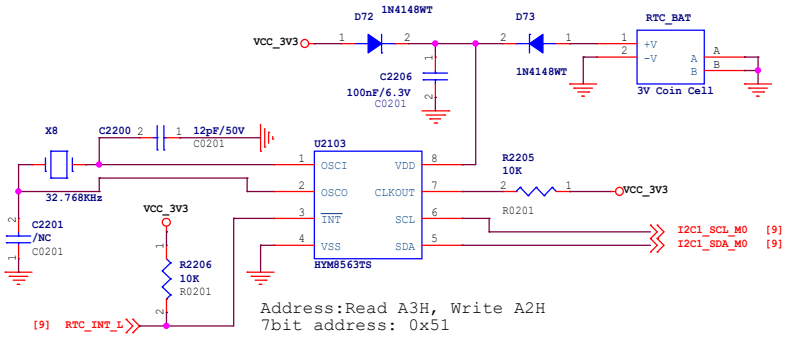
# VIN-1 USB-C, VCC5V0_SYS



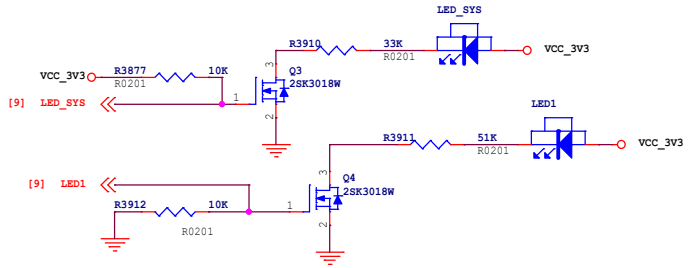

# VIN-2, Bebug UART




# RTC IC

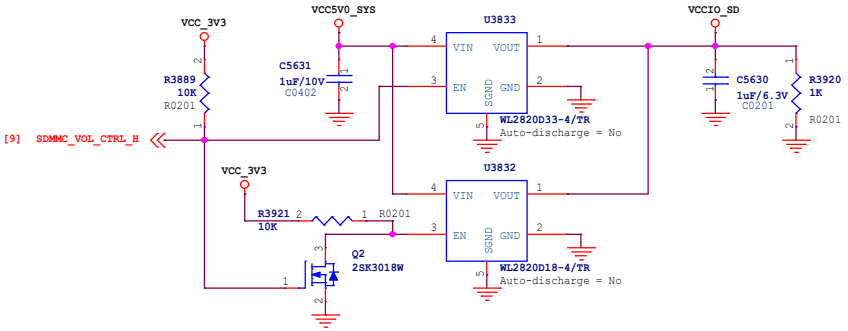


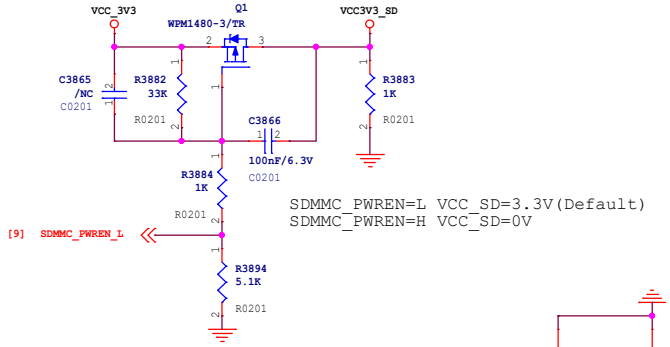

# LEDs

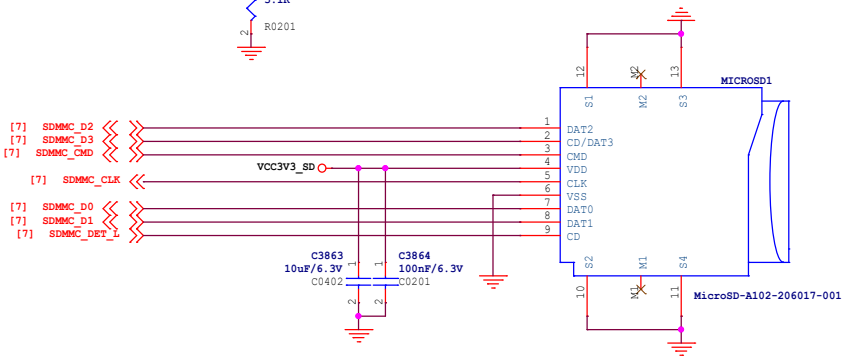


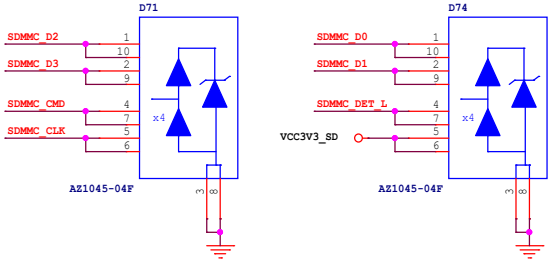

# microSD

SDIO2.0 SDMMC0_VOL_CTRL=H VCCIO_SD=3.3V(Default)
SDIO3.0 SDMMC0_VOL_CTRL=L VCCIO_SD=1.8V

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| Size A3 | Page Name 13.Power-IN/RTC/SD/Debug | |
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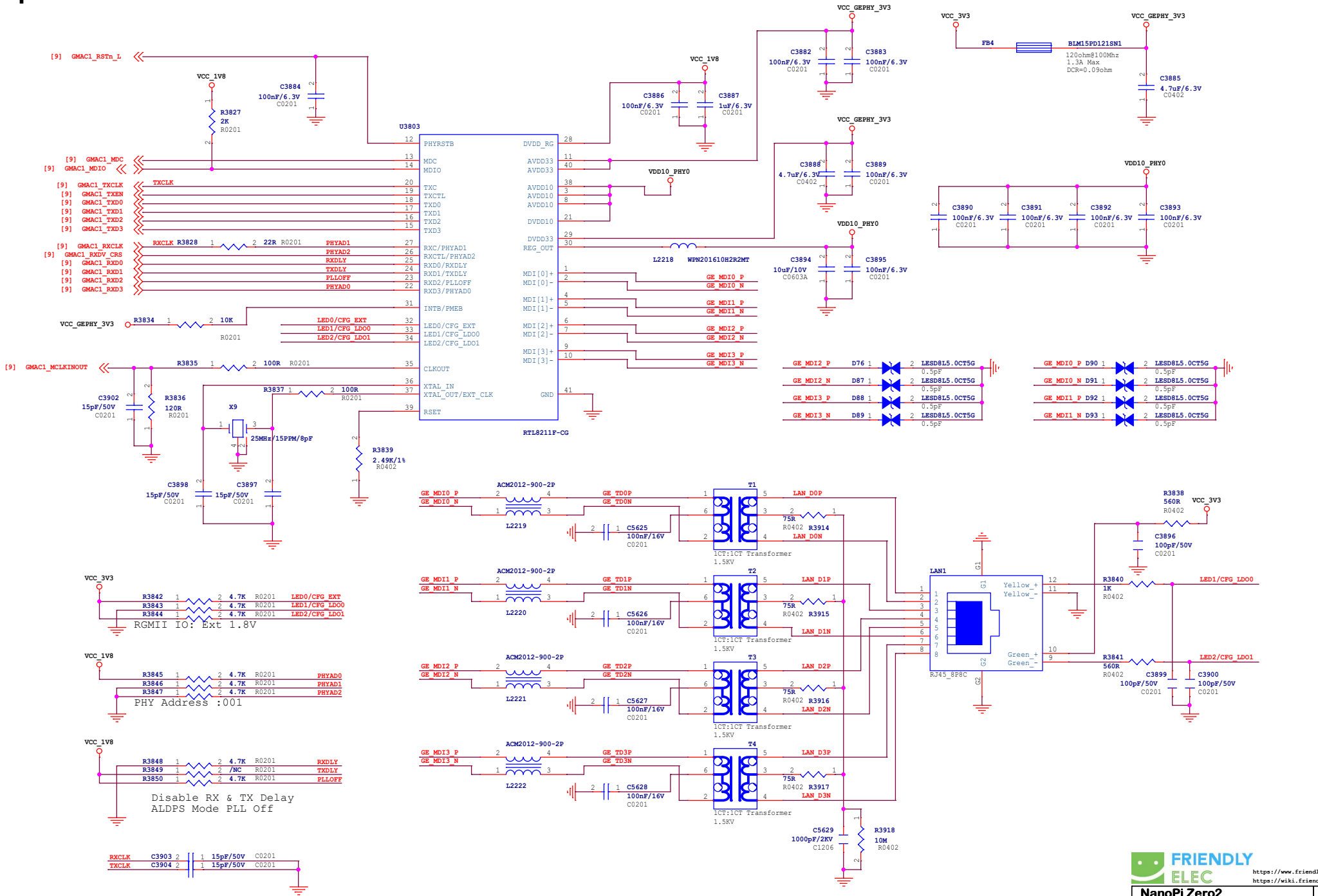
# Gbps Ethernet

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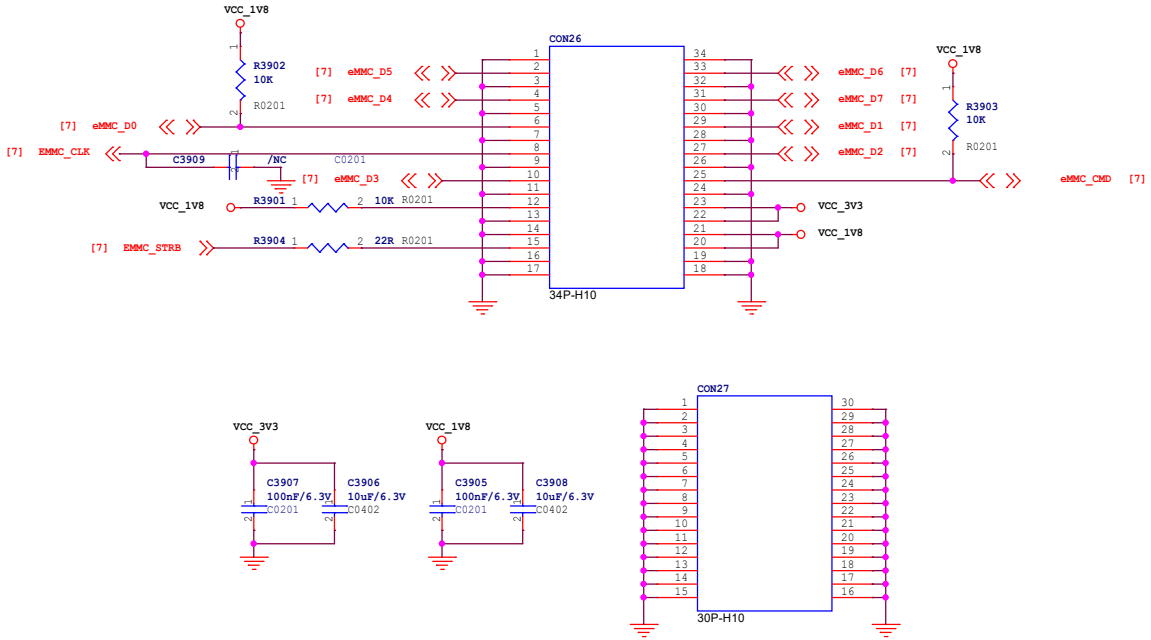
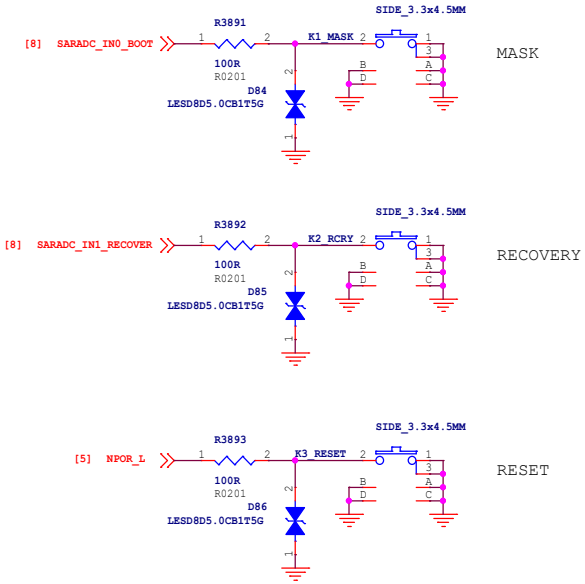
| NanoPi Zero2 | | Rev 2407 |
|---|---|---|
| Size A3 | Page Name 14.Gbps Ethernet | |
| Date: Monday, July 22, 2024 | | Sheet: 14/ 16 |

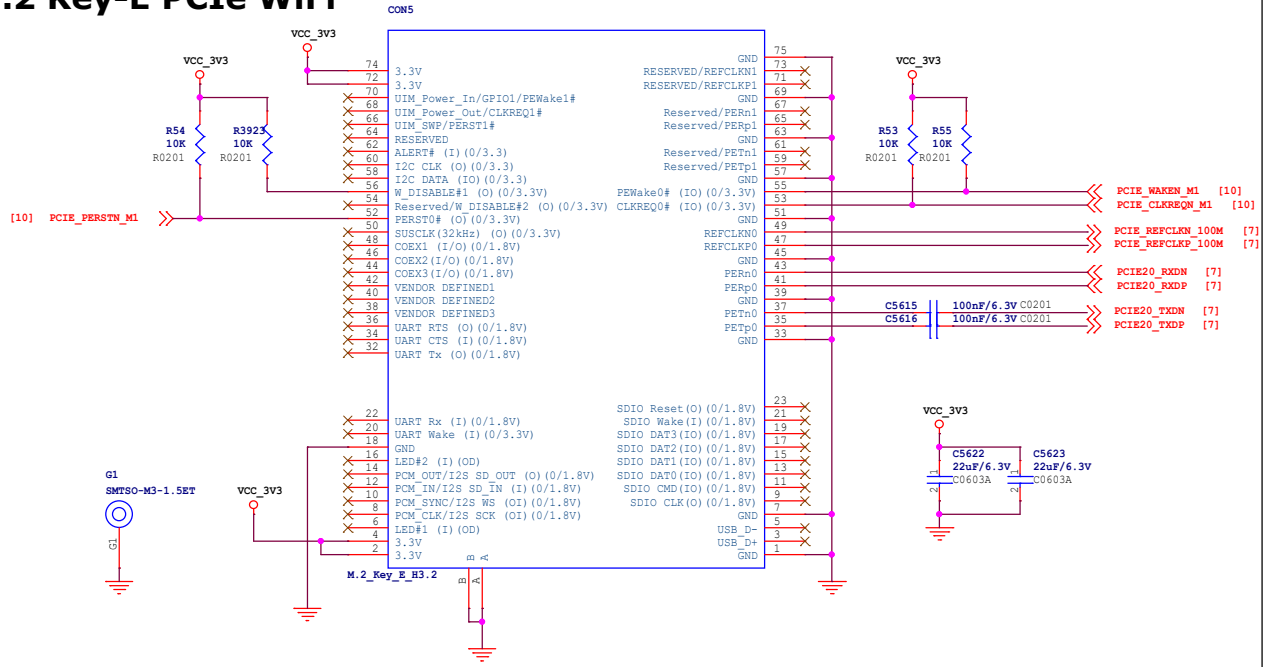
# eMMC Socket



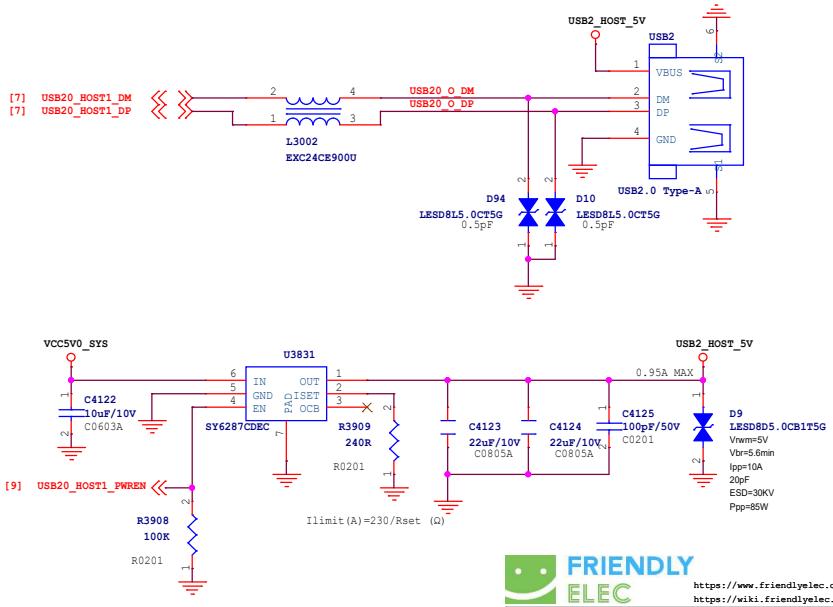

# Buttons




# M.2 Key-E PCIe WiFi




# USB2.0

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| Size A3 | Page Name 15.eMMC/M2/Buttons/USB |
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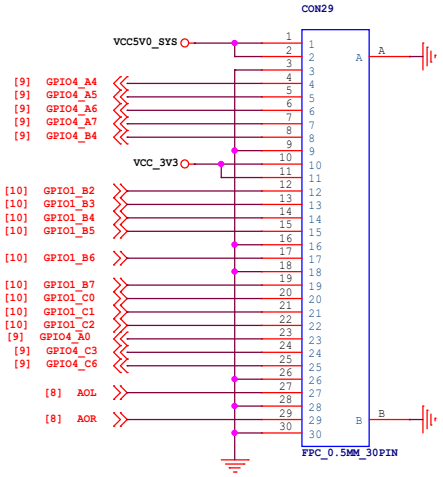
# GPIO




***TABLE***

| GPIOs | Alt Functions | | | Level |
|---|---|---|---|---|
| GPIO4_A0 | SPDIF_TX_M0 | | | 3.3V |
| GPIO4_A4 | UART1_CTSN | I2S1_MCLK | | 3.3V |
| GPIO4_A5 | UART1_RTSN | I2S1_SCLK | | 3.3V |
| GPIO4_A6 | UART1_TX_M0 | I2S1_LRCK | | 3.3V |
| GPIO4_A7 | UART1_RX_M0 | I2S1_SDO0 | | 3.3V |
| GPIO4_B4 | | I2S1_SDI0 | | 3.3V |
| GPIO4_C3 | PWM0_M0 | | | 3.3V |
| GPIO4_C6 | PWM3_M0 | | | 3.3V |
| GPIO1_C1 | SPI1_CSN0 | | | 3.3V |
| GPIO1_C2 | SPI1_CSN1 | | | 3.3V |
| GPIO1_B6 | SPI1_CLK | I2S0_LRCK_M1 | | 3.3V |
| GPIO1_B7 | SPI1_MOSI | I2S0_SDI_M1 | | 3.3V |
| GPIO1_C0 | SPI1_MISO | I2S0_SDO_M1 | | 3.3V |
| GPIO1_B4 | | I2S0_MCLK_M1 | | 3.3V |
| GPIO1_B5 | | I2S0_SCLK_M1 | | 3.3V |
| GPIO1_B2 | I2C5_SCL_M0* | UART7_TX_M1 | | 3.3V |
| GPIO1_B3 | I2C5_SDA_M0* | UART7_RX_M1 | | 3.3V |

* An external 2.2K pull-up resistor is required.